500 MS/s Dual Channel Digital Storage Oscilloscope

PM3323

Service Manual

4822 872 05333
890901

MAT3523

WARNING: These servicing instructions are for use by qualified personnel only. To avoid electric shock do not perform any servicing other than that contained in the Operating Instructions unless you are fully qualified to do so.

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IMPORTANT

In correspondence concerning this instrument, please quote the type number and serial number as given on the type plate.

NOTE : The design of this instrument is subject to continuous development and improvement.
Consequently, this instrument may incorporate minor changes in detail from the information contained in this manual.

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CONTENTS

SAFETY INSTRUCTIONS 1

INTRODUCTION ..... E

CHARACTERISTICS 3

PERFORMANCE CHECK 4

DISMANTLING THE INSTRUMENT 5

BLOCKDIAGRAM AND DESCRIPTION 6

INTRODUCTION TO CIRCUIT DESCRIPTIONS 7

CIRCUIT DESCRIPTIONS 8

ADJUSTING PROCEDURE 9

DISASSEMBLING AND ASSEMBLING 10

TROUBLE SHOOTING AND SERVICE DIAGNOSTICS 11

HANDLING OF COMPONENTS AND SOLDERING TECHNIQUES 12

SERVICE TOOLS 13

SAFETY INSPECTION AND TESTS AFTER REPAIR AND MAINTENANCE .. 14

PARTS LISTS 15

ACCESSORY INFORMATION 16

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SAFETY INSTRUCTIONS

SAFETY INSTRUCTIONS

CONTENTS

1.0 Safety instructions..... 1-1
1.1 Introduction..... 1-1
1.2 Safety precautions..... 1-1
1.3 Caution and warning statements..... 1-1
1.4 Symbols..... 1-1
1.5 Impaired safety protection..... 1-2
1.6 General clauses..... 1-2

1.0 SAFETY INSTRUCTIONS

Read these pages carefully before installation and use of the instrument.

1.1 INTRODUCTION

The following clauses contain information, cautions and warnings which must be followed to ensure safe operation and to retain the instrument in a safe condition.
Adjustment, maintenance and repair of the instrument shall be carried out only by qualified personnel.

1.2 SAFETY PRECAUTIONS

For the correct and safe use of this instrument it is essential that both operating and servicing personnel follow generally-accepted safety procedures in addition to the safety precautions specified in this manual.
Specific warning and caution statements, where they apply, will be found throughout the manual.
Where necessary, the warning and caution statements and/or symbols are marked on the apparatus.

1.3 CAUTION AND WARNING STATEMENTS

CAUTION: Is used to indicate correct operating or maintenance procedures in order to prevent damage to or destruction of the equipment or other property.

WARNING: Calls attention to a potential danger that requires correct procedures or practices in order to prevent personal injury.

1.4 SYMBOLS

High voltage ≥ 1000 V (red)

Live part (black/yellow)

Read the operating instructions

Protective earth (grounding) terminal (black)

1.5 IMPAIRED SAFETY PROTECTION

Whenever it is likely that safety-protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation. The matter should then be referred to qualified technicians.
Safety protection is likely to be impaired if, for example, the instrument fails to perform the intended measurements or shows visible damage.

1.6 GENERAL CLAUSES

1.6.1 WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts and accessible terminals which can be dangerous to live.

1.6.2 The instrument shall be disconnected from all voltage sources before it is opened.

1.6.3 Bear in mind that capacitors inside the instrument can hold their charge even if the instrument has been separated from all voltage sources.

1.6.4 WARNING: Any interruption of the protective earth conductor inside or outside the instrument, or disconnection of the protective earth terminal, is likely to make the instrument dangerous.
Intentional interruption is prohibited.

1.6.5 Components which are important for the safety of the instrument may only be renewed by components obtained through your local PHILIPS organisation. (See also chapter 12).

1.6.6 After repair and maintenance in the primary circuit, safety inspection and tests, as mentioned in chapter 14 have to be performed.

INTRODUCTION

INTRODUCTION

CONTENTS

2.0 Introduction..... 2-1

2.0 INTRODUCTION

This compact dual channel digital storage oscilloscope features an extensive sampling rate of 500 Megasamples/s with a vertical bandwidth of 300 MHz and a vertical resolution of 10 bit. An outstanding feature is the AUTO-SET pushbutton facility, which automatically sets various controls of the instrument to suit the input signal value. In this way, optimum ease of operation is obtained as the input signal immediately presents a correct, stable display on the bright C.R.T. screen.
The brightness is independent of the time base settings.
The M68000 microprocessor gives a wide choise of measurement and display possibilities, which can be selected via the ergonomic designed front panel.

Figure 2.1 500 Megasamples/s digital storage oscilloscope.

The oscilloscope is provided with integrated circuits (including thinfilm circuits), which guarantee highly-stable operation.

Furthermore, connection to the local mains is simplified by a tapless switched-mode power supply that covers most voltage ranges in use: 90 V...264 V a.c.

All these features make this oscilloscope suitable for a wide range of measuring applications.

CHARACTERISTICS 3

CHARACTERISTICS

CONTENTS

3.0 Characteristics..... 3-1
3.1 Cathode ray tube..... 3-2
3.2 Signal acquisition..... 3-3
3.3 Channels A and B..... 3-5
3.4 Time base..... 3-10
3.5 Trigger..... 3-10
3.6 Memory..... 3-13
3.7 Display..... 3-14
3.8 Setting memory..... 3-15
3.9 Calculation facilities..... 3-15
3.10 Auto setting..... 3-16
3.11 Cursors..... 3-19
3.12 Calibrator..... 3-19
3.13 Power supply..... 3-20
3.14 Options..... 3-21
3.15 Sundries..... 3-23
3.16 Mechanics..... 3-25
3.17 Environmental..... 3-26
3.18 Safety..... 3-29
3.19 Accessories..... 3-29
3.20 Optional versions..... 3-29

A. General

This instrument has been designed and tested in accordance with IEC publication 348 for Class I instruments.
This specification is valid after the instrument has warmed up for 30 minutes.

Properties expressed in numerical values with tolerances stated, are guaranteed by the manufacturer.
Numerical values without tolerances are typical and represent the characteristics of an average instrument.
Within 5 minutes after switching on, the temperature difference inside the instrument has reached 70 percent of its end value.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.1	CATHODE RAY TUBE		
3.1.1	Type	Philips D18-190GH/129	180 mm rectangular single beam tube.
3.1.2	Usefull screen area (h. x w.)	100 mm x 120 mm	For graticule see 3.1.7.
3.1.3	Screen type	GH (P31)	
3.1.4	Total acceleration voltage	16 kV	
3.1.5	Spot size	0,3 mm	Tube only.
3.1 6	Maximum trace distortion		Deviation from straight line.
	-@ screen periphery	1 mm	Outside central 80 mm (vert.) x 100 mm (hor.).
3.1.7	Graticule	Internal, fixed	
	-Illumination	Continuously variable	
	-Size (h. x w.)	80 mm x 100 mm	Centered @ 50 mm from top of CRT screen (hor.) and @ 50 mm from left edge of CRT screen (vert.).
	-Engravings		
	division lines	@ 10 mm	Horizontal and vertical.
	2 mm tick marks	@ 2 mm	On vertical and horizontal central axes.
	0.5 mm tick marks	@ 2 mm	On horizontal lines #2,3,4,6,7,8.
	dots	@ 2 mm	On dotted lines @ 1,5 div and 6,5 div from top of graticule.
	percentages	100-90-10-0 %	To facilitate rise and fall time measurements.
3.1.8	Orthogonality		Measured @ centre of screen.
		$90 \pm 0,5^{o}$	(Angle between X and Y axes, when traces are written in X- and Y direction alternately).

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.1.9	Intensity	Blank to max. intens.	Separate front panel controls for trace and text.
3.1.10	Focus	Manually set	Common screwdriver control on front for trace and text.
3.1.11	Trace rotation		Screw driver control on front; direction of screw driver rotation same as direction of trace rotation.
	-Minimum range	14°	Either X or Y trace can be aligned with graticule, when environmental magnetic field is within 0,1 mT.
3.2	SIGNAL ACQUISITION		
3.2.1	Sampling type		
	-@ 100 ns/div... 360 s/div:	Real time	
	-@ 5 ns/div... 50 ns/div:	Equivalent time	Random sampling.
3.2.2	Maximum sampling rate		Sampling rate depends on time/div setting.
	-Real time:	500 megasamples/s	
	-Equivalent time:	10 gigasamples/s	Repetitive only.
	-Ext. clock	50 kilosamples/s	Max. aperture uncertainty of 10 us.
3.2.3	Vertical (=voltage) resolution	10 bits	(= 0,1 % of full range).

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.2.4	Horizontal (=time) resolution		
	-In single Ch. or added Ch. acquisition		
	@ 1 ms/div... 5 s/div	4096 samp./acquisition	1 Sample = 0,025 % of full record.
	@ 5 ns/div... 500 us/div	512 samp./acquisition	1 Sample = 0,2 % of full record.
	-In dual channel acquisition		
	@ 1 ms/div... 5 s/div	2048 samp./acquisition	1 Sample = 0,05 % of full record.
	@ 5 ns/div... 500 us/div	512 samp./acquisition	1 Sample = 0,2 % of full record.
3.2.5	Record length	10,2 x time/div	Display in unmagnified position.
3.2.6	Acquisition time		
	-Real time	10,2 x time/div	
	5 s/div ... 1 ms/div	+ 1 ms/div	} }Exclusive delay time.
	500 us/div ... 200 ns/div	+ 10 ms	} }
	-Equivalent time		
	@ 5ns/div	2 s	} After this time there is a 99 % probability of all dots being updated to the new acquisition.
	@ 100 ns/div	10 ms	
3.2.7	Sources	Channel A	} Both channels can be inverted before acquisition.
		Channel B	
3.2.8	Acquisition modes	1 channel only	Full memory available for 1 channel.
		2 channels	Simultaneously sampled; 2 channels share memory.
		Ch.A and ch.B added	Full memory available for added channels.
		Average	Combined with 1 channel only, 2 channels or ch. A and ch. B added.
		MIN / MAX	Combined with 1 channel only, 2 channels or ch. A and ch. B added.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
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	@ 5 ns/div... 500 us/div	512 samp./acquisition	1 Sample = 0,2 % of full record.
3.2.5	Record length	10,2 x time/div	Display in unmagnified position.
3.2.6	Acquisition time		
	-Real time	10,2 x time/div	
	5 s/div ... 1 ms/div	+ 1 ms/div	} Exclusive delay time.
	500 us/div ... 200 ns/div	+ 10 ms	} Exclusive delay time.
	-Equivalent time		
	@ 5ns/div	2 s	} After this time there is a 99 % probability of all dots being updated to the new acquisition.
	@ 100 ns/div	10 ms	} After this time there is a 99 % probability of all dots being updated to the new acquisition.
3.2.7	Sources	Channel A	} Both channels can be inverted before acquisition.
		Channel B	} Both channels can be inverted before acquisition.
3.2.8	Acquisition modes	1 channel only	Full memory available for 1 channel.
		2 channels	Simultaneously sampled; 2 channels share memory.
		Ch.A and ch.B added	Full memory available for added channels.
		Average	Combined with 1 channel only, 2 channels or ch. A and ch. B added.
		MIN / MAX	Combined with 1 channel only, 2 channels or ch. A and ch. B added.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.2.9	Maximum time difference	200 ps	Two channels are sampled simultaneously.
3.3	CHANNELS A AND B		
3.3.1	Input connector	BNC with probe read-out	Probe read-out causes instrument to change V/div indication, input impedance and attenuator setting according to probe (when fitted with a probe indicator).
3.3.2	Input impedance (In high Z position)		For frequency > 1 MHz see Fig. 3.1.
	-R parallel	1 M Ohm ± 1 %	}In DC position of input coupling. In AC position of input coupling.: 18 nF in series with R par. & C par.
	-C parallel	14 pF	
			}In 0 position of input coupling: R par. = ∞.
	-Maximum input capacitance difference	1,5 pF	Capacitance difference between channel A, channel B and/or trigger input.
3.3.3	Input impedance (in 50 ohm position)		
	-R parallel	50 Ohm ± 1 %	In DC, AC and 0 position of input coupling.
3.3.4	Input coupling	a.c. d.c. 0	In 0 position: channel input disconnected from BNC and connected to ground.
3.3.5	Max. input voltage		Instrument should be properly grounded through the protective-ground conductor of the power cord.
	-In high Z position (d.c. + a.c. peak)	300 V	Up to 1 MHz; for freq. > 1 MHz see Fig. 3.2.
	-In 50 ohm position		
	d.c.	5 V	}
	a.c. (r.m.s.)	5 V	} Max. 50 mJ during any
	a.c. (peak)	50 V	} 100 ms interval.
			}

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.3.6	Deflection coefficient		Measured with a square wave signal of 2 kHz.
	-Steps	5 mV/div...5 V/div	In a 1-2-5 sequence of 10 steps.
	-Vernier ratio	1:2,7	Continuously variable between steps.
	Read out accuracy	± 15 %	
	-Error limit (Ambient:15..35°C)		Add 3 % for ambient: 0...50°C.
	overall	± 2 %	}Add 2% in 100 ns/div. }Vernier in 0 position.
	up to memory	± 2 %	}Add 2 % in MIN/MAX mode.
	-Non linearity acc. to IEC 351	3 %	
	additional error	± 15 %	Vernier not in 0 position.
3.3.7	Dynamic range	10 div	
3.3.8	D.c. offset control		Related to BNC input.
	-Range (± 5%)		Input voltage within the limits of 3.3.5.
	Att. @ 5 mV/div ...20 mV/div	± 5 V	}In AUTO OFFSET, the }offset is automatically }controlled such, that }average d.c. level of }signal is presented at }screen centre (± }2 div), provided signal }is within offset range. }Shift is set to zero }(mid) level.
	Att. @ 50 mV/div ...0,2 V/div	± 50 V	
	Att. @ 0,5 V/div ...5 V/div	± 300 V	
	-Resolution (± 5%)		
	Att. @ 5 mV/div ...20 mV/div	5 mV	
	Att. @ 50 mV/div ...0,2 V/div	50 mV	
	Att. @ 0,5 V/div ...5 V/div	0,5 V	
3.3.9	Shift range	± 5 div	From screen centre.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.3.10	Frequency response (in 50 ohm position)		Z source: 50 Ohm
	-Lower transition point of BW		
	Input coupling in DC position	d.c.	
	Input coupling in AC position	$\leq$ 10 Hz	
	-Upper transition point of BW (Ambient: 15..35°C)	$\geq$ 300 MHz (-3 dB)	Deviation max. 30 MHz for ambient: 0...50°C.
3.3.11	Freq. resp. (In hi.Z pos. through probe)		Z source = 25 Ohm. Probe according to 3.19.
	-Lower transition point of BW		
	Input coupling in DC position	d.c.	
	Input coupling in AC position	$\leq$ 1 Hz	
	-Upper transition point of BW (Ambient: 15..35°C)	$\geq$ 300 MHz (-3 dB)	Deviation max. 30 MHz for ambient: 0...50°C.
3.3.12	Bandwidth limiter		
	-Starting point of HF rejection	20 MHz (-3 dB)	
	-Slope	6 dB/octave	
3.3.13	Pulse response (in 50 Ohm position) (exclusive first mm after transient)		Z source = 50 Ohm; measured over central 6 div.
	-Rise time (Ambient: 15..35°C)	$\leq$ 1,1 ns	(Calculated from bandwidth x Rise time = 0,35). Add max. 0,25 ns for ambient: 0...50°C.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.3.14	Pulse resp. (in hi.Z pos. through probe) (exclusive first mm after transient)		Z source: = 50 Ohm; measured over central 6 div. Probe according to 3.19.
	-Rise time (Ambient: 15..35°C)	$\leq$ 1,1 ns	(Calculated from bandwidth x Rise Time = 0,35). Add max. 0,25 ns for ambient: 0...50°C.
3.3.15	Max. base line instability		
	-Jump (Ambient 15..35°C):		Add 25 % for ambient: 0...50°C.
	when switching to added mode	0,3 div	
	when switching to MIN / MAX mode	0,5 div	
	between any V/div positions	0,15 div	
	when actuating inverter switch	0,3 div	
	between AC, 0 and DC position	0,1 div	
	when rotating vernier	0,6 div	Input externally grounded.
	between any time/div positions	0,6 div	
	when switching to magn. x5	0,5 div	
	-Drift	0,1 div/h	}
	-Temperature coefficient	$\pm$ 0,05 div/K	}Measured in 20 mV/div }position. }

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.3.16	Common mode rejection ratio		Both channels @ same attenuator setting; vernier for V/div setting adjusted for optimal CMMR at 10 kHz measured with max. 8 div input signal on each channel, (± 4 div around zero).
	-@ 1 MHz	100:1	
	-@ 50 MHz	20:1	
3.3.17	MIN / MAX function		Time base setting 5 us/div ... 360 s/div. Average switched off.
	-Accuracy > 50 %	@ pulse > 3 ns	
	-Reset time	20 ns	
3.3.18	Average		Average formula after the first front change (MIN / MAX switched off).
	Constant is max.	64x	$So(n)=So(n-1)+\frac{Sn-So(n-1)}{C}$
		32 x or off	In ROLL mode.
3.3.19	Cross talk (according to IEC 351)	<-30 dB @ 100 MHz <-50 dB @ 2 MHz	

3

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.4	TIME BASE		
3.4.1	Modes	Recurrent Single shot Single scan Multiple shot Multiple scan Roll Save/Stop on difference	 Up to 4 shots. Up to 4 scans. Can be stopped manually or by trigger.
3.4.2	Time coefficients		
	-In recurrent	5 ns/div...5 s/div	
	-In single scan and multiple scan	5 ns/div...50 ns/div	
	-In single shot and multiple shot	100 ns/div...5 s/div	
	-In roll mode	50 ms/div...360 s/div	
	-With EXT CLOCK	Depending on clock frequency	Input via EXT CLOCK, every clock pulse a sample is taken, so for single channel 4k samples are stored and for dual channel 2 times 2k samples.
	-Error limit (Ambient 15..35 ^{o}C)		
	In equivalent time mode	$\pm$ 4 %	
	In real time mode	$\pm$ 1 %	Add 0,5 % for ambient: 0...50°C.
	Up to memory	$\pm$ 0,01 %	
3.5	TRIGGER		
3.5.1	Sources		
	-Signal trigger	Channel A Channel B EXT LINE	
	-Events	EXT	Serves as delay to signal trigger.
3.5.2	Input connectors	BNC	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.5.3	Input impedance of EXT trigger inputs		
	-R parallel	1 M Ohm ± 1 %	In DC position of input coupling.
	-C parallel	14 pF	
	-Max. input capacitance difference	1,5 pF	Difference between channel A, channel B and EXT trigger input.
3.5.4	Coupling		
	-Signal trigger	d.c. a.c. LF rejected HF rejected Auto level TVF	According to CCIR.
	-Clock & events trigger level	TTL ECL Through variable level	Adjustable via menu "trigger coupling" - events.
3.5.5	Max. input voltage (d.c. + a.c. peak)		Instrument should be properly earthed through the protective-earth conductor of the power cord.
	-Clock trigger	300 V	
3.5.6	Signal trigger sensitivity (Ambient 15..35°C)		Add 10 % for ambient: 0...50°C.
	-Channel A or B		
	@ 300 MHz	≤ 4 div	
	@ 200 MHz	≤ 1,5 div	
	@ 30 MHz	≤ 0,5 div	
	-EXT		
	@ 300 MHz	≤ 300 mV	
	@ 200 MHz	≤ 0,1 V	
	@ 30 MHz	≤ 0,05 V	
	-EXT/10		
	@ 300 MHz	≤ 3 V	
	@ 200 MHz	≤ 1 V	
	@ 20 MHz	≤ 1 V	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.5.7	Slope selection	Positive going Negative going Dual slope	Level adjustable; not effective in random sampling and TVF.
3.5.8	Signal level control range		
	-Channel A or B	± 8 div	} }When not in AUTO position
	-EXT	± 0,8 V	}of trigger mode. }
	-EXT/10	± 8 V	}
	-DUAL	± 5 div	}
	-Any source	Related to peak value	}In AUTO position of trig- }ger mode.
3.5.9	Frequency response		Trigger BW not affected by bandwidth limiter.
	-Lower transition point of BW		Ch. A and Ch. B coupling cascaded with trig. coupl.
	Trigger coupling in DC position	d.c.	
	Trigger coupling in AC position	10 Hz (- 3dB)	
	Trigger coupling in LF reject pos.	50 kHz (- 3 dB)	
	-Higher transition point of BW	see also 3.5.6.	
	Trigger coupling in HF reject pos.	50 kHz (-3 dB)	
3.5.10	Trigger delay		
	-Range	-10...9999 div	}can also be indicated in }time.
	@ 5 ns/div ... 100 ns/div	-10...500 div	} }
	-Number of events	1...9999	
	Max. frequency	5 MHz	
	-Accuracy	± 1 %	
	@ 5 ns/div ... 100 ns/div	± 3 % ± 5 ns	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.6	MEMORY		
3.6.1	Memory size		
	-Registers	4	Registers #0, #1, #2, #3
	-Register depth	4096 words	
	-Wordlength	10 bits	
3.6.2	Functions	Clear	Register #0 is cleared, incl. pre-trigger memory and blanked if DOTS is selected.
		Save	Contents of register #0 is saved in selected register (#1, #2 or #3).
		Write	Acquired signal is written into register #0.
		Lock	Memory system is locked, including register #0.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.7	DISPLAY		
3.7.1	Sources	Register #0 Register #1 Register #2 Register #3	} }In any combination. } }
3.7.2	Display expansion		
	-Horizontal		
	Steps:	1x...64x	In Y versus t mode.
		1x...8x	In A versus B mode.
	Vernier ratio	1:2	Continuously variable between steps. Recalculated value is displayed with an accuracy of ± 5 %.
	-Vertical		
	Steps:	0.2x, 1x and 5x	Both in Y versus t and A versus B modes.
3.7.3	Display manipulations	Smooth	Reduces noise by adding a filter in the display section, that is only effective at time base 500 us/div ... 360 s/div.
		Dot join	Linearly interpolated between measured dots.
		Invert	Alle registers can be inverted.
3.7.4	Position range		All channels can be positioned independently.
	-Horizontal	± 5 div	From screen centre.
	-Vertical	± 5 div	From screen centre.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.8	SETTING MEMORY		
3.8.1	Memory size	Max. 251 front settings	
3.8.2	Functions		
		Save	Actual settings are stored in memory, replacing contents of memory cell indicated on CRT.
		Insert	Actual settings are stored in memory; insertion is after memory cell indicated on CRT.
		Delete	Contents of memory cell indicated on CRT is deleted.
		Recall	Actual settings are replaced by contents of memory cell indicated on CRT. Actual settings are saved in "back-up" memory (= mem. cell #0).
		(Recall) Next	Actual settings are replaced by contents of memory cell indicated on CRT increased by 1. Actual settings are saved in "back-up" memory (= memory cell #0).
		(Recall) Previous	Actual settings are replaced by contents of memory cell indicated on CRT decreased by 1. Actual settings are saved in "back-up" memory (= memory cell #0).

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.9	ANALYZE FACILITIES		
3.9.1	Measure		
	-Amplitude	RMS value Mean value Peak to peak voltage Peak to zero voltage Overshoot Preshoot	} }Including or excluding } }offset voltage }Result calculated from }part between cursors or }markers. }
	-Time	Risetime Pulse width Duty cycle Frequency Phase	
3.9.2	Mathematics		
		Add Subtract Multiply Divide Differentiate Integrate Delay channel	} }Results of calculation }displayed in selected }register and scalable }for optimum display } }
		Histogram	Amplitude density vs. absolute amplitude of an input signal
		Filter	Digital filter of order 3,5,9,17,33,65,129.
3.10	AUTO SETTING		
3.10.1	Settling time	Typical 3 s	During plot, AUTO SET is not possible.
3.10.2	CRT functions		
	-Focus	Not influenced	
	-Trace intens	Not influenced	
	-Text intens	Not influenced	
3.10.3	Display functions		
	-Select	To register #0	
	-X-position	Zero	
	-Y-position	Zero	
	-Invert	Off	Only for register #0.
	-X-expand	*1	Vernier calibrated.
	-Y-expand	*1	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.10.4	Cursors	Off	
	-Calculation	Off	
3.10.5	Text		
	-Reduced	Off	
	-Bottom text lines	Not affected	
3.10.6	Vertical acquisition		
	Y-deflection source	Every source having a triggerable signal at its output	}Channel A if no trigger }is found. }
	Input impedance		
	-Accessory with probe read out	According to probe read out	
	-Otherwise	Not affected by AUTO SET	
	Input coupling	ac	
	Y-deflection		Each channel is independently set.
	-10 mV <input voltage <30 V	Approx. 4 div	} }Vernier in calibrated }position.
	-Input voltage <10 mV	Channel at 200 mV/div	} }
			Due to trigger uncertainty at freq. > 60 MHz or at duty cycle <> 50% sensitivity can deviate from above, but signal will remain on the screen.
	Channel inverter	Off	
	-Add	Off	
	-MIN / MAX	Off	
	-Bandwidth limiter	Off	
	-Average	Off	
	-Offset	Not affected	Offset is neglected due to a.c. coupling.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
	Y base line position		
	-In single channel display	Centre of screen ± 0,3 div	
	-In dual channel display		
	Ch. A	2 ± 0,3 div above centre screen	
	Ch. B	2 ± 0,3 div below centre screen	
3.10.7	Horizontal acquisition		
	Mode	RECURRENT MAX. RESOLUTION	
	External clock	Off	
	TB deflection coefficient		For TVF not affected.
	-Signal frequency 40 Hz ... 80 MHz	Min. 2, max 6 signal periods over 10 div.	
	-Signal freq. > 80 MHz	5 ns/div	
	-When no trigger found	2 ms/div	
3.10.8	Triggering		
	-Delay negative delay	Off not affected	For TVF not affected.
	-Events	Off	For TVF not affected.
	-Source		
	Triggerable signal @ ext input	Ext	If External was selected.
	No signal @ ext input, but trigg. signal @ channel A or B	Channel A or B	Channel with lowest input frequency is selected. (Channel A when frequencies are equal).
	No triggerable signal @ any input	Channel A	
	-Mode	Auto	For TVF not affected
	-Level	50 ... 70% of peak to peak value	DC component of signal neglected.
	-LF reject	Off	
	-HF reject	Off	
	-Slope	Positive	For TVF not affected.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.11	CURSORS		
3.11.1	Cursor intensity control	Independent of trace intensity but combined with text intensity	
3.11.2	Horizontal resolution		
	-In single channel mode	1 : 4096	
	-In dual channel mode	1 : 2048	
3.11.3	Vertical resolution	1 : 1024	
3.11.4	Read out resolution	3 digits	
3.11.5	Voltage cursors		
	-Error limit Ambient: 15..35°C	± 2 % In accordance with specification of vertical channels, points 3.3.6 error limit and points 3.3.8 to 3.3.16 inclusive.	Referred to input at BNC, error of probes etc. excluded. Add 3 % for ambient: 0...50°C.
	-Cursor Range	Visible part of signal	Cursors cannot pass each other (to avoid negative readings).
3.11.6	Time cursors		
	-Error limit	± 0,2 %	
3.12	CALIBRATOR		
3.12.1	Wave form		
	-Shape	Square wave	
3.12.2	Internal impedance	50 Ohm ± 1 %	
3.12.3	Output voltage (peak to peak)	1 V ± 1 %	Open voltage. Halves when terminated with 50 Ohm. Positive going with respect to ground.
3.12.4	Output current (peak to peak)	20 mA ± 2 %	Output short circuited. Halves when terminated with 50 Ohm.
3.12.5	Frequency	2 kHz	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.13	POWER SUPPLY		
3.13.1	Source voltage a.c. (r.m.s)		
	-Nominal	100 V ... 240 V	
	-Limits of operation	90 V ... 264 V	
3.13.2	Source frequency		
	-Nominal	50 Hz ... 400 Hz	
	-Limits of operation	45 Hz ... 440 Hz	
3.13.3	Source waveform characteristics		@ Nominal source voltage.
	-Max. waveform deviation factor	10%	
	-Crest factor	1,27...1,56	
3.13.4	Allowable power source interruption	At least 20 ms	@ Nominal source voltage. After this time oscilloscope settings are saved before instrument goes down. Automatic power up after restoration of Power line voltage. (For setting retention: see 3.15.1).
3.13.5	Power consumption (a.c. source)		@ Nominal source voltage.
	-Nominal	170 W	

3.14 OPTIONS

For specification of an option refer to the separate manual of the option.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.15	SUNDRIES		
3.15.1	Data and settings retention		When instrument is switched off or during mains failure.
	-Memory back up voltage	2 V ... 3 V	
	-Memory back up current drain	Typical 300 uA	@ 25°C (with interface PM8956A installed).
	-Recommended Batteries:		
	type	NCR 6	According to Nickel Cadmium penlight battery e.g. PHILIPS NCR6 (9299 000 40622).
	quantity	2 pcs	(=9299 000 40636)
	-Temperature rise of batteries	20 K	After warming up period of instrument.
	-Retention time	Typical $\geq$ 2 months	@ 25°C, with recommended (fully charged) batteries.
	-Temperature Range	0...+70°C	@ -40...0°C settings retention is uncertain. It is advised to remove batteries from instrument when it is stored during longer period (> 24 h) below -30°C or above 60°C. UNDER NO CIRCUMSTANCES BATTERIES SHOULD BE LEFT IN THE INSTRUMENT @ TEMPERATURES BEYOND THE RATED RANGE OF THE BATTERY SPECIFICATIONS!

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.15.2	Probe Read Out		With Philips probe provided with indicator ring.
	-Input impedance setting		
	Passive high impedance probe	}Fixed @ 1 MOhm	
	Passive 50 Ohm probe	}	
	Passive 50 Ohm attenuator	}	
	Passive 75 Ohm in 50 Ohm out attenuator	}Fixed @ 50 Ohm	
	Active current probe	}	
	Active isolation probe	}	
	-Vertical sensitivity setting		
	Passive probe	Not affected	
	Passive attenuator	Not affected	
	Active current probe	20 mV/div	Can be manually changed.
	Active isolation probe	20 mV/div	Can be manually changed.
	-V/div and voltage cursor read out		
	Passive 10:1 probe	10 x higher	}
	Passive 10 x attenuator	10 x higher	}
	Passive 100:1 probe	100 x higher	}Offset read out is changed accordingly.
	Passive 100 x attenuator	100 x higher	}
	Active current probe	In divisions	}
	Active isolation probe	In divisions	}

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.15.3	Analog plot output		
	-Connector	DIN 5 pole 45°	
	-Functions	Screen dump	Included channel identifier.
		Memory dump	Register selectable.
	-Sensitivity	1 V/Full screen ± 3 % 1 V/Full memory ± 3 %	} }Horizontal and vertical. } }
	-Pen lift	TTL compatible	Pen-up is selectable (0 or 1). Open collector output; max. 12 V.
	-Plot time per dot	20 ms .. 2 s	Software selectable. Signal dependent.
	-Plot sequence	Channel A first	In dual channel operation; with more registers starting with the lowest number.
3.16	MECHANICS		
3.16.1	Height		Fits 5E in 19 inch rack.
	-Without feet and accessory pouch	176 mm (6,9 in.)	Add 15. mm (0,6 in.) for feet.
	-Feet and accessory pouch included	250 mm (9,8 in.)	
3.16.2	Width	419 mm (16,5 in.)	Add 46 mm (1,8 in.) for handle.
3.16.3	Depth		
	-Handle excluded	570 mm (22,5 in.)	Add 35 mm (1,4 in.) for protective front cover.
	-With extended handle	670 mm (26,4 in.)	
3.16.4	Mass	18 kg	
3.16.5	Finish	Epoxy powder coated	
3.16.6	Printed circuit boards	Glass laminate epoxy	
3.16.7	Cooling	Fan aided convection	Maintenance free. To allow air convection, at least 1,5 cm free space is required below the oscilloscope.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.17	ENVIRONMENTAL		
3.17.1	General		
	The characteristics are valid only if instrument is checked inaccordance with the official checking procedures. Details on these procedures and failure criteria are supplied on request.		
3.17.2	Meets environmental requirements of	MIL-T-28800C Type III Class 5, Style D	
3.17.3	Temperature		Memory back-up batteries removed from instrument, unless batteries meet temperature specifications (see also 3.15.1).
	-Operating		
	Min. low temperature	0°C	Cf. MIL-T-28800D par. 3.9.2.3 tested cf. par. 4.5.5.1.1.
	Max. high temperature	+ 50°C	Cf. MIL-T-28800D par. 3.9.2.4 tested cf. par. 4.5.5.1.1.
	-Non operating (Storage)		
	Min. low temperature	-40°C	Cf. MIL-T-28800D par. 3.9.2.3 tested cf. par. 4.5.5.1.1.
	Max. high temperature	+ 75°C	Cf. MIL-T-28800D par. 3.9.2.4 tested cf. par. 4.5.5.1.1.
3.17.4	Maximum humidity		Cf. MIL-T-28800D par. 3.9.2.2 tested cf. par. 4.5.5.1.1.
	-Operating and non-operating (Storage)	95% Relative humidity	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.17.5	Maximum altitude		Cf. MIL-T-28800D par. 3.9.3 tested cf. par. 4.5.5.2. Memory Back-up batteries removed from instrument, unless batteries meet maximum altitude specs.
	-Operating	4,5 km (15000 feet)	Maximum operating temperature derated 3 °C for each km (for each 3000 feet) above sea level.
	-Non-operating (storage)	12 km (40000 feet)	
3.17.6	Vibration (Operating)		Cf. MIL-T-28800D par. 3.9.4.1 tested cf. par. 4.5.5.3.1.
	-Freq. 5...15 Hz		
	Sweep time	7 min	
	Excursion (pk to pk)	1,5 mm	
	Max acceleration	7 m/s^2 (0,7 x g)	@ 15 Hz.
	-Freq. 5...25 Hz		
	Sweep time	3 min	
	Excursion (pk to pk)	1,0 mm	
	Max acceleration	13 m/s^2 (1,3 x g)	@ 25 Hz.
	-Freq. 25...55 Hz		
	Sweep time	5 min	
	Excursion (pk to pk)	0,5 mm	
	Max acceleration	30 m/s^2 (3,0 x g)	@ 55 Hz.
	-Resonance dwell	10 min	@ each resonance freq. (or @ 33 Hz if no resonance was found). Excursion cf. 3.17.6.
3.17.7	Shock (Operating)		Cf. MIL-T-28800D par. 3.9.5.1 tested cf. par. 4.5.5.4.1.
	-Amount of shocks		
	total	18	
	each axis	6	(3 in each direction).
	-Shock wave form	half sine wave	
	-Duration	11 ms	
	-Peak acceleration	300 m/s^2 (30 x g)	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.17.8	Bench handling		Cf. MIL-T-28800D par. 3.9.5.3 tested cf. par. 4.5.5.4.3.
	-Meets requirements of:	MIL-STD-810 methode 516, proced. V	
3.17.9	Salt atmosphere		Cf. MIL-T-28800D par. 3.9.8.1 tested cf. par. 4.5.6.2.1.
	-Structural parts meet requirements of:	MIL-STD-810 methode 509, proced. I salt solution 20%	
3.17.10	EMI (Electro magnetic interference) meets requirements of:	MIL-STD-461	Applicable requirements of Part 7: CE03, CE07, CS01, CS02, CS06, RE02, RS02, RS03.
3.17.11	Magnetic radiated susceptibility		Tested conforming IEC 351-1 par. 5.1.3.1.
	-Maximum deflection factor	7 mm/mT (0,7 mm/gauss)	Measured with instrument in a homogeneous magnetic field (in any direction with respect to instrument) with a flux intensity (peak to peak value) of 1,42 mT (14,2 gauss) and of symmetrical sine wave form with a frequency of 45...66 Hz.
3.17.12	Packing		
	Meets requirements of:	NLN-L88	
3.17.13	Transportation		
	Meets requirements of:	AN-D628	
	-Packaged transportation drop		
	meets requirements of:	Nat. safe transp. ass. procedure 1A-B-2	
	-Packed transportation vibration		
	meets requirements of:	Nat. safe transp. ass. procedure 1A-B-1	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.18	SAFETY		
3.18.1	Meets requirements of:	IEC 348 Class I VDE 0411 Class I UL 1244 CSA 556B	
3.18.2	Approvals	CSA 556B (applied for)	
3.19	ACCESSORIES		
3.19.1	Accessories furnished with instrument	2 x PM8929/39	10 MOhm, 10:1 passive probe with read out (1,5 m).
		Blue contrast filter	Factory installed.
		Operating manual	
		Front cover Plot probe	
3.20	OPTIONAL VERSIONS		
3.20.1	General		These options can be factory installed only.
3.20.2	Power Cord		Length 2,1m , (82,7 in.).
		Universal european U.S.A. United kingdom Swiss Australian	VDE, KEMA listed. CSA, UL listed. BSI listed. SAV listed. SAA listed.
3.20.3	Cabinet	Rack mount	
3.20.4	IEEE 488/RS232-C interface	Option	
3.20.5	F.F.T.	Option	

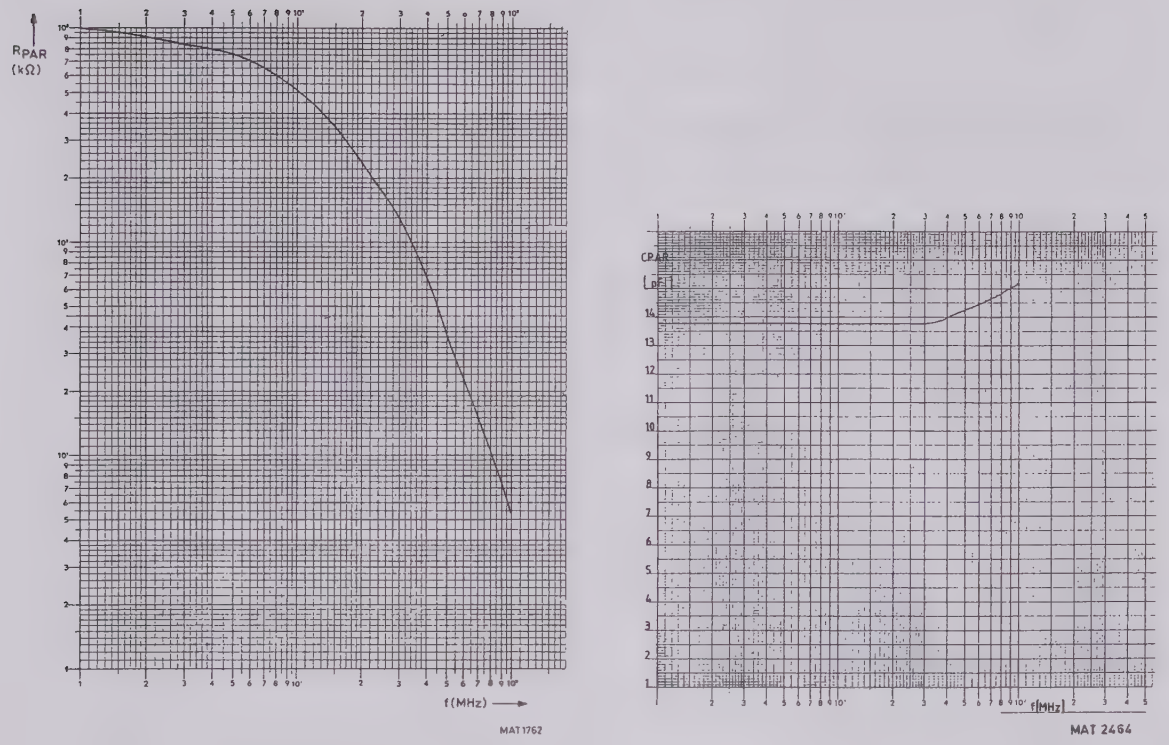


Figure 3.1. Input resistance Rpar. and capacitance Cpar. versus frequency.

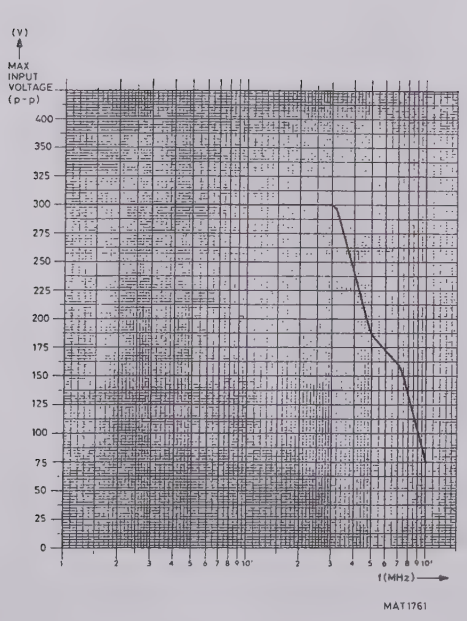


Figure 3.2. Maximum input voltage (peak to peak) derating versus frequency.

PERFORMANCE CHECK

PERFORMANCE CHECK

CONTENTS

4.0 Performance check..... 4-1
4.1 General information..... 4-1
4.2 Recommended test and calibration equipment..... 4-2
4.3 Preliminary settings..... 4-2
4.4 Checking procedure..... 4-3

4.0 PERFORMANCE CHECK

4.1 GENERAL INFORMATION

WARNING: Before switching on, ensure that the instrument has been installed in accordance with the Installation Instructions outlined in chapter 3.0 of the Operating Manual.

This procedure is intended to:

- check the instruments´specification.
- be used for incoming inspection to determine the acceptability of newly purchased instruments and/or recently recalibrated instruments.
- check the necessity of recalibration after the specified recalibration intervals.

NOTE: The procedure does not check every facet of the instrument´s calibration; rather, it is concerned primarily with those parts of the instrument which are essential to measurement accuracy and correct operation. Removing the instrument covers is not necessary to perform this procedure. All checks are made from the outside of the instrument.

If the test is started within a short period after switching on, bear in mind that steps may be out of specification, due to insufficient warming-up time.

Warming-up time under average conditions is 30 minutes.

The performance checks are made with a stable, well-focussed, low-intensity display. Unless otherwise noted, adjust the intensity and level controls as needed.

NOTES :

* At the start of every check, the controls always occupy the preliminary settings AUTO SET position, unless otherwise stated.

* The input voltage has to be supplied to the channel A input; unless otherwise stated.
Unless otherwise stated, the switches TIME/DIV, SHIFT A and B, X-POSITION, TRACE INTENS and TEXT INTENS must be put in such a position that a good read-out of the phenomena of interest is obtained.

* Tolerances given are for the instrument under test and do not include test equipment error.

* The given input impedance of the oscilloscope under test (being 50 ohm or 1 megaohm) are valid if the generator types are used that are given in chapter 13.1 "Recommended test and calibration equipment". If you use other types, the input impedances may be different.

* For some checks, we make use of service routines. If you want additional information concerning these service routines refer to chapter 11 "Trouble shooting".

* In some checks in this chapter channel B is mentioned between brackets behind channel A. It is advised to perform the channel A checks first. After that the checks for channel B can be done.

4.2 RECOMMENDED TEST AND CALIBRATION EQUIPMENT

A complete list of all material necessary for both this performance check and also the adjusting procedure is given in chapter 13.1 in this manual.

4.3 PRELIMINARY SETTINGS

- Switch the oscilloscope on.
- Check that all the LEDs in the front panel are on for 1 sec. during the power up routine of the instrument´s microprocessor.
- Press AUTO SET.
- Check that after adjustment of TEXT INTENS and TRACE INTENS the read-out information and a horizontal line become visible at the CRT-screen.

A.	POWER SUPPLY	
	IMPORTANT	The measurements of the power supply must be done with life voltages. Therefore it is strongly advised to use a variable mains transformer with isolated primary and secondary windings. Nevertheless, these tests must only be done by a qualified technician who is aware of the danger involved.
A.1	SUBJECT	Mains voltage range.
	TEST EQUIPMENT	Variable mains voltage transformer (and digital multimeter).
	SETTINGS	- Connect the oscilloscope (switched off) to the output of the variable mains voltage transformer. If the transformer has no output voltage read-out, you must connect the digital multimeter (a.c. voltage range) to the outputs of the transformer. - Connect the variable mains transformer to the mains and adjust the output voltage.
	REQUIREMENTS	- Check that the oscilloscope starts up normally when switched on at any voltage in the range 90...264 V (a.c). Preferred check points are 110, 220 and 240 V (a.c.).
	MEASURING RESULTS	.....
	SETTINGS	- Switch the oscilloscope on at a mains voltage between 90...264 V (a.c.). - Connect the input of Ch. A with the CAL voltage. - Press AUTO SET. - Adjust AMPL/DIV of Ch. A, TIME/DIV and other controls to a nice display of the CAL output voltage.
	REQUIREMENTS	- Check that the display stays stable over the mains voltage range 90...264 V (a.c.).
	MEASURING RESULTS	.....
		- Switch the oscilloscope off and disconnect the variable transformer from the mains.

A.2 SUBJECT

Mains voltage current.

TEST EQUIPMENT

Variable mains voltage transformer and digital multimeter.

SETTINGS

- Connect the oscilloscope to the variable mains transformer. In one of the mains conductors of the oscilloscope the digital multimeter (a.c. current range) must be present.
- Connect the transformer to the mains and switch the oscilloscope on. Graticule illumination must be on.

REQUIREMENTS

- Measure the current drain of the oscilloscope according to the table below (rms value). This current depends on the applied mains voltage and from the fact if the IEEE option is installed or not. The current with installed option is mentioned between brackets.

Mains voltage:	Current:
110 V (a.c.)	1,2 A (1,4 A)
220 V (a.c.)	0,55 A (0,65 A)
240 V (a.c.)	0,5 A (0,6 A)

MEASURING RESULTS .....

Disconnect the variable mains transformer from the mains and connect the oscilloscope directly to the mains voltage.

B.	C.R.T. DISPLAY SECTION	
B.1	SUBJECT	Trace distortion.
	TEST EQUIPMENT	LF sine wave generator.
	SETTINGS	- Press AUTO SET. - Select input coupling GROUND. - Shift the Ch. A trace in the vertical mid of the screen.
	REQUIREMENTS	- Check that the Ch. A trace is exactly in parallel with the horizontal graticule lines. - If not correct this with the screwdriver control TRACE ROT. - Shift the Ch. A trace upwards and downwards and check if the deviation from the straight line does not exceed 0,1 div measured outside the central 8x10 div.
	MEASURING RESULTS	.....
	SETTINGS	- Press AUTO SET. - Apply a 2 kHz/1,6 V (pp) sine wave voltage to the Ch. A input socket. - Adjust the generator´s output voltage to 8 div vertical deflection. - Select vertical display of Ch. A and B. - Shift the Ch. A and Ch. B display in the vertical mid of the screen. - Select in the DISPLAY section A versus B display and switch register Ø on.
	REQUIREMENTS	- Check that a vertical line of 8 div is displayed. - Shift this line to the left and the right by means of X-POSITION and check if the deviation from the straight line does not exceed 0,1 div outside the central 8x10 div.
	MEASURING RESULTS	.....

	SETTINGS	- Shift the vertical line in the horizontal mid of the screen.
	REQUIREMENTS	- Check that the angle between the vertical graticule lines and the displayed line does not exceed 0,5 degree.
	MEASURING RESULTS	.....

C.	VERTICAL DEFLECTION	
C.1	SUBJECT	Input coupling Ch. A (B).
	TEST EQUIPMENT	LF sine wave generator.
	SETTINGS	- Apply a 1 kHz/120 mV (pp) to input socket A (B). - Press AUTO SET. - Select 50 ohm and DC input coupling. - Adjust AMPL/DIV to 20 mV/div for Ch. A (B) and the generator to an output voltage of 6 div. - Lower the generator frequency to 10 Hz. Vertical display must stay 6 div. - Select DC trigger coupling and adjust the LEVEL control for a triggered display. - Select 20 ms/div with the TIME/DIV control. - Select AC input coupling for Ch. A (B).
	REQUIREMENTS	- Check that the amplitude of the displayed signal is 4,3 div or higher.
	MEASURING RESULTS	.....
	SETTINGS	- Select GROUND input coupling for Ch. A (B).
	REQUIREMENTS	- Check that only a straight line is displayed.
	MEASURING RESULTS	.....

C.2 SUBJECT — Vertical deflection coefficients Ch. A (B).

TEST EQUIPMENT — Square wave calibration generator.

SETTINGS
- Apply a calibrated square wave signal of 1 kHz/20 mV (pp) to input Ch. A (B).
- Press AUTO SET.
- Select DC input coupling and 1 megaohm input impedance.
- Select 5 mV/div with the Ch. A (B) AMPL/DIV control.

REQUIREMENTS
- Check if the amplitude of the signal is 4 div (+or- 2%).

MEASURING RESULTS .....

4

SETTINGS AND REQUIREMENTS
- Increase the Ch. A (B) input signal according to the following table and check the accuracy of the displayed signal.

Input voltage (pp)	Y AMPL setting	Requirements	Measuring results
50 mV	10 mV	5 div.(+or- 2%)	.....
0,1 V	20 mV	5 div.(+or- 2%)	.....
0,2 V	50 mV	4 div.(+or- 2%)	.....
0,5 V	100 mV	5 div.(+or- 2%)	.....
1 V	200 mV	5 div.(+or- 2%)	.....
2 V	500 mV	4 div.(+or- 2%)	.....
5 V	1 V	5 div.(+or- 2%)	.....
10 V	2 V	5 div.(+or- 2%)	.....
20 V	5 V	4 div.(+or- 2%)	.....

SETTINGS
- Select 5 V/div input sensitivity for Ch. A (B).
- Turn the VARIABLE gain of Ch. A (B) into the UNCAL position towards an input sensitivity of 10 V/div.

REQUIREMENTS — Check that the accuracy of the vertical deflection is within +or- 15%.

MEASURING RESULTS .....

Put the VARIABLE gain back in the calibrated position.

C.3 SUBJECT — Input impedance and capacitance Ch. A (B).

TEST EQUIPMENT — Square wave calibration generator and 1 megaohm/14 pF dummy probe 2:1.

SETTINGS
- Apply a calibrated square wave signal of 1 kHz/50 mV (pp) to input Ch. A (B) via the dummy probe.
- Press AUTO SET.
- Select 5 mV/div with the Ch. A (B) AMPL/DIV control.
- Select DC input coupling and 1 megaohm input impedance.

REQUIREMENTS
- Check if the amplitude of the signal is 4 div (+or- 2%) and that it is free from overshoot or undershoot.

MEASURING RESULTS .....

SETTINGS AND REQUIREMENTS
- Increase the Ch. A (B) input signal according to the following table and check the signal accuracy and pulse response.

Input voltage(pp) via dummy probe	Y AMPL setting	Requirements	Measuring results
0,1 V	10 mV	5 div.(+or- 2%)	.....
0,2 V	20 mV	5 div.(+or- 2%)	.....
0,5 V	50 mV	5 div.(+or- 2%)	.....
1 V	100 mV	5 div.(+or- 2%)	.....
2 V	200 mV	5 div.(+or- 2%)	.....
5 V	500 V	5 div.(+or- 2%)	.....
10 V	1 V	5 div.(+or- 2%)	.....
20 V	2 V	5 div.(+or- 2%)	.....
50 V	5 V	5 div.(+or- 2%)	.....

C.4

SUBJECT	Protection of 50 ohm input impedance Ch. A(B).
TEST EQUIPMENT	LF square wave generator (source impedance 50 ohm).
SETTINGS	- Select 1 megaohm input impedance. - Apply a square wave signal of 1 kHz/6 V (pp) to the Ch. A (B) input. - Press AUTO SET. - Select 2 V/div with the Ch. A (B) AMPL/DIV control.
REQUIREMENTS	- Check if it is possible to switch Ch. A (B) from 1 megaohm to 50 ohm input impedance. This can be observed on the CRT because the signal amplitude halves and the softkey text "50ohm" becomes intensified.
MEASURING RESULTS	.....
SETTINGS	- Keep the instrument in 50 ohm position. - Increase the output signal from the generator to 15 V (pp) (into 50 ohm). - Check if the instrument switches automatically back to 1 megaohm input impedance. The softkey text "1Mohm" becomes intensified now and the displayed signal amplitude doubles.
MEASURING RESULTS	.....
SETTINGS	- Keep the instrument in 1 megaohm position. - Adjust the generator output voltage to 15 V (pp) (into 1 megaohm).
REQUIREMENTS	- Check that the Ch. A (B) input impedance cannot be switched to 50 ohm.
MEASURING RESULTS	.....

C.5	SUBJECT	Vertical dynamic range Ch. A (B).
	TEST EQUIPMENT	Constant amplitude sine wave generator.
	SETTINGS	- Apply a sine wave of 300 MHz/2 V (pp) to the Ch. A (B) input. Select 50 ohm input impedance for Ch. A (B). - Press AUTO SET. - Select 500 mV/div with the Ch. A (B) AMPL/DIV control. - Re-adjust the output signal of the generator so that 4 div are displayed. - Select 200 mV/div with the Ch. A (B) AMPL/DIV control.
	REQUIREMENTS	- Shift the displayed sine wave upwards and downwards and check that it is free from distortion.
	MEASURING RESULTS	.....

C.6	SUBJECT	Vertical bandwidth Ch. A (B) in 50 ohm and 1 megaohm positions.
	TEST EQUIPMENT	Constant amplitude sine wave generator.
	SETTINGS	- Apply a sine wave of 50 kHz/120 mV (pp) to the Ch. A (B) input. - Press AUTO SET. - Select 50 ohm input impedance (external termination resistor not necessary). - Select 20 mV/div with the Ch. A (B) AMPL/DIV control. - Re-adjust the output signal of the generator so that exactly 6 div are displayed.
	REQUIREMENTS	- Check that the displayed amplitude via Ch. A (B) is always 4,3 div or higher over the complete bandwidth range until 300 MHz. - Adjust -if necessary- the TIME/DIV knob for a well-defined sine wave.
	MEASURING RESULTS	.....

	TEST EQUIPMENT	Constant amplitude sine wave generator, 50 ohm termination resistor and adapter BNC/probe tip.
	SETTINGS	- Connect the termination resistor directly to the output socket of the sine wave generator. - Connect the 10:1 attenuator probe PM8929/09 to input A (B) of the oscilloscope. This probe must be correctly compensated according to the procedure given in chapter 8.1.1.4 in the operating manual. - Put the probe tip via the BNC/probe tip adapter in the 50 ohm termination at the generator. - Re-adjust the generator so that exactly 6 div are displayed at a frequency of 50 kHz.
	REQUIREMENTS	- Check that the displayed amplitude via Ch. A (B) is always 4,3 div or higher over the complete bandwidth range until 300 MHz. - Adjust -if necessary- the TIME/DIV knob for a well-defined sine wave.
	MEASURING RESULTS	.....
C.7	SUBJECT	Bandwidth limiter Ch. A (B).
	TEST EQUIPMENT	Constant amplitude sine wave generator.
	SETTINGS	- Apply a sine wave of 20 MHz/120 mV (pp) to the Ch. A (B) input. - Press AUTO SET. - Select 50 ohm input impedance. - Select 20 mV/div with the Ch. A (B) AMPL/DIV control. - Re-adjust the output signal of the generator so that exactly 6 div are displayed.
	REQUIREMENTS	- Switch the instrument´s bandwidth limiter on (via vertical MODE and softkey PROCESSING). - Check that the amplitude of the displayed signal is 4,3 div.
	MEASURING RESULTS	.....

C.8 SUBJECT

Pulse response Ch. A (B) in 50 ohm and 1 megaohm positions.

TEST EQUIPMENT

Square wave calibration generator.

SETTINGS

- Apply the fast-rise output of the generator to the Ch. A (B) input. Maximum output voltage must be selected and a frequency of 1 MHz.
- Press AUTO SET.
- Select 50 ohm and DC coupled input
- Select 200 mV/div with the Ch. A (B) AMPL/DIV control. Adjust the generator output voltage to a deflection of exactly 6 or 5 div.
- Put the signal exactly in the vertical mid of the screen.
- Select 5 ns/div with the TIME/DIV control.

REQUIREMENTS

- Check the pulse response during first 10 ns: the pulse abberations must not exceed +or- 6%. This means abberations of +or- 0,3 div (0,35 div) at an pulse amplitude of 5 div (6 div).
- For an accurate measurement it is necessary that the rise-time of the generator signal is 1 ns. Eventual pulse distortion from the generator must also be taken into account.

MEASURING RESULTS .....

TEST EQUIPMENT

Square wave calibration generator, 50 ohm termination resistor and adapter BNC/probe tip.

SETTINGS

- Connect the termination resistor directly to the fast-rise output of the generator.
- Connect the 10:1 attenuator probe PM8929/09 to input A (B) of the oscilloscope. This probe must be correctly compensated according to the procedure given in chapter 8.1.1.4 in the operating manual.
- Put the probe tip via the BNC/probe tip adapter in the 50 ohm termination at the generator.
- Select 200 mV/div with the Ch. A (B) AMPL/DIV control. Adjust the generator output voltage to a deflection of 6 or 5 div.
- Put the signal exactly in the vertical mid of the screen.
- Re-adjust the generator so that 5 or 6 div are displayed on the screen.

	REQUIREMENTS	Check the pulse response during the first 10 ns: the pulse abberations must not exceed +or- 6%. Other conditions identical to the check with 50 ohm input impedance.
	MEASURING RESULTS	.....

C.9	SUBJECT	Base line instability.
	TEST EQUIPMENT	BNC/banana adaptor PM9051 with interconnected outlets
	SETTINGS	- Press AUTO SET without input signals. - Select Ch. A and B for vertical display. - Position the A and B lines in the vertical mid of the screen. - Select function ADD.
	REQUIREMENTS	- Check that the line that should be in the vertical mid of the screen does not have a displacement of more that 0,3 div.
	MEASURING RESULTS	.....

	SETTINGS	- Select Ch. A and B for vertical display. - Position the Ch. A line 1 div. above the vertical mid of the graticule and the Ch. B line 1 div. under the vertical mid. - Select softkey function PROCESSING. - Switch softkey function MIN MAX repeatedly on and off.
	REQUIREMENTS	- Check that the Ch. A and B lines do not jump more than 0,5 div.
	MEASURING RESULTS	.....

SETTINGS	- Switch function MIN MAX off. - Switch up and down through the complete range of the Ch. A and B AMPL/DIV control. This happens if you keep the knob fixed in one position.
REQUIREMENTS	- Check that the Ch. A and B lines do not jump more than 0,15 div.
MEASURING RESULTS	.....

SETTINGS	- Switch the softkey functions A-INVERT and B-INVERT repeatedly on and off.
REQUIREMENTS	- Check that the Ch. A and B lines do not jump more than 0,3 div.
MEASURING RESULTS	.....

SETTINGS	- Switch the INVERT functions off. - Switch the Ch. A and B input couplings repeatedly between AC, DC and GROUND.
REQUIREMENTS	- Check that the Ch. A and B lines do not jump more than 0,1 div.
MEASURING RESULTS	.....

SETTINGS	- Ground the Ch. A (B) input externally by means of a BNC/banana adapter with interconnected outlets. - Select DC input coupling for Ch. A and B. - Turn the controls VARIABLE gain Ch. A and B repeatedly between their extreme positions.
REQUIREMENTS	- Check that the Ch. A and B line do not move more than 0,6 div.
SETTINGS	- Remove the BNC/banana adaptor. - Put the VARIABLE gain controls in their CAL position. - Shift the Ch. A and B line exactly in the vertical mid of the screen. - Switch the MAGNIFY function repeatedly between Yx1 and Yx5.

	REQUIREMENTS	- Check that the jump of the Ch. A and B line does not exceed 0,5 div.
	MEASURING RESULTS	.....

C.10	SUBJECT	Common mode rejection ratio.
	TEST EQUIPMENT	Constant amplitude sine wave generator, terminator 50 ohm and T-piece.
	SETTINGS	- Apply a 50 kHz sine wave of 1,6 V (pp) to input A and B via equal cables. The generator must be terminated with an external 50 ohm piece. Input impedance of oscilloscope channels is 1 megaohm. - Press AUTO SET. - Select 200 mV/div with the Ch. A and B AMPL/DIV controls. - Position both signals exactly in the vertical mid of the screen. - Select B-INVERT mode and ADD-mode. - Adjust either the VARIABLE gain control of Ch. A or B for minimal amplitude of the displayed signal.
	REQUIREMENTS	- Increase the generator´s frequency to 1 MHz (50 MHz). - Check that the amplitude of the displayed signal does not exceed 0,08 div (0,4 div).
	MEASURING RESULTS	.....

C.11	SUBJECT	Average function.
	TEST EQUIPMENT	Constant amplitude sine wave generator and LF sine wave generator.
	SETTINGS	- Select 50 ohm input impedance for Ch. A and B. - Apply a LF sine wave of 1 kHz/1,2 V (pp) to the Ch. A input. - Press AUTO SET. - Select 200 mV/div for Ch. A. - Select trigger COUPLING modes AC and HF reject. - Apply a HF sine wave of 100 MHz/0,2 V (pp) from the constant amplitude generator to the Ch. B input socket. - Ch. B input sensitivity must be 200 mV/div. - Select ADD mode for vertical display. The display now shows the 1 kHz/6 div sine wave with much noise superimposed.
	REQUIREMENTS	- Select via vertical mode and processing the average mode. Now you can select the AVERAGE value C between 2...64. The higher C is choosen, the cleaner the display becomes: the noise is eliminated. A high C value has the disadvantage that the correction action lasts longer.
	MEASURING RESULTS	.....

D. HORIZONTAL DEFLECTION

D.1	SUBJECT	Deflection coefficients time-base.
	TEST EQUIPMENT	Time marker generator.
	SETTINGS	- Press AUTO SET. - Select DC input coupling and 50 Ohm input impedance for Ch. A. - Select DC trigger coupling. - Apply the output signal of the time marker generator to input Ch. A. - Adjust the LEVEL control for a triggered display.
	REQUIREMENTS	- Check the deflection coefficient error according to the table below.

Time markers(pp) pulse frequency	Time-base setting .../div	Max. coefficient error	Measuring results
5 s	5 s	+or- 1%	.....
2 s	2 s	+or- 1%	.....
1 s	1 s	+or- 1%	.....
0,5 s	0,5 s	+or- 1%	.....
0,2 s	0,2 s	+or- 1%	.....
0,1 s	0,1 s	+or- 1%	.....
50 ms	50 ms	+or- 1%	.....
20 ms	20 ms	+or- 1%	.....
10 ms	10 ms	+or- 1%	.....
5 ms	5 ms	+or- 1%	.....
2 ms	2 ms	+or- 1%	.....
1 ms	1 ms	+or- 1%	.....
0,5 ms	0,5 ms	+or- 1%	.....
0,2 ms	0,2 ms	+or- 1%	.....
0,1 ms	0,1 ms	+or- 1%	.....
50 us	50 us	+or- 1%	.....
20 us	20 us	+or- 1%	.....
10 us	10 us	+or- 1%	.....
5 us	5 us	+or- 1%	.....
2 us	2 us	+or- 1%	.....
1 us	1 us	+or- 1%	.....
0,5 us	0,5 us	+or- 1%	.....
0,2 us	0,2 us	+or- 1%	.....
0,1 us	0,1 us	+or- 1%	.....
50 ns	50 ns	+or- 4%	.....
20 ns	20 ns	+or- 4%	.....
10 ns	10 ns	+or- 4%	.....
5 ns	5 ns	+or- 4%	.....

- Remove the input signal.

D.2 SUBJECT — Time-base line instability.

TEST EQUIPMENT — -

SETTINGS
- Press AUTO SET.
- Position the Ch. A base line in the vertical mid of the screen.
- Switch up and down through the complete range of the TIME/DIV switch. This happens if you keep the knob fixed in one position.

REQUIREMENTS
- Check that the vertical jump of the line does not exceed 0,6 div.

MEASURING RESULTS .....

D.3 SUBJECT — Trigger sensitivity via Ch. A (B).

TEST EQUIPMENT — Constant amplitude sine wave generators.

SETTINGS
- Apply a sine wave of 50 kHz/0,5 V (pp) to the Ch. A (B) input socket. Input impedance 50 ohm.
- Press AUTO SET.
- Increase the signal frequency to 30 MHz.
- Select 20 ns/div for the time-base.
- Decrease the signal amplitude to 0,5 div (pp) displayed on the screen.

REQUIREMENTS
- Check that the signal of 30 MHz/0,5 div (pp) is correctly triggered via Ch. A (B). The pilot lamp NOT TRIG´D must be off.

MEASURING RESULTS .....

SETTINGS
- Increase the signal frequency to 200 MHz.
- Select 5 ns/div for the time-base.
- Increase the signal amplitude to 1 div (pp).

REQUIREMENTS
- Check that the signal of 200 MHz/1 div (pp) is correctly triggered via Ch. A (B). The pilot lamp NOT TRIG´D must be off.

MEASURING RESULTS .....

SETTINGS
- Change the constant amplitude sine wave generator into the type that is able to deliver 300 MHz into Ch. A (B).
- Adjust the amplitude of the generator to 3 div (pp).

REQUIREMENTS
- Check that the signal of 300 MHz/3 div (pp) is correctly triggered via Ch. A (B). The pilot lamp NOT TRIG´D must be off.

MEASURING RESULTS .....

D.4 SUBJECT

Trigger sensitivity via EXT (EXT:10).

TEST EQUIPMENT

Constant sine wave generators, terminator 50 ohm and T-piece.

SETTINGS

- Apply a 50 kHz sine wave of 100 mV (pp) (1 V (pp)) to input Ch. A and EXT TRIG. The generator must be terminated with an external 50 ohm terminator. From this terminator, the signal is supplied to EXT TRIG and Ch. A via a T-piece and two equal coaxial cables.
- Select 1 megaohm input impedance for Ch. A.
- Press AUTO SET.
- Select 20 mV/div (200 mV/div) for Ch. A.
- Trigger the time-base on SOURCE EXT (EXT:10).
- Increase the signal frequency to 30 MHz.
- Select 20 ns/div for the time-base.
- Decrease the signal amplitude to 50 mV (pp) (500 mV (pp)). This can be monitored via Ch. A.

REQUIREMENTS

Check that the signal of 30 MHz/50 mV (pp) (500 mV (pp)) is correctly triggered via EXT (EXT:10).
The pilot lamp NOT TRIG´D must be off.

MEASURING RESULTS

.....

SETTINGS

- Increase the signal frequency to 200 MHz.
- Select 5 ns/div for the time-base.
- Increase the signal amplitude to 100 mV (pp) (1 V (pp)).

REQUIREMENTS

- Check that the signal of 200 MHz/100 mV (pp) (1 V (pp)) is correctly triggered via EXT (EXT:10).
  The pilot lamp NOT TRIG´D must be off.

MEASURING RESULTS

.....

	SETTINGS	- Change the constant amplitude sine wave generator into the type that is able to deliver a signal of 300 MHz/300 mV (pp) (3 V (pp)) into the EXT TRIG input. - Terminate the generator´s output signal with an external termination piece and apply it to the EXT TRIG input. - Adjust the generator´s output signal ot exactly 300 mV (pp) (3 V (pp)). - Select EXT (EXT:10) as a trigger source.
	REQUIREMENTS	- Check that the sine wave of 300 MHz/300 mV (pp) (3 V (pp)) triggers the time-base correctly. The pilot lamp NOT TRIG´D must be off then.
	MEASURING RESULTS	.....
D.5	SUBJECT	Level control range Ch. A (B).
	TEST EQUIPMENT	LF sine wave generator.
	SETTINGS	- Apply a sine wave of 50 kHz/1,6 V (pp) to Ch. A (B). - Select 50 ohm input impedance for Ch. A (B). - Press AUTO SET. - Select 200 mV/div with the Ch. A and B AMPL/DIV controls. - Adjust the generator output voltage to a vertical display of 8 div. - Select AC trigger coupling. - Select 100 mV/div with the Ch. A and B AMPL/DIV controls.
	REQUIREMENTS	- Shift the via Ch. A (B) displayed sine wave upwards and downwards and check that the range of the LEVEL control lies at least between top and bottom of the sine wave.
	MEASURING RESULTS	.....

D.6

SUBJECT	Level control range via EXT (EXT:10).
TEST EQUIPMENT	LF sine wave generator, terminator 50 ohm and T-piece.
SETTINGS	- Apply a 50 kHz sine wave of 1,6 V (pp) (16 V (pp)) to input Ch. A and EXT TRIG. The generator must be terminated with an external 50 ohm terminator. From this terminator the signal is supplied to EXT TRIG and Ch. A via a T-piece and two equal coaxial cables. - Select 1 megaohm input impedance for Ch. A. - Press AUTO SET. - Select 200 mV/div (2 V/div) for Ch. A. - Trigger the time-base on EXT (EXT:10). - Select AC trigger coupling. - Adjust the generator for a vertical display via Ch. A of exactly 8 div.
REQUIREMENTS	- Check that the range of the LEVEL control is at least between the top and bottom of the displayed sine wave.
MEASURING RESULTS	.....

D.7 SUBJECT — Bandwidth of trigger filters.

TEST EQUIPMENT — LF sine wave generator, terminator 50 ohm and T-piece.

SETTINGS
- Apply a 1 kHz sine wave of 50 mV (pp) to input Ch. A and EXT TRIG. The generator must be terminated with an external 50 ohm terminator. From this terminator the signal is supplied to EXT TRIG and Ch. A via a T-piece and two equal coaxial cables.
- Select 1 megaohm input impedance for Ch. A.
- Press AUTO SET.
- Select 20 mV/div and DC input coupling for Ch. A and check that 2,5 div signal are displayed. If necessary the generator output voltage must be re-adjusted.
- Select EXT as trigger source.
- Select AC and HF REJECT trigger coupling and adjust the LEVEL control for a well-triggered display.
- NOT TRIG´D lamp must be off.
- Increase the generator´s frequency to 100 kHz. Time-base in position 5 us/div.

REQUIREMENTS
- Check that there is no position of the LEVEL control that gives a triggered display.
- Increase the generator´s output voltage to 100 mV (+6 dB). This results in 5 div signal amplitude on the screen.
- Check that the LEVEL can be adjusted to a triggered display.

MEASURING RESULTS .....

SETTINGS
- Decrease the generators frequency to 5 Hz.
- Select 50 ms/div for the time-base.
- Decrease the generator´s output voltage to 50 mV (0 dB). This results in 2,5 div signal amplitude on the screen.
- Select AC trigger coupling.

REQUIREMENTS
- Check that there is no position of the LEVEL control that gives a triggered display.
- Increase the generator´s output voltage to 100 mV (+6 dB). This results in 5 div signal amplitude on the screen.
- Check that the LEVEL can be adjusted to a triggered display.

MEASURING RESULTS .....

D.8 SUBJECT — Horizontal expansion accuracy.

TEST EQUIPMENT — Time marker generator.

SETTINGS
- Apply a 100 us time marker signal to the Ch. A input socket.
- Press AUTO SET.
- Select 200 us/div for the time-base.
- Select a suitable input sensitivity with the Ch. A AMPL/DIV.
- Turn the X-EXPAND towards the UNCAL position 100 us/div.

REQUIREMENTS — Check for a display accuracy of + or - 5%.

MEASURING RESULTS .....

D.9 SUBJECT — Positioning range vertical and horizontal.

TEST EQUIPMENT — Constant amplitude sine wave generator.

SETTINGS
- Apply a 50 kHz/1,6 V (pp) sine wave to the Ch. A (B) input socket.
- Input impedance of Ch. A must be 50 ohm.
- Press AUTO SET.
- Select 200 mV/div input sensitivity for Ch. A (B).
- Adjust the generator output voltage to a vertical display of exactly 8 div.

REQUIREMENTS
- Turn the Ch. A (B) SHIFT clockwise and check that the sine wave does not cover the 5 div in the bottom half of the screen.
- Turn the Ch. A (B) SHIFT anti-clockwise and check that the sine wave does not cover the 5 div in the top half of the screen.

MEASURING RESULTS .....

SETTINGS
- Turn the Ch. A or B SHIFT so that the 8 div signal are exactly in the vertical mid of the screen.

REQUIREMENTS
- Turn the X-POSITION clockwise and check that the left 5 div of the screen are not covered by the signal.
- Turn the X-POSITION anti-clockwise and check that the right 5 div of the screen are not covered by the signal.

MEASURING RESULTS .....

E.	CURSORS	
E.1	SUBJECT	Voltage cursor accuracy.
	TEST EQUIPMENT	Square wave calibration generator.
	SETTINGS	- Apply a square wave voltage of 1 V (pp) to the Ch. A input. - Press AUTO SET. - Select 200 mV/div for Ch. A and AC input coupling. - Select 1 megaohm input impedance for Ch. A. - Press LOCK. - Press CURSOR. - Select cursors on REG A. - Position the 1st CURSOR in the horizontal mid of the top of the waveform. - Position the 2nd CURSOR in the horizontal mid of the bottom of the waveform.
	REQUIREMENTS	Check for a voltage cursor read-out of 1000 mV + or - 20 mV.
	MEASURING RESULTS	.....
E.2	SUBJECT	Time cursor accuracy.
	TEST EQUIPMENT	Time marker generator.
	SETTINGS	- Apply 1 ms time marker signal to the Ch. A input. - Press WRITE. - Press AUTO SET. - Select a suitable AMPL/DIV position for Ch. A. - Select 1 ms/div for the time-base. - Press LOCK. - Press CURSOR. - Select REG A. - Position the 1st CURSOR and the 2nd CURSOR so that they cover a distance of 8 time marker intervals.
	REQUIREMENTS	Check for a time cursor read-out of 8 ms + or - 0,0016 ms.
	MEASURING RESULTS	.....

F.	CALIBRATION VOLTAGE	
F.1	SUBJECT	Calibration voltage frequency accuracy.
	TEST EQUIPMENT	-
	SETTINGS	- Connect the CAL output voltage with the Ch. A input. - Press AUTO SET. - Press LOCK. - Press CURSOR. - Select cursors on REG A.
	REQUIREMENTS	Check by positioning of the cursors that the duration of one period of signal is 500 us (+or- 1,5 us). Check also the duration of both halves of a period are equal. This is important for the rms voltage measurement in section F.2.
	MEASURING RESULTS	.....
		- Select WRITE again.
F.2	SUBJECT	Calibration voltage accuracy.
	TEST EQUIPMENT	Digital multimeter and 50 ohm termination resistor.
	SETTINGS	Connect the multimeter (a.c. rms voltage range) between the instrument´s measuring earth and the CAL output socket and measure the rms value of the output voltage directly and with terminated (50 ohm) CAL output.
	REQUIREMENTS	Check for a voltage read out of 500 mV (+or- 5 mV) respectively of 250 mV (+or- 2,5 mV).
	MEASURING RESULTS	.....

G.	PLOT OUTPUT	
	SUBJECT	Accuracy of vertical and horizontal plot output voltages.
	TEST EQUIPMENT	Digital multimeter.
	SETTINGS	- Plug the plot cable into the DIN plot output socket at the rear side of the instrument. - Apply a the CAL signal to inputs A and B. - Press AUTO SET. - Position the two square wave signals in the vertical mid of the screen with SHIFT A and B. - Select 100 mV/div for channels A and B. - Select A versus B via the DISPLAY mode and switch on register RØ. - Select 200 ms/DT via the menus PLOT, SELECT and ANALOG. - Press SAVE/PLOT and then softkey ANALOG. The oscilloscope starts the plot action. This can be seen because the dot moves from left to right in the bottom of the screen.
	REQUIREMENTS	- Measure with the digital multimeter (d.c. voltage range) the maximum voltage at the vertical plot output (red banana plug, black is mass). This voltage must be 1000 mV + or - 30 mV. - Measure with the digital multimeter (d.c. voltage range) the maximum voltage at the horizontal plot output (blue banana plug, black is mass). This voltage must be 1000 mV + or - 30 mV.
	MEASURING RESULTS	.....

DISMANTLING THE INSTRUMENT

DISMANTLING THE INSTRUMENT

CONTENTS

5.0 Dismantling the instrument..... 5-1
5.1 General information..... 5-1
5.2 Removing the covers..... 5-1
5.3 Access to parts for the adjusting procedure..... 5-2

5.0 DISMANTLING THE INSTRUMENT

5.1 GENERAL INFORMATION

This section provides the dismantling procedures required for the removal of components during repair operations.
All circuit boards removed from the instrument must be adequately protected against damage, and all normal precautions regarding the use of tools must be observed.
During dismantling a careful note must be made of all disconnected leads so that they can be reconnected to their correct terminals during assembly.

CAUTION: Damage may result if:

- the instrument is switched on when a circuit board has been removed.
- a circuit board is removed within one minute after switching-off the instrument.

5.2 REMOVING THE COVERS

The instrument is protected by three covers: a front protection cover, a top cover and a bottom cover. To facilitate the removal of the instruments covers, first put the front protection cover in position.

Then proceed as follows:

- Hinge the carrying handle clear of the front protection cover.
- Stand the instrument on its protective front cover on a flat surface.
- Unscrew the screw marked E, which is placed in the center of the bottom cover (see figure 5.1).
- Unscrew the two screws A and B present in the left foot and the two screws C and D present in the right foot at the rear panel and remove these feet (see figure 5.1).
- The top cover and the bottom cover (without carrying handle) can be removed by shifting them backwards and lifting them of the instrument.

NOTE: When reinstalling the top and bottom covers again, take care that the wiring (coaxial cables and flat cables) is not damaged.
Re-installing the top and bottom covers has to be done in the reversed order as described above.

5.3 ACCESS TO PARTS FOR THE ADJUSTING PROCEDURE

After performing the actions which are described in section 5.2, all adjustment points are easily accessible.

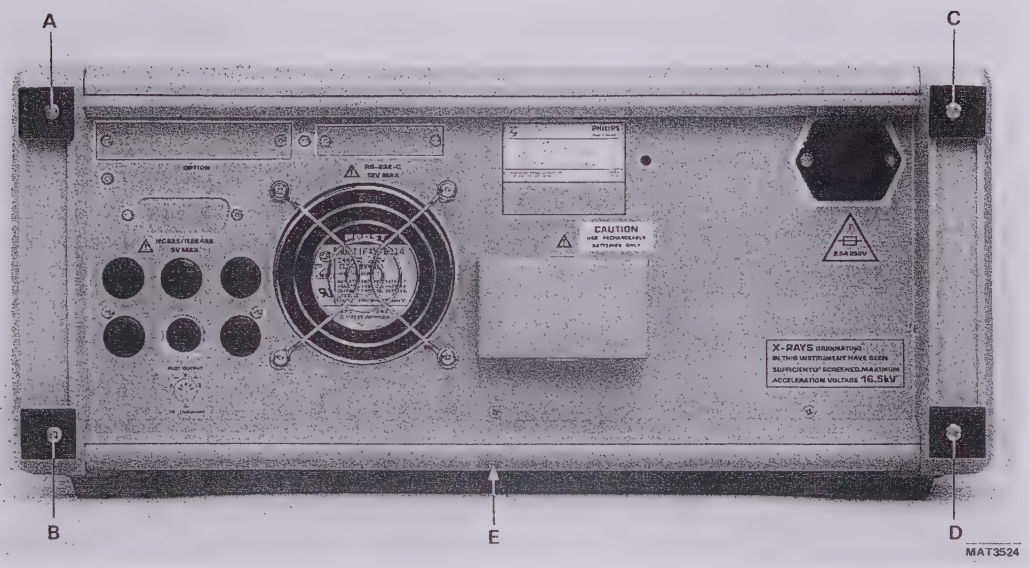


Figure 5.1 Removing the rear feet.

BLOCKDIAGRAM AND DESCRIPTION

BLOCK DIAGRAM AND DESCRIPTION

CONTENTS

6.0	Blockdiagram and description	6-1
6.1	Acquisition section	6-1
6.1.1	The vertical channels	6-1
6.1.2	The signal switches and peak detectors	6-3
6.1.3	The P^2CCD circuits and control logic	6-3
6.1.4	The ADC circuit	6-4
6.1.5	The trigger, trigger events and trigger delay circuits	6-5
6.1.6	The delta-t and digital time base circuits	6-5
6.1.7	The acquisition control logic	6-6
6.2	The calculation section	6-6
6.3	Display and plot section	6-7
6.3.1	The SAVE function	6-8
6.3.2	Trace display	6-8
6.3.3	Text display	6-9
6.3.4	Display control	6-10
6.3.5	Z-control	6-10
6.3.6	Plot-output	6-11
6.3.7	Option handling	6-11
6.3.8	Calibrator	6-11
6.4	Front section	6-11
6.5	Control section	6-12
6.6	Power supply section	6-13
6.7	The aquisition system	6-33
6.7.1	Introduction	6-33
6.7.2	Roll mode	6-33
6.7.3	Direct mode	6-33
6.7.4	P^2CCD mode	6-34
6.7.5	Random sampling mode	6-36
6.7.6	Miscellaneous	6-36
6.7.7	Survey of clock signals	6-40

6.0 BLOCKDIAGRAM AND DESCRIPTION

This chapter serves to explain the main functions of the oscilloscope. The system can be divided into a number of sections:

- Acquisition section
- Calculation section
- Display and plot section
- Front section
- Control section
- Power supply section

6.1 ACQUISITION SECTION

By means of the acquisition section the analog signals are sampled and converted into digital codes.
Before conversion the analog input signals must be adapted so that an Analog to Digital Converter (ADC) is able to convert them.

6.1.1 The vertical channels (units A27...A32, A35)

The vertical section consists of two identical channels A and B with a sensitivity range of 5 mV/div...5 V/div in a 1-2-5 sequence.
Each channel includes a probe indication and an input protection circuit.

HF and LF attenuator and EXT trigger unit (units A27, A28, A29 and A30)

Since channel A and B attenuator units are identical, only channel A is described. The input signal is applied to the vertical input socket. From here the signal is split up into two components; namely:

- The HF (high frequency) component applied to the CAPACITIVE ATTENUATORS block, which gives signal attenuation of x100, x10 or x1,
- The LF and DC (low frequency and direct current) components applied to the COMPARATOR block. The OFFSET control signal, which comes from the MANAGEMENT UNIT via the OFFSET ADAPTION UNIT, is applied to the FEEDBACK RESISTORS block together with an offset bias level from the OFFSET BIAS circuit. The output of the FEEDBACK RESISTORS block is then applied to the COMPARATOR for vertical OFFSET control. In the input of the COMPARATOR, a d.c. blocking capacitor is present for the AC-coupled mode. This capacitor is short-circuited by a switch contact in the DC-coupled mode.

The output signals from the CAPACITIVE ATTENUATORS and from the COMPARATOR are added and amplified by the SUMMATION STAGE AND OUTPUT AMPLIFIER. The output signal is routed to the VERTICAL SIGNAL UNIT. A part of the output signal is fed back via the FEEDBACK RESISTORS block to the input of the COMPARATOR where it is compared with the LF and DC components in the input signal. Various feedback resistors can be selected in the FEEDBACK RESISTORS block. This occurs simultaneously with the selection of the attenuation coefficients of the CAPACITIVE ATTENUATORS.
The input impedance of the attenuator unit can be changed from 1 MOhm to 50 Ohm if the 50 Ohm termination resistor is switched on. If the dissipation in this resistor is excessive, the TEMPERATURE SENSING CIRCUIT gives an alarm to the microprocessor system. This alarm is routed via the line that is also used for the probe indicator to the PROBE DET. AND 50 OHM PROT. ADC on the MANAGEMENT UNIT.

The EXT TRIG circuit operates in the same way as the channel attenuators A and B. However, there are only two attenuation steps. The LINE trigger signal (LNTR), applied to the FEEDBACK RESISTORS block comes from the POWER SUPPLY. The selected output signal is applied to the TRIGGER SOURCE SELECTOR block.

The EVENTS/EXT CLOCK input circuit is identical to the EXT TRIG input circuit, except the EVENT LEVEL signal coming from the MANAGEMENT UNIT which determines the level on which the trigger is passing through. The output signal is applied to the EVENTS AMPLIFIER on the VERTICAL SIGNAL unit.

Vertical signal unit (unit A32)

The output of the summation stage of the HF ATTENUATOR UNIT is fed to the VAR ATTENUATOR-circuit via the PRE-AMPLIFIER which determines the attenuator factors x1, x2 and x5. The VAR-circuit is controlled by the VAR DAC which on its turn is controlled by the VAR frontpanel control via the data bus and the VAR-SHIFT LATCHES on the MANAGEMENT unit to achieve continuous control of the signal amplitude. Via the NORMAL-INVERT circuit the signal is routed to the BANDWIDTH LIMITER AND SHIFT-circuit. The SHIFT is controlled by the SHIFT DAC via the data bus and the VAR-SHIFT LATCHES on the MANAGEMENT unit.

The channel A as well as the channel B output signals are applied to the CHANNEL SWITCH.
This switch can be switched for single channel A, single channel B, dual channel or add. In add the added signal is present on the channel A output.

The setting of the channels is realized via the microprocessor system and the MANAGEMENT unit. The microprocessor system is able to react on changes on the frontpanel or on selection of softkey functions by the operator of the instrument.

Management unit (unit A25)

The settings of the vertical channels A, B, EXT TRIG and EVENTS/ EXT CLOCK input and also the VERTICAL SIGNAL UNIT are controlled by the microprocessor system via the ATT. - VERTICAL SIGNAL AND TRIGGER LATCHES block on the MANAGEMENT UNIT.
On this unit the digital control codes from the microprocessor system are converted into analog values by the Digital to Analog Converters (DAC): TRIGGER LEVEL, OFFSET A (B), EVENT LEVEL.
The VAR-SHIFT DACs are driven, via the VAR-SHIFT LATCHES.
The analog 50 Ohm and probe detection signals are converted into a digital code by the PROBE DETECTION AND 50 OHM PROT. ADC circuit and can be read by the microprocessor system.
DATA and ADDRESS BUFFERS are also present on this unit to buffer the data and control signals for the DACs, ADCs and several latches.
A number of control signals is generated by the ADDRESS DECODER.

A SERIAL-PARALLEL CONVERTER circuit converts the serial data from the DELTA-t CIRCUIT on the clock unit into parallel data, which is applied to the microprocessor system when an IL$\emptyset$6--LT interrupt signal is generated.
Communication between the CCD logic and the microprocessor system is possible via an INPUT LATCH and an OUTPUT LATCH.

6.1.2 The signal switches and the peak detectors (unit A33)

The CHANNEL SWITCH output signals are each applied to a SIGNAL SWITCH which is controlled by an OUTPUT LATCH and by the ACQUISITION CONTROL LOGIC via the STATUS LOGIC.
Depending on the selection of the MIN / MAX softkey function, signals are fed through PEAK DETECTORS or not. Resetting of the PEAK DETECTORS is done in a rate which depends on the time base speed.

6.1.3 The P^2CCD circuits and control logic (unit A33 and A26)

Signals from the signal switches are passing P^2CCD circuits. These profiled peristaltic charged coupled devices acts as analog shiftregisters which are able to store signal samples with a rate which depends on the selected time base speed. This rate is generated by the FAST TIME BASE DIVIDER and via DRIVERS applied to the P^2CCD circuits. For time base speeds which can not be handled by the ADC anymore, the P^2CCD devices are used for time conversions. This means that signal samples can be taken by the P^2CCD circuits with a rate of up to 500 Mega-samples/second and later converted by an ADC circuit with a lower rate of 200 kHz per channel. This lower rhythm is generated by the SLOW CLOCK DIVIDER.
Each channel contains a P^2CCD device which contains two sections of 256 signal samples. So in each channel 512 signal samples can be present.

The output signals of the P^2CCDs are applied to fast CLAMP / INTEGRATE / HOLD circuits. These CIH circuits are able to hold the signal information for a time which is long enough for the TRACK AND HOLD circuit behind them to take them over.
The holded signal levels are applied to a P^2CCD CHANNEL SWITCH and to differential stages, whose outputs also are applied to the P^2CCD CHANNEL SWITCH. The P^2CCD CHANNEL SWITCH switches in a way which depends on the selected time base modes under the control of the P^2CCD OUTPUT LOGIC.
This logic also generates a start conversion signal for the ADC, which is also a clock signal for the SHIFT REGISTER in the ACQUISITION CONTROL LOGIC.
This switch places the output signal samples in serial and transportsthem to the TRACK AND HOLD circuit on unit A11.

The P^2CCD system is controlled by a CCD LOGIC which delivers control signals and which controls the FAST TIME BASE DIVIDER which produces the clock signals for the P^2CCD devices. The logic is controlled by trigger signals, and by the ACQUISITION CONTROL LOGIC. This ACQUISITION CONTROL LOGIC handles the timing in the different time base modes.
The CCD LOGIC also controls the PEAK DETECTOR RESET LOGIC which generates the reset pulses for the PEAK DETECTORS.

Aliasing (f sampling < 2x f trigger) is detected by an ALIASING DETECTOR of which the output signal is applied to the microprocessor system via an INPUT LATCH to control the frontpanel ALIASED lamp.

Auto triggering can be selected by the microprocessor system via the OUTPUT LATCH. The AUTO TRIGGER LOGIC receives the trigger pulses from the CCD LOGIC and produces an auto trigger for this CCD LOGIC when during a time of 100 ms no trigger signal appears. The NOT TRIG´D frontpanel lamp is controlled via the INPUT LATCH and the microprocessor system.

The TRIGGER DELAY COUNTER is a down counter of which the loading is effected by the microprocessor system with a value derived from the softkey settings in combination with he TIME/DIV switch setting. Upon the receipt of a trigger pulse from the CCD LOGIC the TRIGGER DELAY COUNTER starts counting time base output pulses until its zero state is reached.
This effects in a pulse which stops the sampling of new input signal samples by the P^2CCD devices. The P^2CCD contents can now be corrected, converted, stored in TRACE REGISTER RØ and displayed on the CRT screen.

6.1.4 The ADC circuit (unit A11)

The signal from the P^2CCD CHANNEL SWITCH is applied to a CORRECTION CIRCUIT, to correct some non-linearity of the P^2CCDs. The output signal is applied to a TRACK AND HOLD circuit which is able to hold the levels for a time long enough for the ADC circuit behind it to do the conversion to a 12-bit digital word. The ADC is able to perform conversion with a maximum speed of 400 kHz and is controlled by the ADC LOGIC. The 12-bit digital code is converted from straight binary into two´s complement by the CODE CONVERT circuit and then latched in the SAMPLE DATA LATCH for further data handling by the Digital Processing Unit (DPU).
The ADC output is also connected to an OVERFLOW DETECTION circuit, which on its turn is connected with the DPU.

6.1.5 The trigger, trigger events and trigger delay circuits (unit A26, A31 and A32)

A trigger signal can be derived via the TRIGGER SOURCE SELECTOR circuit from one of the sources channel A, channel B, the EXT TRIG input socket or the LINE frequency. The selected trigger signal is via softkey selectable TRIGGER FILTERS and a TRIGGER AMPLIFIER with trigger slope selection applied to an AUTO P-P LEVEL DETECTOR circuit where it is influenced by a signal derived from the frontpanel TRIGGER LEVEL control via the TRIGGER LEVEL DAC. It also delivers the DC level of the input signal to an AUTO OFFSET ADC, which converts this into a digital code for the microprocessor system, which is used for AUTO OFFSET.
The trigger signal is then applied to a TRIGGER AMPLIFIER + TV SYNC SEPARATOR where it can pass a tv. sync. separator, if selected. Next the TRIGGER LOGIC generates trigger pulses from the trigger signal. These trigger pulses go to the TRIGGER SYNC LOGIC on unit A49.

Signals from the EVENTS AMPLIFIER on the VERTICAL SIGNAL UNIT are applied to an EVENTS COUNTER which can be preset by a value which is generated by the microprocessor system depending on the number of events selected by the user.

The trigger signal from the TRIGGER LOGIC as well as the output signal from the EVENTS COUNTER are fed to the TRIGGER SYNC LOGIC.

6.1.6 The delta-t and digital time base circuits (units A26, A34, A48)

A DELTA-t CIRCUIT is introduced to measure the time between the moment of triggering and the real sample moment. This is needed to know for the different modes, on which memory location, converted digital codes have to be stored.
The DELTA-t CIRCUIT consists of a DIGITAL TO ANALOG CONVERTER, an INTEGRATOR and an ANALOG TO DIGITAL CONVERTER.
The input voltage for the INTEGRATOR is determined by themicroprocessor system and via the DAC applied to the INTEGRATOR.
The INTEGRATOR is started on a trigger from the TRIGGER SYNC LOGIC and is stopped when the first sample is taken. The output voltage of the INTEGRATOR, which is a measure for the time between the trigger pulse and the sample pulse, is converted via A SERIAL PARALLEL CONVERTER circuit into parallel data. These are applied to the microprocessor system via DATA BUFFERS after an ILØ6--LT interrupt signal is generated.

A 100 MHz OSCILLATOR and a 125 MHz OSCILLATOR, which are controlled by the microprocessor system applies a signal to the FREQUENCY DOUBLER on unit A48.
The output signal (FAST CLOCK) can be divided by the FAST TIME BASE DIVIDER by different factors. These factors depend on the selected time base speed. The dividers are set for a certain factor via the microprocessor system. The selected frequency depends on the selected time base position.

A SLOW CLOCK GENERATOR and a SLOW CLOCK DIVIDER generate a slow clock signal for the slow time base settings.

The ADDRESS DECODER and the CONTROL LATCH enable the microprocessor system to have control the over time base circuits.

6.1.7 The acquisition control logic (units A5 and A9)

The ACQUISITION CONTROL LOGIC controls the timing of the acquisition section in all the different time base modes.

The circuit is operating in a different way for each of the four time-base modes ROLL - DIRECT - P^2CCD and RANDOM SAMPLING.

The ACQUISITION CONTROL LOGIC is informed about the mode by the microprocessor system via the MODE REGISTER.
This MODE REGISTER also controls the SLOW TIME BASE LOGIC and the SHIFT LOGIC.
The SLOW TIME BASE LOGIC generates various control signals for the various time base settings in the ROLL and DIRECT modes.
The SHIFT LOGIC keeps track of wether samples that are taken are still in the P^2CCD or are leaving it and informs the DPU CONTROL via the STATUS MUX.

6.2 THE CALCULATION SECTION (units A8 and A9)

The calculation section consists of a Data Processing Unit (DPU unit A9) which is a very fast microcomputer system with a cycle time of 125 nsec.
It takes data from the ADC, performs calculations on it and sends the data to the TRACE DATA LATCH. All data is transported via the BUFFER.

The possible calculations are:

- digital MIN / MAX function in the ROLL and the DIRECT mode
- zero channel substraction in the P^2CCD mode
- averaging
- interpolation in the P^2CCD and the RANDOM SAMPLING mode
- overflow detection

To perform the calculations the DPU has a number of calculation registers and function blocks:

- REGISTER I, II and III
- SHIFT REGISTER
- +/- (complement function)
- ADDER
- LIMIT DETECTION

An overflow at the ADC is detected by the OVERFLOW DETECTION circuit, which enables the REFLECTION SUPPRESSION.

The DPU has registers in which data are stored. These are:

- PRE-TRIGGER RAM.
  This is used as a shift register and contains pre-trigger data in the DIRECT mode.
  It is also used as work space for the digital MIN / MAX calculations.
- AVERAGE RAM.
  Used for average calculations.
- FLAG RAM.
  In this ram is stored wether samples are real samples or samples obtained by interpolation. If an ovwerflow occurs, this is also stored by means of a flag. Flags are stored by means of the FLAG HANDLER.

The DPU is controlled by the DPU control (unit A8). The heart of the DPU control is the CONTROL MEMORY. This serves as a program memory for the DPU.
This memory is loaded for the various functions by the microprocessor system via the ADDRESS MULTIPLEXER and the BUFFER.
The DPU control has a PIPELINE REGISTER, which holds the current instruction, while the next instruction is fetched from the CONTROL MEMORY.
The instruction which is fetched depends on the address given by the ADDRESS MULTIPLEXER.
This address depends on data given by the STATUS MULTIPLEXER, which on its turn gets status signals from various function blocks.
The PIPELINE REGISTER is controlled by the START/STOP logic and the CONTROL LATCH.
When a DPU program is finished, the START/STOP LOGIC informs the microprocessor system about this via interrupt line ILØ2--LT.
The INSTRUCTION REGISTER and the CONTROL REGISTER, control theoperation of the DPU control.
The ADDRESS GENERATOR generates addresses for the PRE TRIGGER RAM, the AVERAGE RAM and the FLAG RAM.
The ADDRESS GENERATOR consists of an ADDRESS REGISTER and a PRETRIGGER COUNTER, which can be loaded via a buffer. The MULTIPLEXER selects the ADDRESS from the PRETRIGGER COUNTER or from the ADDER. The ADDER adds the addresses from the ADDRESS REGISTER and the OFFSET JUMP REGISTER. The latter enables the DPU to make jumps in program execution.
In the DIRECT MODE, the TRIGGER ADDRESS COMPARATOR generates a signal when all available pretrigger samples have been transported to the TRACE MEMORY.
The ADDRESS DECODER enables the microprocessor system to have control over the calculation section.

6.3 DISPLAY AND PLOT SECTION (units A1, A2, A3 and A4)

The display section consists of hardware to display trace data as well as text data on the C.R.T display.
A complete display cycle for all traces and all texts to be displayed, is realized in less than 20 ms. This results in a stable and flicker-free display.

Trace data words from the DPU system which have to be copied to the TRACE MEMORY in the display section are latched in the TRACE DATA LATCH with the rate of the DPU clock and the display section is for each new trace data word informed via the HANDSHAKE LOGIC (signal sample ready) that it is available for storage in REGISTER RØ of the TRACE MEMORY.
Addresses for the TRACE MEMORY are then generated by the COPY ADDRESS COUNTER. This counter which is directed to the TRACE MEMORY via ADDRESS MULTIPLEXER II starts each new copy cycle for a complete new trace with the generation of address zero. It counts then with the same rate as the DPU. After the storage of each trace data word in the TRACE MEMORY, a sample ready acknowledge signal is given to the DPU via the HANDSHAKE LOGIC.

6.3.1 The save function

When a SAVE function is selected, the contents of REGISTER RØ is copied in one or more of the REGISTERS R1, R2 or R3.
The trace data words are then first saved in the SAVE LATCH before they are saved in the selected REGISTER.
The REGISTER can be addressed then by the DISPLAY ADDRESS COUNTER via ADDRESS MULTIPLEXERS I AND II.

6.3.2 Trace display

X=t display mode

The trace data words to be displayed are transferred from the TRACE MEMORY via the DISPLAY CONTROL LATCH to an INVERT stage which offers the facility to invert the stored data before display. This facility can be softkey selected per register.
Data passes then a VERTICAL EXPAND stage of which the expand factor is set in combination with the gain factor of the Y AMPLIFIER later in the signal path. In this way, the Y/5, Y*1 and Y*5 vertical expand modes are realized.
The resulting data is latched in a LATCH and vertical position information, which is calculated by the microprocessor and applied via a VERTICAL POSITION LATCH, can be added by a VERTICAL POSITION ADDER stage. It is then converted from 2´s complement into straight binary by the CODE CONVERT circuit and latched in a YDAC LATCH before the conversion by the digital to analog converter YDAC. The converter output signal can then be deglitched by a SAMPLE AND HOLD circuit and influenced by a DOT JOIN/SMOOTH circuit. It is then amplified by a Y AMPLIFIER by a factor which depends on the selected vertical expand factor. The signal is then applied to a Y FINAL AMPLIFIER which directly drives the vertical deflection plates of the C.R.T.

Horizontal deflection signals are derived from the addresses for the TRACE MEMORY, which are generated by the DISPLAY ADDRESS COUNTER. These addresses are applied via the DISPLAY ADDRESS DATA BUFFFER to the HORIZONTAL EXPAND I CIRCUIT.
Horizontal expand factors of *1, *2, *4 and *8 can be realized. After expansion, horizontal position information, which is calculated by the microprocessor system and applied via a HORIZONTAL POSITION LATCH, can be added by a HORIZONTAL POSITION ADDER stage.
An additional expand factor of *1 or *8 can be realized in the HORIZONTAL EXPAND II circuit before the conversion by the digital to analog converter XDAC.
The converter output signal can then be deglitched by a SAMPLE AND HOLD circuit and influenced by a DOT JOIN/SMOOTH circuit. It is then amplified by an X AMPLIFIER of which the gain factor depends on the setting of the continuous X-EXPAND control on the frontpanel. This information is applied via an X-EXPAND LATCH and an X-EXPAND DAC to the X-AMPLIFIER.
The signal is then applied to an X FINAL AMPLIFIER which directly drives the horizontal deflection plates of the C.R.T.

A versus B display mode

This display mode is only selectable in dual channel mode.
The channel B TRACE MEMORY contents is applied to the vertical deflection plates of the CRT in a way as described for the X=t display.

For horizontal deflection the channel A TRACE MEMORY contents is used instead of the addresses from the DISPLAY ADDRESS COUNTER. The channel A trace data is converted from 2's complement into straight binary via the CODE CONVERT circuit and then transferred via the AVSB DATA BUFFER to the horizontal signal path and the horizontal deflection plates as described before for the X=t display addresses.

6.3.3 Text display

The text which has to be displayed, is generated by the microprocessor system and stored in the TEXT MEMORY.
Data is transferred from the microprocessor data bus via the DATA/TEXT BIDIRECTIONAL LATCH to the TEXT MEMORY.
Addresses from the microprocessor address bus are applied to the TEXT MEMORY via ADDRESS MULTIPLEXER I.

Each dot to be displayed on the C.R.T screen is stored in the TEXT MEMORY by a word consisting of a vertical and a horizontal coordinate and an intensity flag.

There are a number of different text blocks like:

Top area text	(TAT)
Trace area text	(TRAT)
Bottom area text	(BAT)
Softkey text	(SKT)
Miscellaneous text	(MSC)

The vertical coordinates are applied to the vertical deflection plates of the C.R.T. via a TEXT/TRACE BIDIRECTIONAL BUFFER and in a way as described for the X=t display.

The horizontal coordinates are applied via the LINE TEXT DATA BUFFER (for TAT, TRAT and BAT) or via the SOFTKEY TEXT DATA BUFFER (for SKT) or via the AVSB DATA BUFFER (for MSC) to the horizontal signal path and the horizontal deflection plates as described before for the X=t display addresses.

The intensity flag is used to inform the Z-stage about normal or intensified display.

6.3.4 Display control

Each display cycle, which consists of a fixed sequence of trace data blocks followed by a fixed sequence of text blocks, is controlled by the microprocessor system.
The microprocessor system places via a DATA BUFFER preset and control data into a number of OUTPUT PORTS, an Z + INTERRUPT TIMER and a PRESET REGISTER for the DISPLAY ADDRESS COUNTER, at the start of the display of each display data block.

At the same moment new position information is placed in the VERTICAL POSITION LATCH and in the HORIZONTAL POSITION LATCH.

At the end of each display block an interrupt signal ILØ5--LT is generated which is applied to the microprocessor system to ask for the actual preset and control data for the next display block.

6.3.5 Z-control (unit A1 and A15)

The Z-AMPLIFIER is controlled by the following circuits:

- Reflection detection circuit
- Overscan detection circuit
- Z detection circuit

Reflection detection

Reflection is caused by adding a position information to a signal information in the vertical as well as in the horizontal signal path which causes an overflow in the highest (non-existing) bits. Such an overflow causes the top of the signal being displayed at the bottom of the display like it is a reflection. In a similar way an underflow causes a reflection in the top of the display. Both situations can also occur in horizontal direction. These reflection can be detected by the REFLECTION DETECTION circuit and via the Z-DETECTION circuit suppressed by the Z-AMPLIFIER.

Overscan detection

Signals have to be displayed within the trace area of 8x10 divisions of the C.R.T. screen. Overscan in one of the four screen area directions is detected by the OVERSCAN DETECTION circuit and suppressed by the Z-AMPLIFIER.

Z-detection

Via the Z-DETECTION which is controlled by the Z-TIMER circuit the trace will be blanked when no traces or texts have to be displayed. The text can also be intensified if required. The last, for example, for active functions.
The Z-DETECTION output signal is applied to the Z-AMPLIFIER where it is influenced by the INTENSITY controls for the trace as well as for the text. The resulting signal is applied via the final Z-AMPLIFIER to the Wehnelt Cylinder of the CRT thus controlling the intensity of the trace on the screen. The focussing of the trace is controlled via the FOCUS block, under the influence of a FOCUS control by a signal which is applied to the focus grid of the CRT.

The a.c. and d.c. components of the output blanking signal from the Z-AMPLIFIER are guided along different paths.
The a.c. path runs straight to the FINAL Z-AMPLIFIER via a high voltage capacitor.
The d.c. component is modulated with 200 kHz by a MODULATOR, guided via a high voltage capacitor to the high voltage part and demodulated again by a DEMODULATOR. The resulting components are added and applied to the FINAL Z-AMPLIFIER and from there to the Wehnelt cylinder of the C.R.T.

6.3.6 Plot-output (unit A1)

Once per cycle of 20 ms a value can be plotted via the ANALOG PLOT INTERFACE. The X and Y informations are derived from the FINAL AMPLIFIERS and the penlift control is realized via the Z-AMPLIFIER stage.

6.3.7 Option handling

For OPTION handling the TRACE MEMORY as well as the TEXT MEMORY can be addressed via the microprocessor system address bus.

The data flows from the microprocessor system data bus to or from the TRACE MEMORY and the TEXT MEMORY is realized via the DATA/TEXT and TEXT/TRACE BIDIRECTIONAL latches.

6.3.8 Calibrator (unit A1)

A CALIBRATOR generator generates a 1 Vp-p 2 kHz calibration signal for the user which can be used to check the calibration of the system.

6.4 FRONT SECTION (units A13 and A14)

The front section contains a number of softswitches (the softkeys beside the CRT inclusive) and rotary controls (optical switches) of which the settings are read by the microprocessor system.

The softswitches are placed in a SOFT SWITCH MATRIX which places a row of switch settings in the FRONT SWITCH BUFFER each time that the matrix is addressed by the microprocessor system. The complete matrix is scanned every 40 ms.

The optical switches generate interrupt signals IL$\emptyset$3--LT for the microprocessor system when they are operated by the user and the microprocessor in turn addresses the circuit after which the information (from the ROTARY ENCODER) about the direction of rotation is placed on the data bus for interpretation by the microprocessor system.

The front section also contains a number of front panel leds which are controlled by the microprocessor system via LED DRIVERS.

The addresses which are generated by the microprocessor system, are decoded by a number of ADDRESS DECODERS.

6.5 CONTROL SECTION (units A5 and A6)

The control section consists mainly of a powerfull MICROPROCESSOR system configuration, with an 68000 uP, a RAM MEMORY for data and a ROM MEMORY containing the system software. The MICROPROCESSOR is running at a frequency of 8 MHz which is provided by a CLOCK GENERATOR which is driven by a 16 MHz OSCILLATOR.

An ADDRESS DECODER decodes a number of addresses resulting in a number of I/O SELECT signals for the various units and a number of MEMORY SELECT signals for the various memories via the I/O and MEMORY SELECT BUFFERS.

Interrupt signals from various units are applied to an INTERRUPT PRIORITY LEVEL DECODER. From here the interrupt with the highest priority is send to the MICROPROCESSOR.

A WATCHDOG circuit detects abnormal program sequences via an OUTPUT PORT and resets the MICROPROCESSOR via the RESET/HALT block in order to restart the program. This is done by a monostable flip flop.

A BUS ARBITER controls the system bus and can give the control over the bus to processors which are fitted on options, if they ask for bus control via their BUS REQUEST signals.

The battery voltage is compared with a reference voltage by a COMPARATOR. The battery status as well as the settings of the on board SERVICE switches are applied via an INPUT PORT to the microprocessor system.
A too low battery voltage results via a SUPPLY VOLTAGE SWITCH in the saving of the memory contents.

The following functions are performed by this control section:

- Front panel settings are read and processed.
- Front panel leds are controlled.
- Time base, trigger delay counter, events counter and acquisition control logic circuits are set in accordance to the user selected settings.
- Digital processing circuits are provided with a separate programm which depends on on the selected functions.
- The display system for trace, text and analog plot out data is controlled.
- If an option is installed, the complete handling is controlled.

6.7 THE ACQUISITION SYSTEM

6.7.1 Introduction

Below is a brief explanation of the principle of the acquisition system. See also figure 6.5.

It is assumed that:

- The oscilloscope is in recurrent mode (except roll mode)
- The oscilloscope is in single channel mode
- Average is off
- MIN/MAX is off
- Trigger delay by events is deselected

It is recommended to read this section together with the sections 8.5.3, 8.8.2 and 8.26.2.

6.7.2 Roll mode

After a new time base setting counter 3 in the slow time base logic (D1801 on unit A5) counts down the P^2CCD length, to enable the P^2CCD to be filled with good samples. Next ENSWTB goes high and the acquisition can start.
The P^2CCD takes continuously samples with a rate of 400 kHz, which appear 256 transport clocks later at the output, after which they are corrected (analog zero correction) and converted by the ADC. The DPU takes only a sample if it comes together with a TKSA pulse. The repetition rate of this pulse depends on the time base setting.
The samples are placed in the pretrigger ram of the DPU which contains the data for a full trace.
These data are shifted through when a sample is taken, to obtain the roll effect.
Each time the display section generates a SYDP, a full sweep of trace data are transported to the display ram in one stroke, to avoid discontinuities in the trace.

6.7.3 Direct mode

After a time base setting counter 3 in the slow time base logic (D1801 on unit A5) counts down the P^2CCD length, to enable the P^2CCD to be filled with good samples. Next ENSWTB goes high and the acquisition can start.
First the DPU loaded and started by the microprocessor. Next the DPU generates TRRY to the A.C.L., which on its turn generates TDLD--LT to load the trigger delay counter. Next HDOF goes low and the system waits for the first incoming trigger pulse.
At the arrival of a trigger pulse, the trigger delay counter starts counting down at the frequency of SYSWTB, which is determined by the time base setting.
The trigger delay counter generates TDUF when it has counted down to zero. If the trigger delay setting was zero divisions, the trigger delay counter was preset to zero.

TDUF causes the A.C.L. to generate DAVA 256 transport clocks later, which enable the samples to shift through the P^{2}CCD. The samples are corrected (analog zero correction) and converted by the ADC.
When DAVA is high, the DPU takes the samples only if they come together with a TKSA pulse.
The repetition rate of TKSA depends on the time base setting.
The samples are stored in the pretrigger ram.
Transport of samples to the display section happens asynchronously.
As soon as a sample is ready for transport to the display section and the trace data latch is released, the sample is placed in the trace data latch.
When a complete sweep of 4096 samples is processed in this way, an interrupt is generated to the microprocessor and the DPU stops. Next the microprocessor restarts the DPU, which on its turn generates TRRY, and so on.
When pretrigger is selected, TRRY is delayed which enables the DPU to take samples to get the desired pretrigger samples, which are stored in the pretrigger ram. After a trigger and DAVA as many samples are taken,that together with the available pretrigger samples, a full sweep of 4096 samples is made.

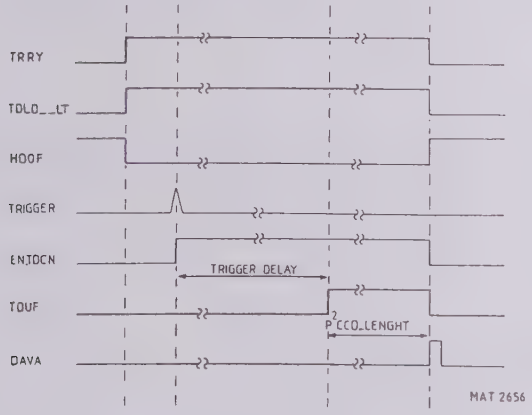


Figure 6.3 Basical timing diagram - Direct mode.

6.7.4 P^{2}CCD mode

In this mode the time conversion principle is used.
After a new time base setting, the P^{2}CCD starts taking samples, with a rate that is determined by the sample clock. The frequency of the latter depends on the time base setting, but is much higher than in the direct mode.
The DPU is loaded and started by the microprocessor. Meanwhile the P^{2}CCD is already filled with samples.
Next the DPU generates TRRY to the A.C.L., which on its turn generates TDLD--LT to load the trigger delay counter. Next HDOF goes low and the trigger delay counter waits for the first incoming trigger pulse.

The P^2CCD contains all pretrigger samples. At the arrival of a trigger pulse, the trigger delay counter starts counting down at the frequency of the sample clock, which is equal to the frequency of the transport clock. The trigger delay counter generates TDUF when it has counted down to zero. If the trigger delay setting was zero divisions, the trigger delay counter was preset to 512, which is equal to the P^2CCD length. In case of a pretrigger selection of 10 divisions, the trigger delay counter is preset to zero.
As TDUF is generated, the P^2CCD contains all samples for the complete sweep, so the taking of samples is stopped. TDUF also causes the CCD logic to change the transport clock frequency to 100 kHz and to make CDRD high.
Also DAVA goes high and the DPU takes all uncorrected and converted samples from the ADC and places them in the pretrigger ram.
When this is done, the A.C.L. generates RSSW and ZECH, which presets the trigger delay counter again. Next the P^2CCD reads zero voltage samples with the fast sampling clock, determined by the time base setting. As TDUF is generated the A.C.L. generates STSW, which causes the CCD logic to make CDRD high. Now 512 zero voltage samples are taken by the DPU and substracted from the corresponding samples in the pretrigger ram (digital leakage correction). Next the DPU calculates all interpolated samples. When the whole sweep is ready, the trace data are transported in one stroke to the display section, thereby ignoring the SYDP signal.
At last an interrupt is generated to the microprocessor and the DPU stops. Next the microprocessor restarts the DPU; which on its turn generates TRRY and so on.

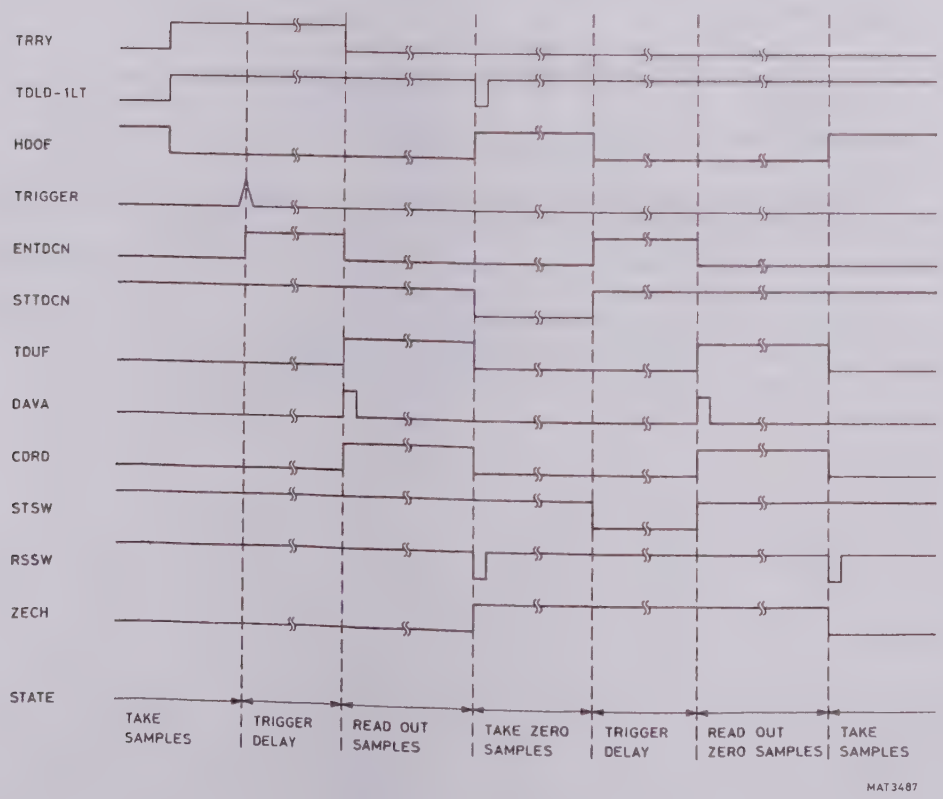


Figure 6.4 Basical timing diagram - P^2CCD mode.

6.7.5 Random sampling mode

The random sampling mode operates roughly in the same way as the P^2CCD mode.

The main differences are:

- The sampling frequency is independent of the time base setting (50 MHz).
- The number of samples that is read in every stroke depends on the time base setting.
- The trigger delay counter is preset in such a way that the samples used at every read out stroke are almost at the output of the P^2CCD as TDUF is generated.

The time that passes by to let the samples shift to the output is used to inform the DPU about the result of the delta-t measurement (the time difference between the trigger pulse and the first sample pulse). The DPU uses this to place the samples in the correct locations in the pretrigger ram.
When the zero voltage samples are processed, a new sweep of samples with probably a different delta-t result is done and so on.
Once in every display cycle (20 ms) SYDP goes high.
Then the DPU calculates interpolated samples and transports the trace data, which is probably not a complete sweep, in one stroke to the display section.
In this way as many as possible sweeps can be done, for the fastest time base setting only 2 or 3 samples are taken every sweep.

When a transport of trace data to the display section is finished, an interrupt is generated to the microprocessor and the DPU stops. As in the other modes, the microprocessor restarts the DPU to start the whole cycle again.

6.7.6 Miscellaneous

- The special modes are combinations of the direct mode and the P^2CCD mode.
- Maximum resolution mode is a combination of P^2CCD mode and random sampling mode.
- In single scan mode the microprocessor checks the sample flags in the display ram to determine if a scan is complete.
- In dual channel mode, the signal CHPT (channel pointer) informs the DPU from which channel the samples are.
- In MIN/MAX mode the signal MMPT informs the DPU if the samples come from the min or from the max peak detector.
- The average function is completely performed in the DPU.

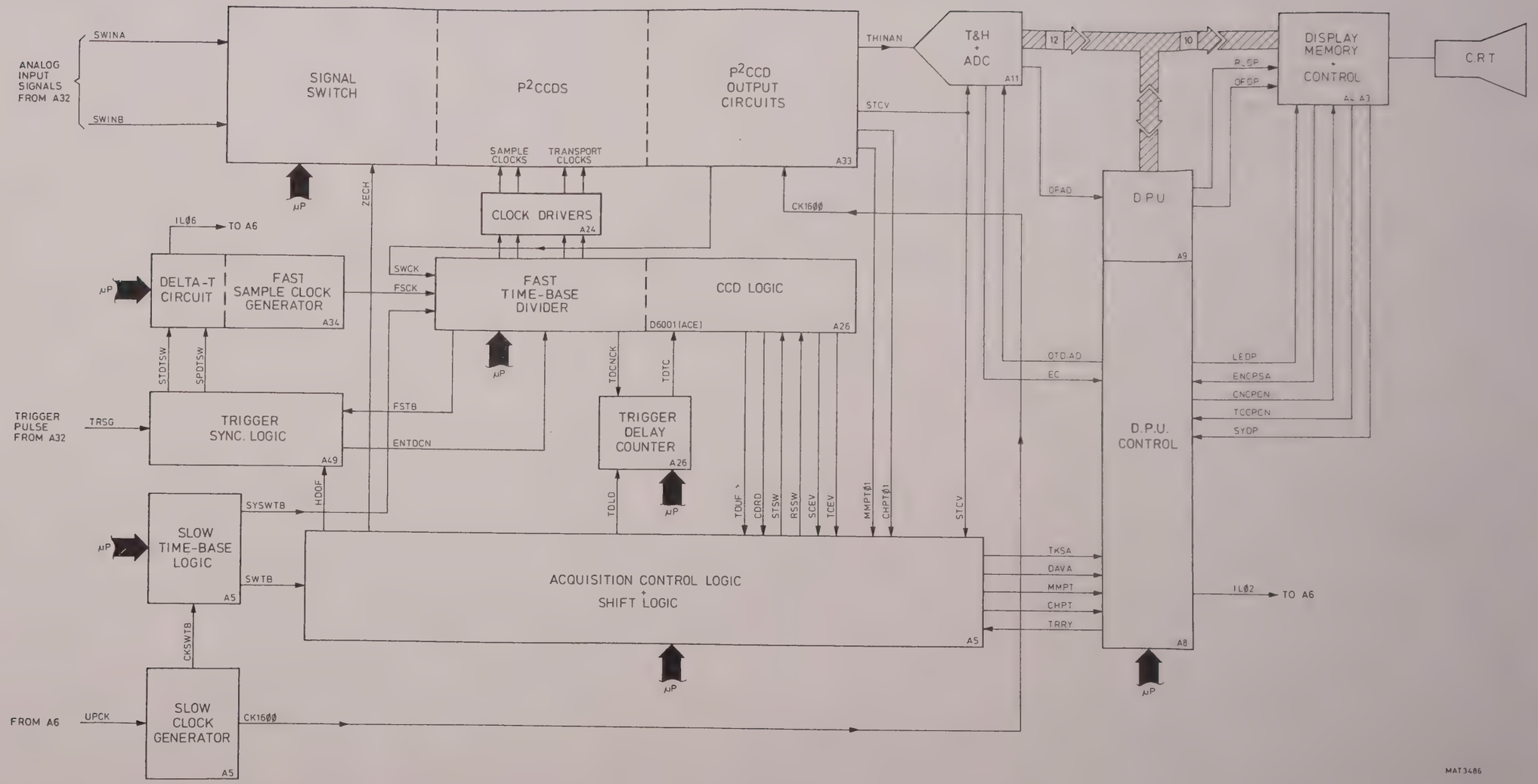


Figure 6.5 Blockdiagram of the acquisition system.

6.7.7 Survey of clock signals.

Mode	Time-base range	Sample clock	Transport clock	Slow time-base
Roll Single Normal	360 s/div : 50 ms/div	400 kHz : 400 kHz	400 kHz : 400 kHz	1,111 Hz : 8 kHz
Roll Dual Normal	360 s/div : 50 ms/div	200 kHz : 200 kHz	400 kHz : 400 kHz	0,555 Hz : 4 kHz
Roll Single Min/max	360 s/div : 50 ms/div	200 kHz : 200 kHz	400 kHz : 400 kHz	1,111 Hz : 8 kHz
Roll Dual Min/max	360 s/div : 50 ms/div	200 kHz : 200 kHz	400 kHz : 400 kHz	0,555 Hz : 4 kHz
Direct Single Normal	5 s/div : 1 ms/div	400 kHz : 400 kHz	400 kHz : 400 kHz	80 Hz : 400 kHz
Dir. Sp Single Normal	0,5 ms/div	400 kHz	400 kHz	100 kHz
Direct Dual Normal	5 s/div : 1 ms/div	200 kHz : 200 kHz	400 kHz : 400 kHz	40 Hz : 200 kHz
Dir. Sp Dual Normal	0,5 ms/div	200 kHz	400 kHz	100 kHz
Direct Single Min/max	5 s/div : 2 ms/div	200 kHz : 200 kHz	400 kHz : 400 kHz	80 Hz : 200 kHz
Dir. Sp. Single Min/max	1 ms/div 0,5 ms/div	200 kHz 200 kHz	400 kHz 400 kHz	400 kHz 100 kHz
Direct Dual Min/max	5 s/div : 2 ms/div	200 kHz : 200 kHz	400 kHz : 400 kHz	40 Hz : 100 kHz
Dir. Sp. Dual Min/max	1 ms/div 0,5 ms/div	200 kHz 200 kHz	400 kHz 400 kHz	200 kHz 100 kHz

Mode	Time-base range	Sample clock	Fast transport clock	Slow Transport clock
P2CCD	200 us/div	125 kHz	125 kHz	100 kHz
Single/	:	:	:	:
Dual	:	:	:	:
Normal	100 ns/div	250 MHz	250 MHz	100 kHz

P2CCD	200 us/div	125 kHz	125 kHz	100 kHz
Single/	:	:	:	:
Dual	:	:	:	:
Min/max	5 us/div	5 MHz	5 MHz	100 kHz

Random	50 ns/div	50 MHz	100 MHz	400 kHz
sampling	:	:	:	:
Single/	:	:	:	:
Dual	:	:	:	:
Normal	5 ns/div	50 MHz	100 MHz	400 kHz

Name	Signal name(s)	Unit(s)
Sample clock	SCODA, SCEVA, SCODB, SCEVB	A24, A26, A33
Transport clock	TCODA, TCEVA, TCODB, TCEVB	A24, A26, A33
	TCOD1A, TCOD2A, TCEV1A, TCEV2A	
	TCOD1B, TCOD2B, TCEV1B, TCEV2B	
	TCODDA, TCEVDA, TCODDB, TCEVDB	
Slow time-base	SWTB, SYSWTB	A5

INTRODUCTION TO CIRCUIT DESCRIPTIONS 7

INTRODUCTION TO CIRCUIT DESCRIPTIONS

CONTENTS

7.0 Introduction to circuit descriptions..... 7-1
7.1 General..... 7-1
7.2 Explanation of signal name set up..... 7-1
7.2.1 Signal names..... 7-1
7.2.2 Signal name list..... 7-2

7.0 INTRODUCTION TO CIRCUIT DESCRIPTIONS

7.1 GENERAL

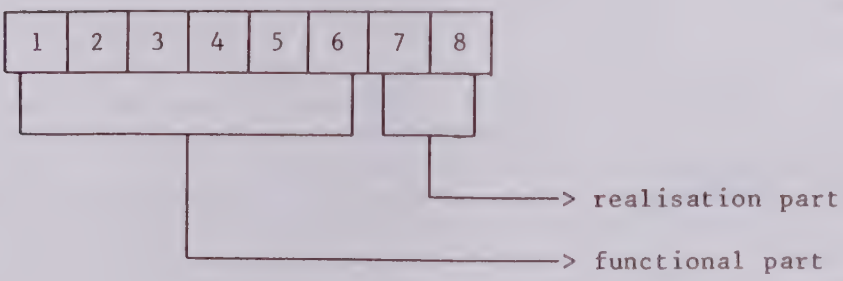
The functioning of the circuits is explained in chapter 8.0 "CIRCUIT DESCRIPTION" per unit in the sequence of the unit numbers (A ..). Every unit section contains the circuit description, the lay-out of the p.c.b., the circuit diagram(s) and a signal-name list, indicating the signal sources and signal flow.

7.2 EXPLANATION OF SIGNAL NAME SET UP

7.2.1 Signal names

Signal names consists of 2 parts:

- a functional part of maximal 6 characters
- a realisation part of 2 characters



The realisation part is optional. If it is used then the functional parts should consist of 6 characters. If necessary dummy's (minus signs) are used in the functional part, to make it 6 characters long.

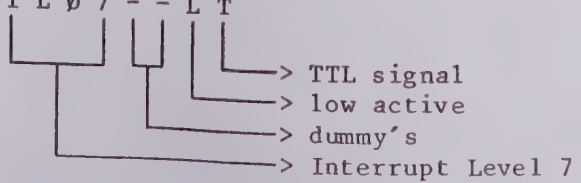
The first character of the realisation part has the following meaning:

H: active high signal
L: active low signal
X: irrelevant (e.g. counter outputs)

The second character of the realisation part is used to identify signal levels:

A: analogue
E: ECL -4,5V or -5,2V
T: TTL 5V or HCT
X: other levels

Example: I L Ø 7 - - L T



Sometimes the functional part can also be used for a serial number e.g. to indicate a buffered version of a signal.

Example: CHPT--Ø1

7.2.2 Signal name list

Each unit description in chapter 8.0 "CIRCUIT DESCRIPTIONS" contains a list with the signal names used in that unit given in alphabetical order.
Behind each name, a description is given and is mentioned on which unit the signal is generated.
Only if the signal is generated on the unit itself, the other units on which the signal is used (signal destination(s)) are mentioned, otherwise a minus sign is filled in.
If the signal flows over more units in sequence, the path is indicated.

Example: The battery voltage (BAVO) comes from unit A66 via A20, A19 and A12 to A6. On unit A66 is indicated: A20-A19-A12-A6.

Some signals may have more signal sources, because the sources have open collector output circuits, or 3-state output circuits.
In this case the sources are mentioned, separated with a plus (+) sign.
As signal source is always indicated, the unit where the signal is generated.

Example: On units A20, A19, A12 and A6, unit A66 is indicated as source.

A number of power supply lines and ground lines, which are generated on POWER 1 unit A19, are not mentioned on the signal name lists because they appear in almost every unit.
These signal names can be found on the signal name list of POWER 1 unit A19 itself, and are in the destination column indicated with "general".
Power supply lines, which are derived from the power supply lines mentioned above, are also not mentioned in the list.

The destinations of the data-bus and address-bus lines from the microprocessor system on MICROPROCESSOR unit A6 are also indicated with "general", because almost all units are involved. This is also done for the signals UPRD--LT (microprocessor read) and UPWR--LT (microprocessor write).

CIRCUIT DESCRIPTIONS 8

CIRCUIT DESCRIPTIONS

CONTENTS

8.0		CIRCUIT DESCRIPTION	8.0-1
8.1	A1	FINAL AMPLIFIER	8.1-1
8.2	A2	DISPLAY DAC	8.2-1
8.3	A3	DISPLAY CONTROL	8.3-1
8.4	A4	DISPLAY MEMORY	8.4-1
8.5	A5	MRAM	8.5-1
8.6	A6	uP BOARD	8.6-1
8.7	A7	OPTION 1	8.7-1
8.8	A8	DPU CONTROL	8.8-1
8.9	A9	DPU	8.9-1
8.10	A10	OPTION 2	8.10-1
8.11	A11	ADC + T&H	8.11-1
8.12	A12	MOTHER BOARD	8.12-1
8.13	A13	FRONT 1	8.13-1
8.14	A14	FRONT 2	8.14-1
8.15	A15	Z-AMPLIFIER	8.15-1
8.16	A16	CRT CONTROL	8.16-1
8.17	A17	SOFTKEY UNIT	8.17-1
8.18	A18	SMOOTH + DOTS	8.18-1
8.19	A19	POWER 1	8.19-1
8.20	A20	POWER 2	8.20-1
8.24	A24	DRIVER UNIT	8.24-1
8.25	A25	MANAGEMENT UNIT	8.25-1
8.26	A26	CCD LOGIC	8.26-1
8.27	A27	HF-UNIT OF ATTENUATOR A	8.27-1
8.28	A28	LF-UNIT OF ATTENUATOR A	8.28-1
8.29	A29	HF-UNIT OF ATTENUATOR B	8.29-1
8.30	A30	LF-UNIT OF ATTENUATOR B	8.30-1
8.31	A31	EXTERNAL TRIGGER UNIT	8.31-1
8.32	A32	VERTICAL SIGNAL UNIT	8.32-1
8.33	A33	P^2CCD UNIT	8.33-1
8.34	A34	CLOCK UNIT	8.34-1
8.35	A35	ATTENUATOR ADAPTION UNIT	8.35-1
8.38	A38	MINI TRIGGER SELECT A	8.38-1
8.39	A39	MINI TRIGGER SELECT B	8.39-1
8.40	A40	MINI TRIGGER FILTER	8.40-1
8.41	A41	MINI TRIGGER AMPLIFIER	8.41-1
8.42	A42	MINI TRIGGER LOGIC	8.42-1
8.43	A43	MINI EVENTS AMPLIFIER	8.43-1
8.44	A44	MINI VERTICAL AMPL. PROC. UNIT	8.44-1
8.48	A48	MINI FREQUENCY DOUBLER	8.48-1
8.49	A49	MINI CCD LOGIC	8.49-1
8.50	A50	OFFSET ADAPTION UNIT	8.50-1
8.66	A66	REAR MODULE	8.66-1

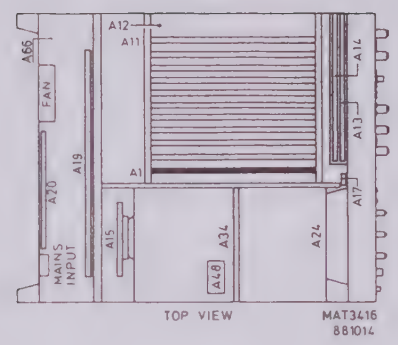
8.0 CIRCUIT DESCRIPTIONS

The functioning of the circuit is explained in this chapter. It is done per unit and in unitnumber (A..) sequence.

Every unit section contains a circuit description, the lay-out of the p.c.b., the circuit diagram(s) and a signal-name list.

See also chapter 7.0 "INTRODUCTION TO CIRCUIT DESCRIPTIONS".

UNIT A1 - FINAL AMPLIFIER UNIT



CONTENTS

8.1.1	General information	8.1-1
8.1.2	Vertical final amplifier	8.1-2
8.1.3	Horizontal final amplifier	8.1-3
8.1.4	Trace/Text intensity	8.1-3
8.1.5	Overscan detection	8.1-4
8.1.6	Z-amplifier	8.1-5
8.1.7	Calibrator	8.1-6
8.1.8	Plot interface	8.1-6
8.1.9	Signal-name list	8.1-7

8.1.1 General information

This unit basically comprises the vertical and horizontal final amplifiers, the overscan detection circuit, the Z-amplifier, the calibrator circuit and the analog plot interface.

8.1.2 Vertical final amplifier

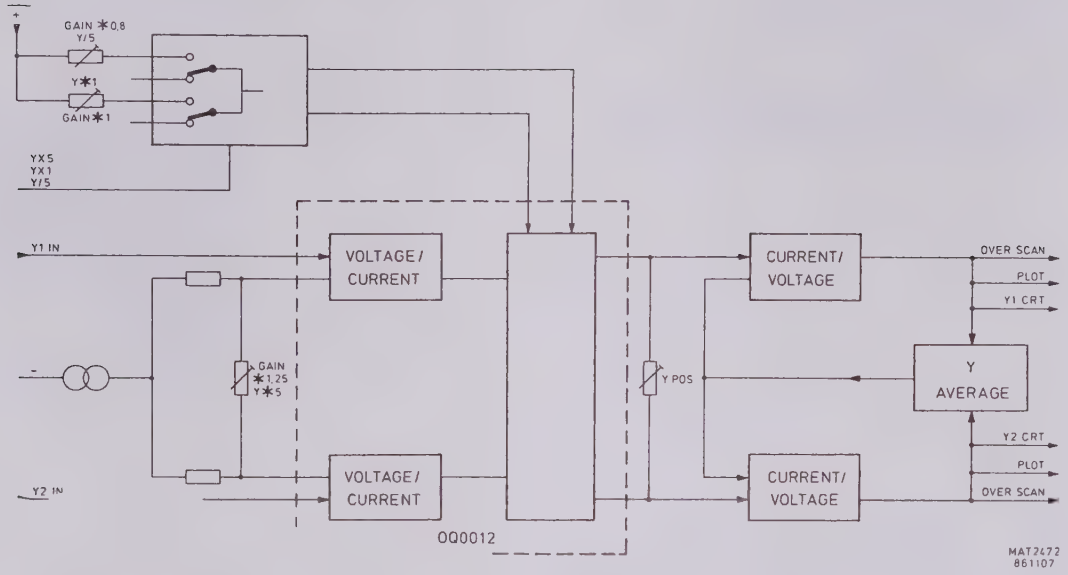


Figure 8.1.1 Blockdiagram Y-final amplifier.

The output signals Y1IN and Y2IN from the DISPLAY DAC UNIT A2 are applied to a voltage/current converter of which the x1,25 (Y*5-mode) gain can be adjusted by potentiometer R2531 in the emitter circuit of the input transistor of D2507.
Furthermore, the gain can be influenced for the Y*1 and the Y/5 mode.
Two sections of multiplexer D2501 can be switched by the signals ANEPY-HT (analog expand) and ANCPY-HT (analog compress) from DISPLAY CONTROL UNIT A3.
The switching is done according the following table:

MODE	ANCPY-HT	ANEPY-HT	analog expand factor (UNIT A1)	digital expand factor (UNIT A2)
Y/5	1	Ø	x0,8	/4
Y*1	Ø	Ø	x1	x1
Y*5	Ø	1	x1,25	x4

An additional circuit can be switched in for the x1 gain (adjustable with potentiometer R2513) and and additional circuit can be switched in for the x0,8 gain (adjustable with potentiometer R2516).
The selection depends on the user selection of the Y*5, Y*1 or the Y/5 mode.

Output points 12/13 and 14/15 of the MULTIPLIER D2506 are applied to current/voltage converters in the Y-OUTPUT stage of which the balance can be adjusted by potentiometer R2533.

The average value of the signals Y1 and Y2 is fed back to the input of the X-OUTPUT stage to keep the average value constant.

The signals X1 and X2 are applied to the vertical deflection plates of the C.R.T., to the OVERSCAN DETECTION circuit on unit A1 and also to the PLOT INTERFACE on this unit A1.

8.1.3 Horizontal final amplifier

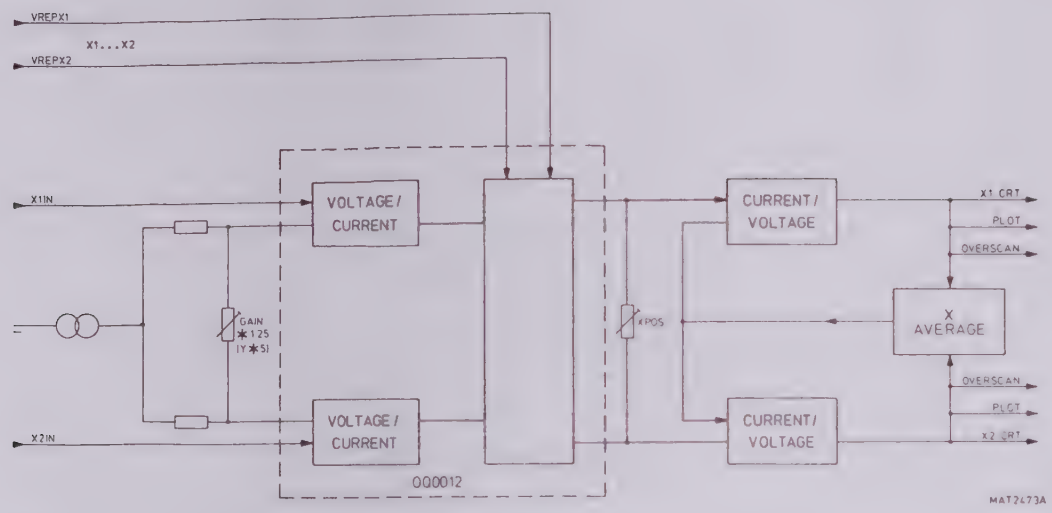


Figure 8.1.2 Blockdiagram X-final amplifier.

The output signals X1IN and X2IN from the DISPLAY DAC UNIT A2 are applied to a voltage/current converter of which the x1 gain can be adjusted by potentiometer R2566 in the emitter circuit of the input transistors of D2507.

Furthermore, the gain can be influenced by signals VREPX1 and VREPX2 which carry a variable X-EXPAND factor between x1/2 (EXPAND x1) and x1 (EXPAND x2). This factor, which is user selected, is multiplied in the stage D2507 to vary the X-gain.

Output points 12/13 and 14/15 of the MULTIPLIER D2507 are applied to current/voltage converters in the X-OUTPUT stage of which the balance can be adjusted by potentiometer R2571.

The average value of the signals X1 and X2 is fed back to the input of the X-OUTPUT stage to keep the average value constant.

The signals X1 and X2 are applied to the horizontal deflection plates of the C.R.T., to the OVERSCAN DETECTION circuit on unit A1 and also to the PLOT INTERFACE on this unit A1.

8.1.4 Trace/Text intensity

The levels ITTR from the TRACE INTENS frontpanel control and ITTX from the TEXT INTENS frontpanel control on C.R.T. CONTROL UNIT A16, are applied to one section of multiplexer D2501. This section, which is switched by the signal DPTR--HT (display trace), switches the trace intensity level to the Z-amplifier when traces have to be displayed and the text intensity level when texts have to be displayed.

8.1.5 Overscan detection

The output signals Y1, Y2, X1 and X2 from the vertical and horizontal final amplifiers are applied to an overscan detection circuit where they are compared with four overscan levels for the top, bottom, left and right sides of the trace area on the C.R.T. screen.

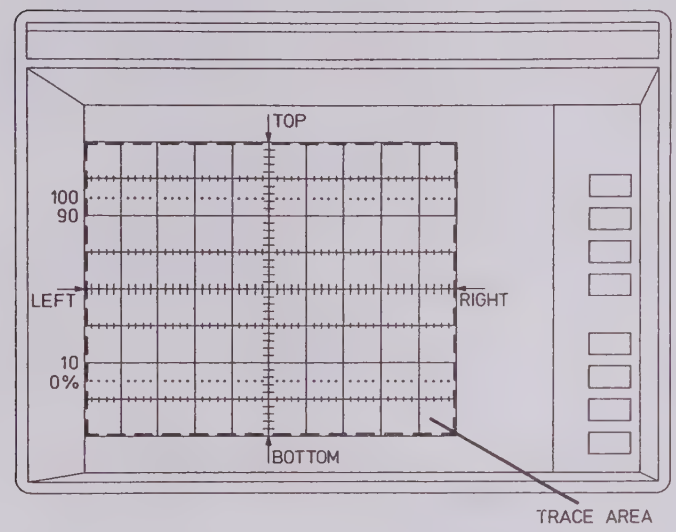


Figure 8.1.3 Overscan detection.

These levels can be adjusted by potentiometers R2658, R2659, R2678 and R2682 in such a way that during the display of traces, the traces can never be displayed outside the trace area on the C.R.T. screen.
In case of overscan a blanking signal is produced by the collector of transistor V2623 and this signal is applied to the Z-amplifier to blank the trace.
The overscan detection circuit can be disabled during text display and enabled during trace display by the signal DIOS--HT (disable overscan) via transistor V2611.

8.1.6 Z-amplifier

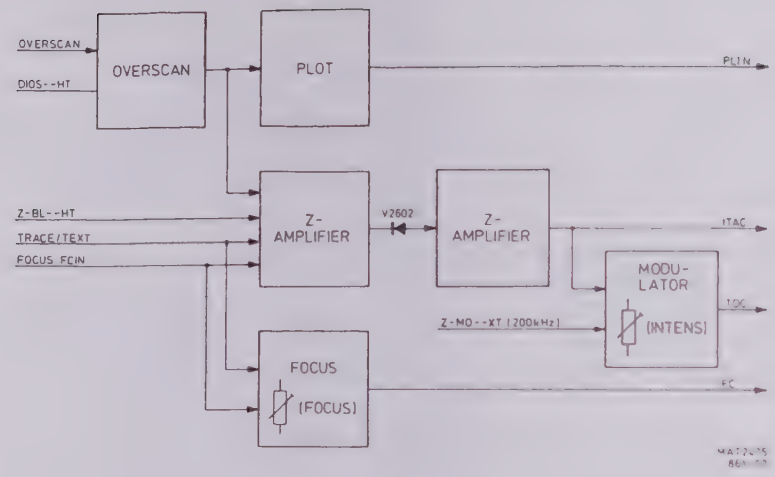


Figure 8.1.4 Blockdiagram Z-circuit.

INTENS

The Z-circuit is controlled by a number of different inputs:

- Overscan
- Z-blank signal
- TRACE or TEXT intensity control level
- FOCUS control level

The signals are applied to a Z-amplifier and the output of this amplifier is guided along two different signal path's. A high frequency component signal path (signal ITAC) and a low frequency component signal path (signal ITDC).
Signal ITAC is directly applied to Z-AMPLIFIER UNIT A15 and from there via a high voltage capacitor to the high voltage part of the circuit and to the intensity grid G1 of the C.R.T..

The low frequency component is applied to a modulation circuit, it can be influenced by a fine adjusting potentiometer R2637 and afterwards modulated with a frequency of 200 kHz from signal Z-MO--XT from the clock generator on the uP unit A6.
The resulting signal ITDC is applied to Z-AMPLIFIER unit A15 and via Z-circuit transferred via a high voltage capacitor to the high voltage part of the circuit. It is then demodulated, combined with the high frequency component and applied to the intensity grid G1 of the C.R.T..

FOCUS

The FOCUS circuit is influenced by the setting of the front panel FOCUS controls as well as the setting of the TRACE and TEXT intensity controls. The last is needed for the auto focus control when the intensity is changed with one of the frontpanel TRACE or TEXT intensity controls. There is also a fine adjustment potentiometer R2609.
The resulting signal FC is applied to the focus circuit on Z-AMPLIFIER UNIT A15 and from there to the focus grid G3 of the C.R.T..

8.1.7 Calibrator

The calibrator circuit is fed by signal Z-MO--XT of 200 kHz which is derived from the CLOCK GENERATOR circuit on the uP UNIT A6. This signal is divided by a factor of 100 by the dividers D2502 into a 2 kHz frequency. It is then applied to a CAL output socket via a stage where the amplitude can be adjusted via R2703. The output signal is a 2 kHz -1Vpp signal (50 Ohm).

8.1.8 Plot interface

The output signals Y1, Y2, X1 and X2 from the vertical and horizontal final amplifiers are applied to a plot interface where they are prepared to be plotted via the rear panel analog plot output socket.

The X-output gain can be adjusted with potentiometer R2728 and the Y-output gain with potentiometer R2738.
Sample and hold signal SAPL activates the interface for a plot action. Signals are only applied to the output socket when enabled by signal PLZEOT if a value is stored in the sample and hold circuit.

A pen lift circuit is activated via the PLIN signal (when an overscan is detected). The penlift flip flop can be reset by the PEN UP signal PU----LT.

The pen lift polarity can be influenced by signal PFPY via exclusive or circuit D2504.

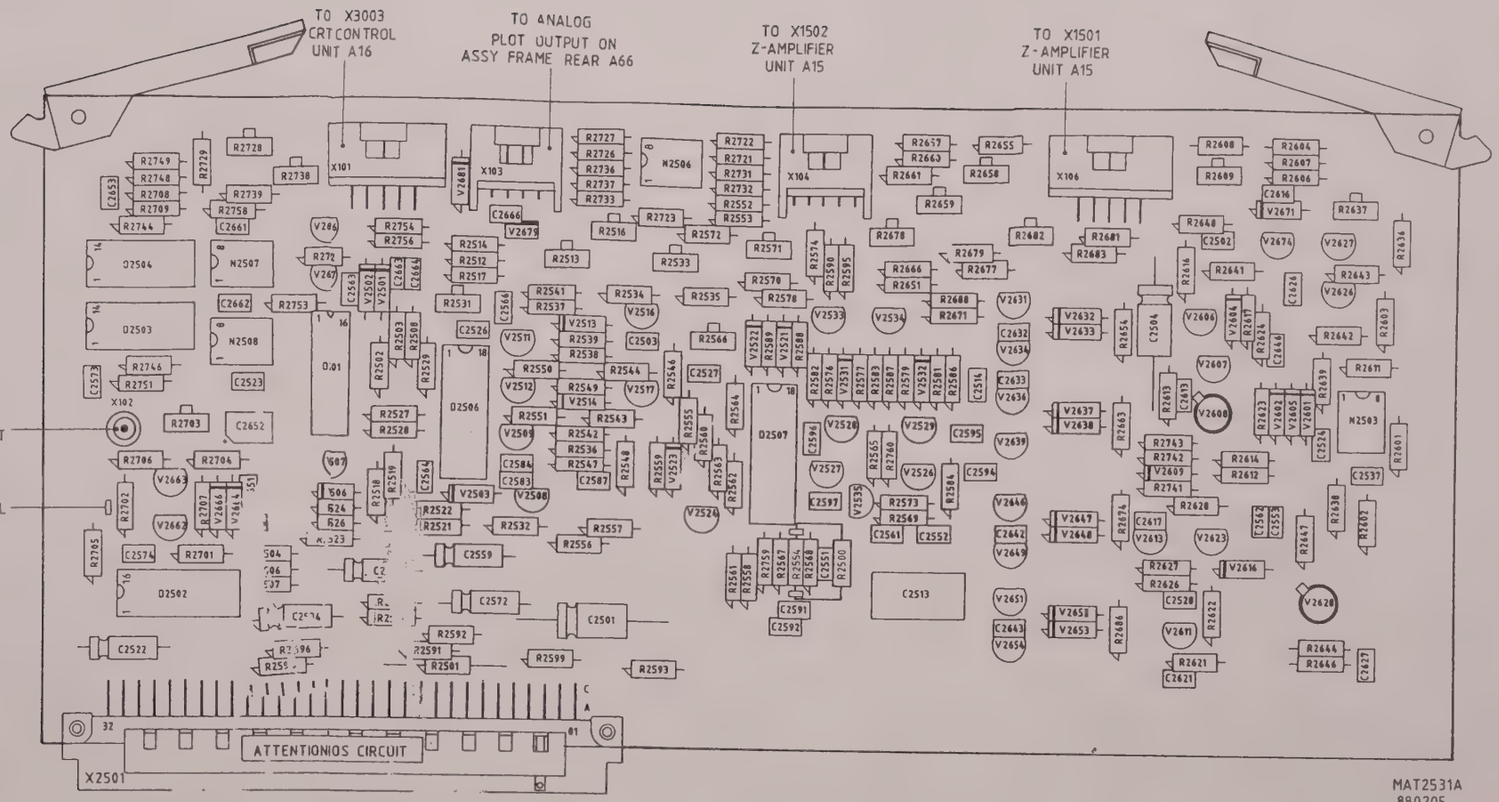


Figure 8.1.5 Unit A1 - FINAL AMPLIFIER UNIT - p.c.b. lay-out.

8.1.9 Signal-name list

UNIT A1

Signal name	Description	Signal source	Signal destination(s)
ANCPY-HT	Analog compress Y	A3	-
ANEPY-HT	Analog expand Y	A3	-
DIOS--HT	Disable overscan	A3	-
DPTR--HT	Display trace	A3	-
FC	Focus	A1	A15
FCIN	Focus input	A16	-
ITAC	Intens a.c. component	A1	A15
ITDC	Intens d.c. component	A1	A15
ITTR	Intensity trace	A16	-
ITTX	Intensity text	A16	-
PENLIFT	Penlift	A1	A66
PLIN	Plot input	A1	A1
PFPY	Penlift polarity	A3	-
PLZEOT	Plot zero output	A3	-
PU----LT	Pen-up	A3	-
SAPL	Sample plot	A3	-
X1	X1 input for C.R.T.	A1	A15-C.R.T.
X2	X2 input for C.R.T.	A1	A15-C.R.T.
X1IN	X1 input final amplifier	A2	-
X2IN	X2 input final amlpifier	A2	-
X-PL	X plot	A1	A66
Y1	Y1 input for C.R.T.	A1	A15-C.R.T.
Y2	Y2 input for C.R.T.	A1	A15-C.R.T.
Y1IN	Y1 input final amplifier	A2	-
Y2IN	Y2 input final amplifier	A2	-
Y-PL	Y plot	A1	A66
VREPX1...X2	Variable expand X	A2	-
Z-BL--HT	Z-blanking	A3	-
Z-MO--XT	Z-modulation (200 kHz)	A6	-

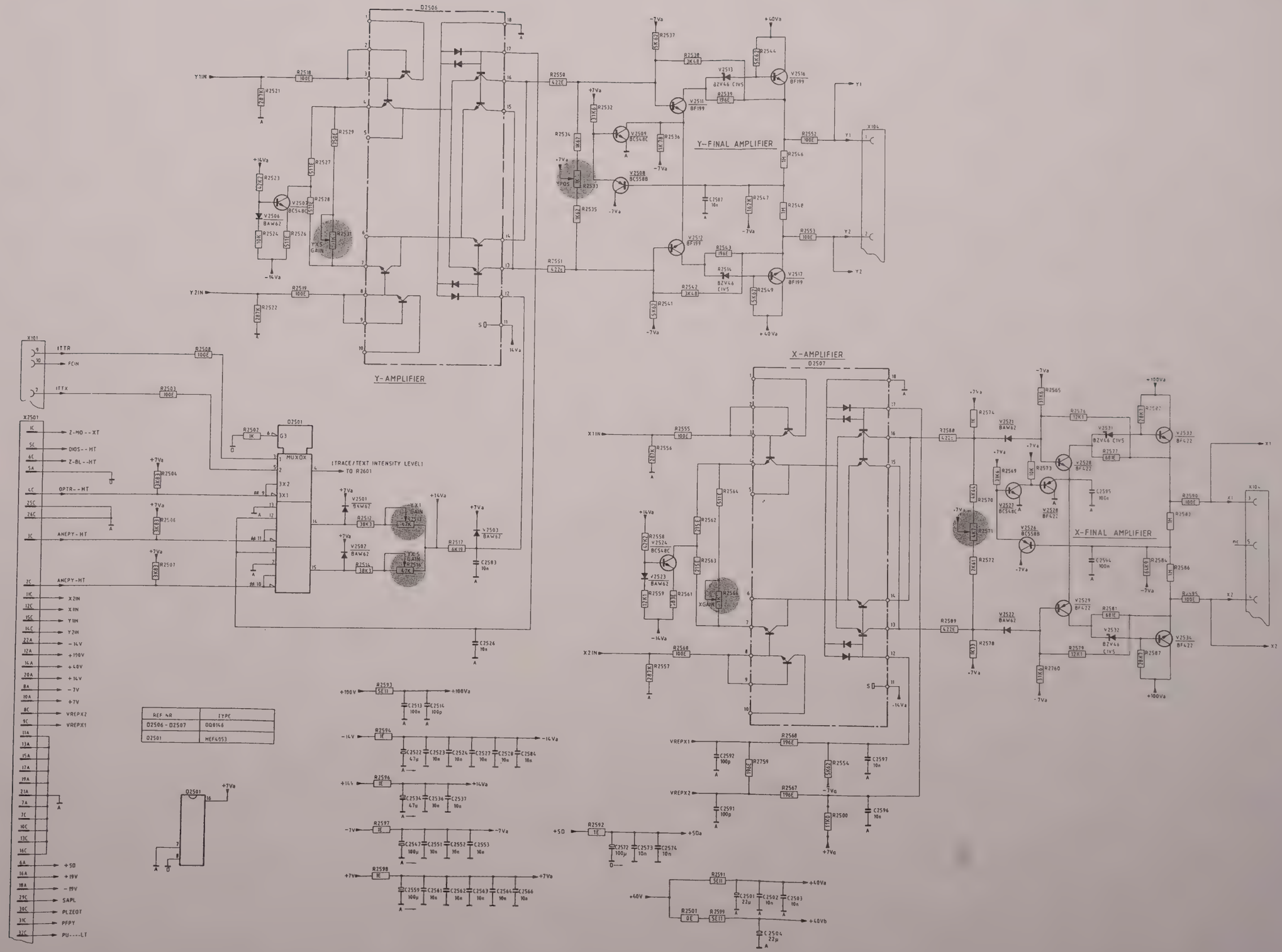


Figure 8.1.6 Unit A1 - FINAL AMPLIFIER UNIT - circuit diagram.

OVERSCAN DETECTOR

Z AMPLIFIER

MODULATOR

FOCUS

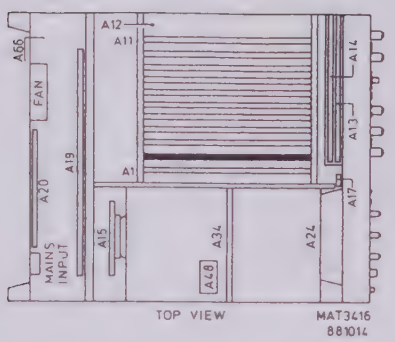
CALIBRATOR

ANALOG PLOT INTERFACE

REF NO	TYPE	+50a	+14Va	-14Va	$\frac{0}{0}$	
D2502	74HCT390	16			8	
D2503	74HCT74	14			7	
D2504	74HCT86	14			7	
N2503	LM358		8	4		
N2506	TL082		8	4		
N2507 N2508	LF398		1	4		

Figure 8.1.7 Unit A1 - FINAL AMPLIFIER UNIT - circuit diagram.

UNIT A2 - DISPLAY DAC UNIT



CONTENTS

8.2.1 General information..... 8.2-1
8.2.2 Vertical data path..... 8.2-1
8.2.3 Horizontal data path..... 8.2-6
8.2.4 X-Variable data path..... 8.2-11
8.2.5 Signal-name list..... 8.2-11

8.2.1 General information

This unit basically comprises the vertical and horizontal position adders and the vertical and horizontal digital to analog converters.

8.2.2 Vertical data path

The vertical trace data as well as all kinds of vertical text data on the ten output lines DCDBØØ...DCDBØ9 of the display control latch is applied to a combined invert/vertical-expand/latch circuit. This circuit consists of the two (not identical) field programmable logic sequencers (FPLS) D2301 and D2302 and the D-type flip flops D2309.
The control signal IVDCDB determines whether the data bits have to be inverted or not and the two control signals EPY-ØØ and EPY-Ø1 determine the vertical expand factor of the circuit.

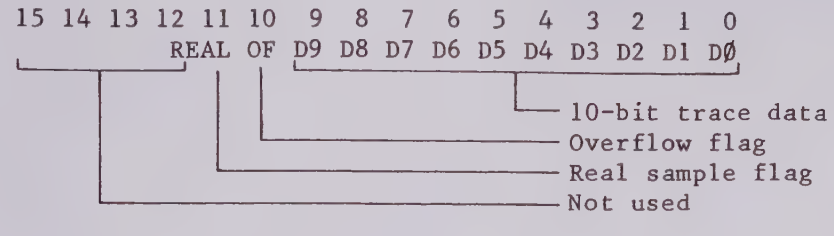
Vertical expand factor	Control signals		Digital expand factor (UNIT A2)	Analog expand factor (UNIT A1)
	EPY-Ø1	EPY-ØØ		
Y/5 (trace)	0	0	/4	/1,25
Y*1 (trace + MSC text)	0	1	x1	x1
line + softkey text	1	0	x4	x1
Y*5 (trace)	1	1	x4	x1,25

The combination of the digital expand factor on the display dac unit A2 and the analog expand factor on the final amplifier unit A1 results in the total required expand factor.
Digital expand is realized by the shifting of the bit pattern two bits to the right (/4) or two bits to the left (x4).
The resulting vertical data is then latched in the output latches of the FPLS circuits and in the four D-type flip flops by signal CKEPVE.

The data can be divided into five different kinds of data.

1) Trace data for X=t display:

Data format:



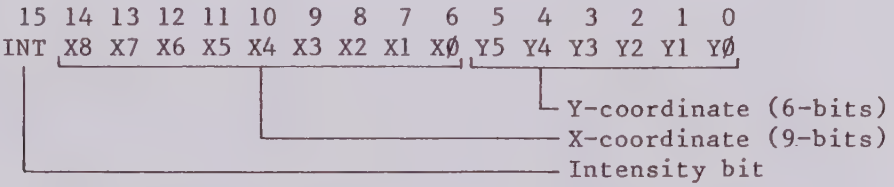
The trace data can be inverted, expanded by factors /5, x1 or x5 before it is applied as EPVEØØ...EPVE11 to the vertical position adder.

2) Trace data for AVSB display:

Data has the same format as for X=t display which is described before. However, only channel B is latched and applied to the vertical position adder.

3) Line text display: Top area text (TAT)
Trace area text (TRAT)
Bottom area text (BAT)

Data format:



Only 10 bits DCDBØØ...DCDBØ9 of this bit pattern are applied to the circuit and only the Y-coordinate bits YØ...Y5 are of interest.
The data is not inverted but expanded by a factor of x4 by shifting the pattern two bits to the left and switching the lowest two bits to zero. Signal ENTXLNLT is active and the output bits EPVEØ8...EPVE11 of D2309 are switched to one.

The final bit pattern is:

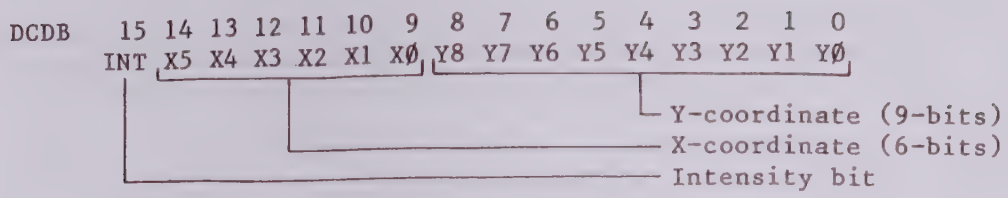
EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	1	1	Y5	Y4	Y3	Y2	Y1	YØ	Ø	Ø

This pattern is applied to the vertical position adder.

Figure 8.1./ Unit A1 - FINAL AMPLIFIER UNIT - circuit diagram.

4) Softkey text display (SKT):

Data format:



Only 10 bits DCDBØØ...DCDBØ9 of this bit pattern are applied to the circuit and only the nine Y-coordinate bits YØ...Y8 are of interest.
The data is not inverted but expanded by a factor of *4 by shifting the pattern two bits to the left and switching the lowest two bits to zero.

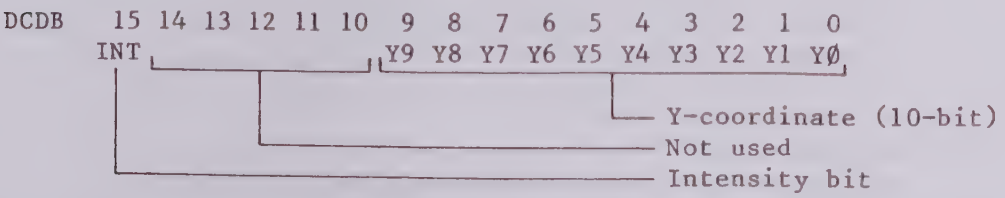
The final bit pattern is:

EPVE 11 10 9 8 7 6 5 4 3 2 1 0
Ø Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 YØ Ø Ø

This pattern is applied to the vertical position adder.

5) Miscellaneous text (MCS):

Data format Y-coordinates:



For miscellaneous text, two words, one carrying the Y-coordinate and the other one carrying the X-coordinate, are placed in the text memory for each dot to be displayed.
Only the 10 bits DCDBØØ...DCDBØ9 of the Y-coordinate pattern are applied to the circuit.
The data is not inverted and not expanded.

The final bit pattern is:

EPVE 11 10 9 8 7 6 5 4 3 2 1 0
Ø Ø Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 YØ

This pattern is applied to the vertical position adder.

The output signal Z-OTØ1LT of the first FPLS circuit D2301 is applied to the second one and the output signal Z-OTØ2LT of the second FPLS circuit D2302 is applied to a reflection detection circuit.

The vertical position adder is a sixteen bit circuit which consists of D2319, D2321, D2324 and D2326. A sixteen bit vertical position information is latched in the vertical position latches D2314 and D2316 by signal WRVEPOLT and applied to the other adder input side. This vertical position information is calculated by the microprocessor and depends on the selected vertical expand factor, the use of the Y-POSITION control and the type of trace or text which has to be displayed.

The adder output bits VEDBØ9...VEDB11 are carrying information about reflection and are applied to a Z-detection circuit on unit A3. The following combinations result in light on the C.R.T. screen.

VEDB 11	1Ø	Ø9	Ø8
0	0	0	1
1	1	1	0

All other combinations result in NO light on the C.R.T. screen. This has no function for text display.

The other ten adder output bits VEDBØØ...VEDBØ9 which carry information in two-complement notation, are first converted by the code convert circuit D2338 into straight binary notation by inverting the highest bit VEDBØ9. These converted ten bits are then latched for a time of 750 ns (time between two dots) in a YDAC latch consisting of D2329 and D2331. This is done by the signal LEDA-1HT. It is then applied to the 10-bits vertical digital-to-analog converter YDAC N2301 which has two symmetrical output current lines.
A constant reference voltage +10VREF from differential amplifier N2304 is applied to the YDAC.
The symmetrical output currents of the YDAC are converted into voltage levels by a Hooper stage with low input impedance and low output impedance. This Hooper stage is formed by the transistors V2301 and V2302. The signals are fed then to sample and hold circuits with switches D2341, capacitors C2366 and C2367 and field effect transistors V2303 and V2303 for the deglitching of the YDAC output signals. This is necessary for dot-join display because the trace is constantly unblanked then.
As long as the YDAC outputs are not stable, the switches D2341 are opened by the signal LEDA-1LT and the previous levels are held (for about 125 ns) over the capacitors C2366 and C2367 and at the inputs of the FET transistors V2303 and V2303. After 125 ns the YDAC outputs are stable and the switches are closed. The capacitors can then be charged to the new YDAC output levels. In this way, the YDAC output glitches are suppressed.

For display of only discrete dots, the S/H output signals are applied via an output buffer of two emitter followers V2304 and V2307 with high input impedance and low output impedance as Y1IN and Y2IN to the inputs of the vertical final amplifier stage on unit A1.

For dot-join display an RC-filter with an RC-time of 750 ns (1 dot cycle) can be switched in.
With signal DJAC--HT active, capacitor C2373 will be switched in via switch D2341. In this case only the real samples (512) will be connected with each other with lines between the dots.

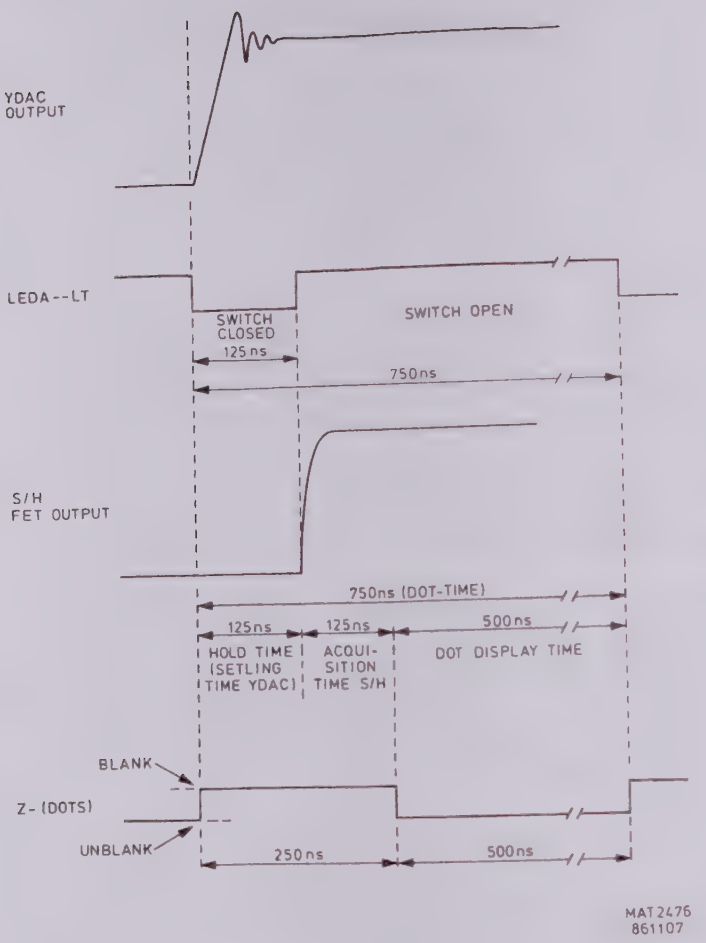


Fig. 8.2.1 Dot cycle

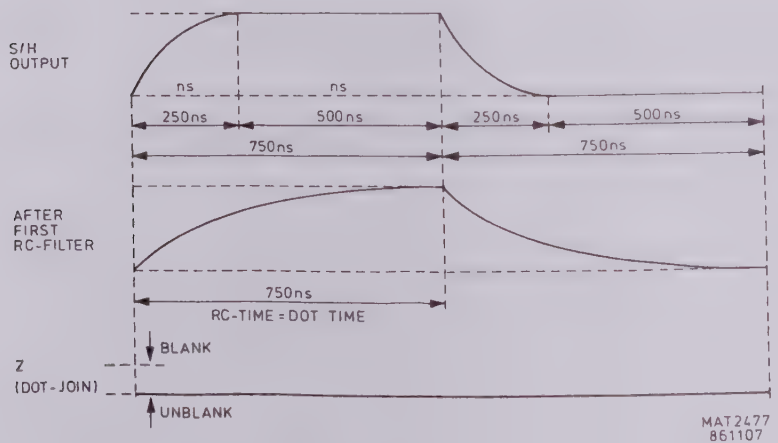


Fig. 8.2.2 Dot join cycle

8

For smooth display not only the dot-join filter is switched in, but also the smooth filter which gives a total RC-time of 7,5 us (10 dot cycles).
This second RC-filter is switched in when signal SM----LT is activated. Capacitor C2369 is switched in via switch D2342 and lines are displayed over ten dots.

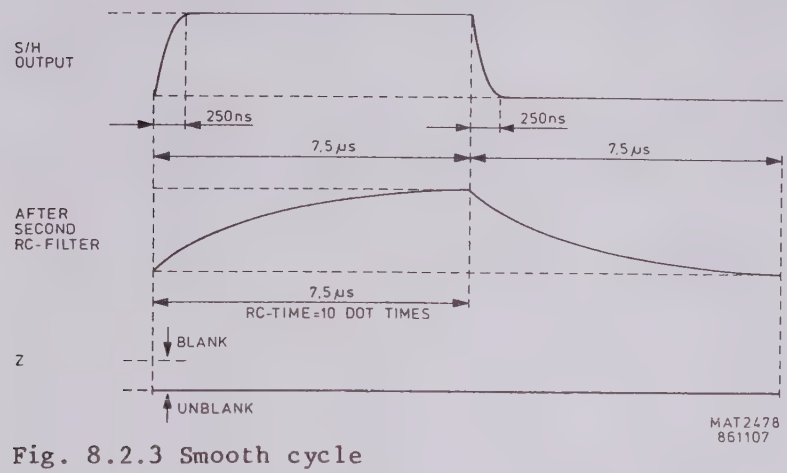


Fig. 8.2.3 Smooth cycle

8.2.3 Horizontal data path

Horizontal data on the expand data bus lines EPDBØØ...EPDB111 can be divided into five kinds of data.

1) Address data for X=t display:

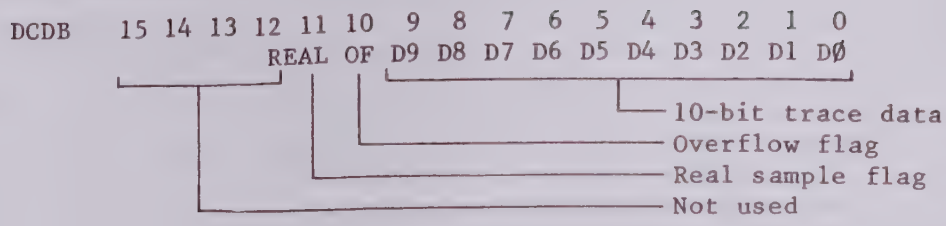
Data format:

DPAB	11	10	9	8	7	6	5	4	3	2	1	0
A	11	10	9	8	7	6	5	4	3	2	1	Ø

12-bit address data from the display address counter on unit A3.

The state of the display address counter is used for horizontal deflection during normal X=t display.
This data is applied to the expand data bus lines EPDBØØ...EPDB11 via the display address data buffer, which consists of D2121 on unit A3 and a part of D2122 on unit A3, when signal HOMO is active.

2) Trace data for AVSB display:



Vertical trace data bits DCDBØØ...DCDBØ9 of channel A for X-deflection in A versus B mode is applied to the expand data bus lines EPDBØØ...EPDB11 via the AVSB trace data buffer, which consists of D2303 and a part of D2304. This buffer is active when signal ENTRHOLT is activated.
The highest bit is inverted by the code convert circuit D2337 to convert the trace data from two-complement notation to straight binary notation. (For channel B this is done in the vertical channel path).
Via the AVSB trace data buffer the data is multiplied by a factor of four to adapt it to the higher horizontal resolution.

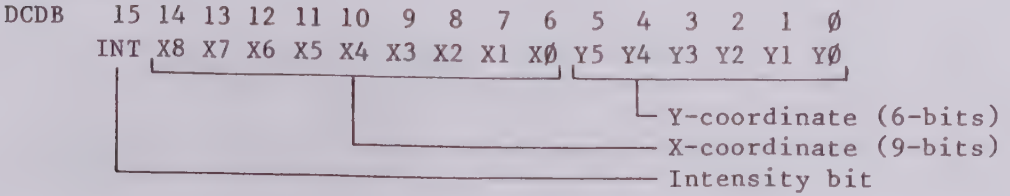
The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	D9	D8	D7	D6	D5	D4	D3	D2	D1	DØ	Ø	Ø

This pattern is applied to the horizontal expand I circuit.

3) Line text display: Top area text (TAT)
Trace area text (TRAT)
Bottom area text (BAT)

Data format:



Only the 9 X-coordinate bits DCDBØ6...DCDB14 or XØ...X8 are of interest. These bits are applied to the expand data bus lines via the line text data buffer which consists of a part of D2304 on unit A2 and D2124 on unit A3. This buffer is active when signal ENTXLNLT is active. The data is via this line text data buffer expanded to twelve bits of which the lowest three bits are made zero.

The final bit pattern is:

EPDB	11	10	9	8	7	6	5	4	3	2	1	Ø
	X8	X7	X6	X5	X4	X3	X2	X1	XØ	Ø	Ø	Ø

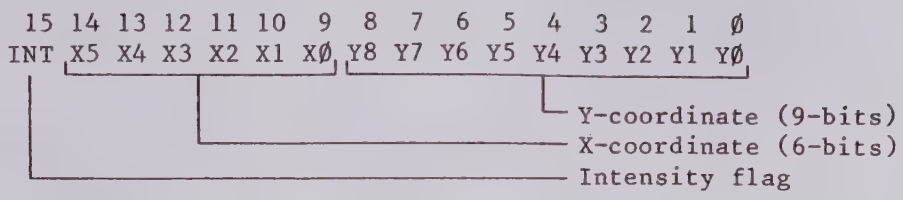
This pattern is applied to the horizontal expand I circuit.

In line text display mode, the X-variable is automatically set by the microprocessor to *1,5.

This results in 512 horizontal text dot positions over 15

4) Softkey text display (SKT):

Data format:



Only the six X-coordinate bits DCDBØ9...DCDB14 or XØ...X5 are of interest. These bits are applied to the expand data bus lines via the softkey text data buffer which consists of D2133 on unit A3 and a part of D2122 on unit A3. This buffer is active when signal ENTXSKLT is active. The data is converted to twelve bits via this buffer. The highest three as well as the lowest three bits are made zero.

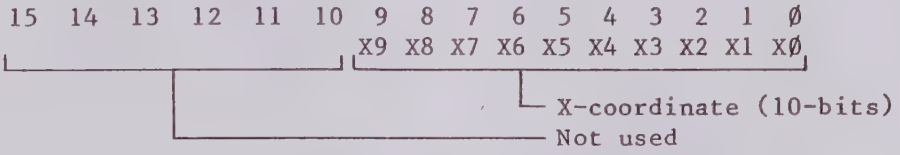
The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	Ø
	Ø	Ø	Ø	X5	X4	X3	X2	X1	XØ	Ø	Ø	Ø

In softkey text display-mode the X-variable is automatically set to *1,5 by the microprocessor.
This results in 512 horizontal text dot positions over 15 divisions, so with a dot distance of 0,293 mm.

5) Miscellaneous text (MSC):

Data format X-coordinates:



For miscellaneous text, two words, one carrying the Y-coordinate and the other one carrying the X-coordinate, are placed in the text memory for each dot to be displayed.
Only the 10 bits DCDBØØ...DCDBØ9 of the X-coordinate pattern are applied to the circuit. The data is not expanded and the X-variable is set to *1.

The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	Ø
	X9	X8	X7	X6	X5	X4	X3	X2	X1	XØ	Ø	Ø

The pattern is applied to the horizontal expand I circuit.

The expand databus is connected to the horizontal expand I circuit consisting of a number of multiplexers. The first group D2305, D2307 and D2308 is able to shift the input bit pattern one bit to the left or not. This means that an expand factor *1 is selected if signal EXP-ØØ is "Ø" and that an expand factor of *2 is selected if signal EXP-ØØ is "1". The second group D2311, D2312 and D2313 is able to shift its input bit pattern two bits to the left or not.

This means that an expand factor *1 is selected if signal EXP-Ø1 is "Ø" and that an expand factor of *4 is selected if signal EXP-Ø1 is "1".
The combination of these two groups results in a circuit of which the expand factor can be switched to *1, *2, *4 or *8 depending on the signals EXP-ØØ and EXP-Ø1.

The twelve lines EPHOØØ...EPHO11 of the expand horizontal data bus are applied to one input side of a sixteen bit horizontal adder circuit which consists of D2322, D2323, D2327 and D2328.
A sixteen bit horizontal position information is latched in the horizontal position latches D2317 and D2318 by signal WRHOPOLT and applied to the other adder input side.
This horizontal position information is calculated by the microprocessor and depends on the selected horizontal expand factor, the use of the X-POSITION control and the type of trace or text which has to be displayed.

The signals HODB13, HODB14 and HODB15 are applied to a reflection detection circuit.

The adder output bits HODBØØ...HODB12 are applied to a horizontal expand II circuit which consists of the multiplexers D2333, D2334 and D2336. This circuit can be switched for and expand factor *1, when signal EPX-Ø2 is "Ø" and to a factor *8, when signal EPX-Ø2 is "1".

*1 The address range is shifted three bits to the left resulting in 512 horizontal display positions over ten divisions

*8 Only the lowest 10 bits of the address range is used resulting in an horizontal expand factor of *8.

Data is latched in the multiplexers by signal LEDA--LT and DPRJ.

Ten bits of the horizontal expand II circuit output data are applied to the 10-bits horizontal digital to analog converter XDAC (N2303) which has two symmectrical output current lines. A constant reference voltage +10VREF from differential amplifier N2304 is applied to the XDAC. The symmetrical output currents of the XDAC are furthermore handled like already described under 8.2.2. for the vertical data path. Afterwards they are applied as X1IN and X2IN to the inputs of the horizontal final amplifier stage on unit A1.

8.2.4 X-variable data path

X-variable data which depends on the use of the X-EXPAND rotary controls, is calculated by the microprocessor and placed on the data bus lines DBØ8...DB15. It is then latched in the X-variable latch D2332 when signal WRHOVRLT is active.
It is then applied to an 8-bit X-variable digital to analog converter N2302. A constant reference voltage +10VREF from differential amplifier N2304 is applied to the DAC. The symmetrical output current lines VREPX1 and VREPX2 are applied to the horizontal final amplifier stage on unit A1.

8.2.5 Signal-name list

UNIT A2

Signal-name	Description	Signal source	Signal destination(s)
CKEPVE	Clock expand vertical	A3	-
DBØØ...15	Data bus ØØ...15	A6+option	-
DCDBØØ...Ø9	Display control data bus ØØ...Ø9	A4	-
DIOS--HT	Disable overscan	A3	-
DJAC--HT	Dot join active	A3	-
DPRJUP	Display reject up	A3	-
DPRJDW	Display reject down	A3	-
DPRJDWØ1	Display reject down	A2	A2
ENTRHOLT	Enable trace horizontal	A3	-
ENTXLNLT	Enable text line	A3	-
EPDBØØ...11	Expanded data bus ØØ...11	A2,A3	A2
EPHOØØ...13	Expanded horizontal bus ØØ...13	A2	A2
EPHO14	Expanded horizontal bus 14	A3	-
EPVEØØ...11	Expanded vertical bus ØØ...11	A2	A2
EPVEØ8LT	Expanded vertical bus Ø8	A2	A2
EPVEØ9LT	Expanded vertical bus Ø9	A2	A2
EPX-ØØ...Ø2	Expand X ØØ...Ø2	A3	-
EPY-ØØ...Ø1	Expand Y ØØ...Ø1	A3	-
EP12--LT	Expand 12	A3	-
IVDCDB	Invert display control address bus	A3	-
LEDA--LT	Latch enable DAC	A3	-
LEDA-1LT	Latch enable DAC	A2	A2
LEDA--HT	Latch enable DAC	A3	-
LEDA-1HT	Latch enable DAC	A2	A2
HODBØØ...15	Horizontal data bus ØØ...15	A2	A2
HOPOØØ...15	Horizontal position bus ØØ...15	A2	A2
SM----LT	Smooth	A3	-

Signal-name	Description	Signal source	Signal destination(s)
VEDBØØ...12	Vertical data bus ØØ...12	A2	A2
VEDBØ9LT	Vertical data bus Ø9	A2	A2
VEDBØ9...12	Vertical data bus Ø9...12	A2	A12-A3
VEPOØØ...15	Vertical position bus ØØ...15	A2	A2
VREPX1...X2	Variable expand X	A2	A12-A1
WRHOPOLT	Write horizontal position	A3	-
WRHOVRLT	Write horizontal variable	A3	-
WRVEPOLT	Write vertical position	A3	-
X1IN	X1 input final amplifier	A2	A12-A1
X2IN	X2 input final amplifier	A2	A12-A1
Y1IN	Y1 input final amplifier	A2	A12-A1
Y2IN	Y2 input final amplifier	A2	A12-A1
Z-OTØ1LT	Z-output Ø1	A2	A2
Z-OTØ2LT	Z-output Ø2	A2	A2
Z-OTØ3	Z-output Ø3	A2	A12-A3

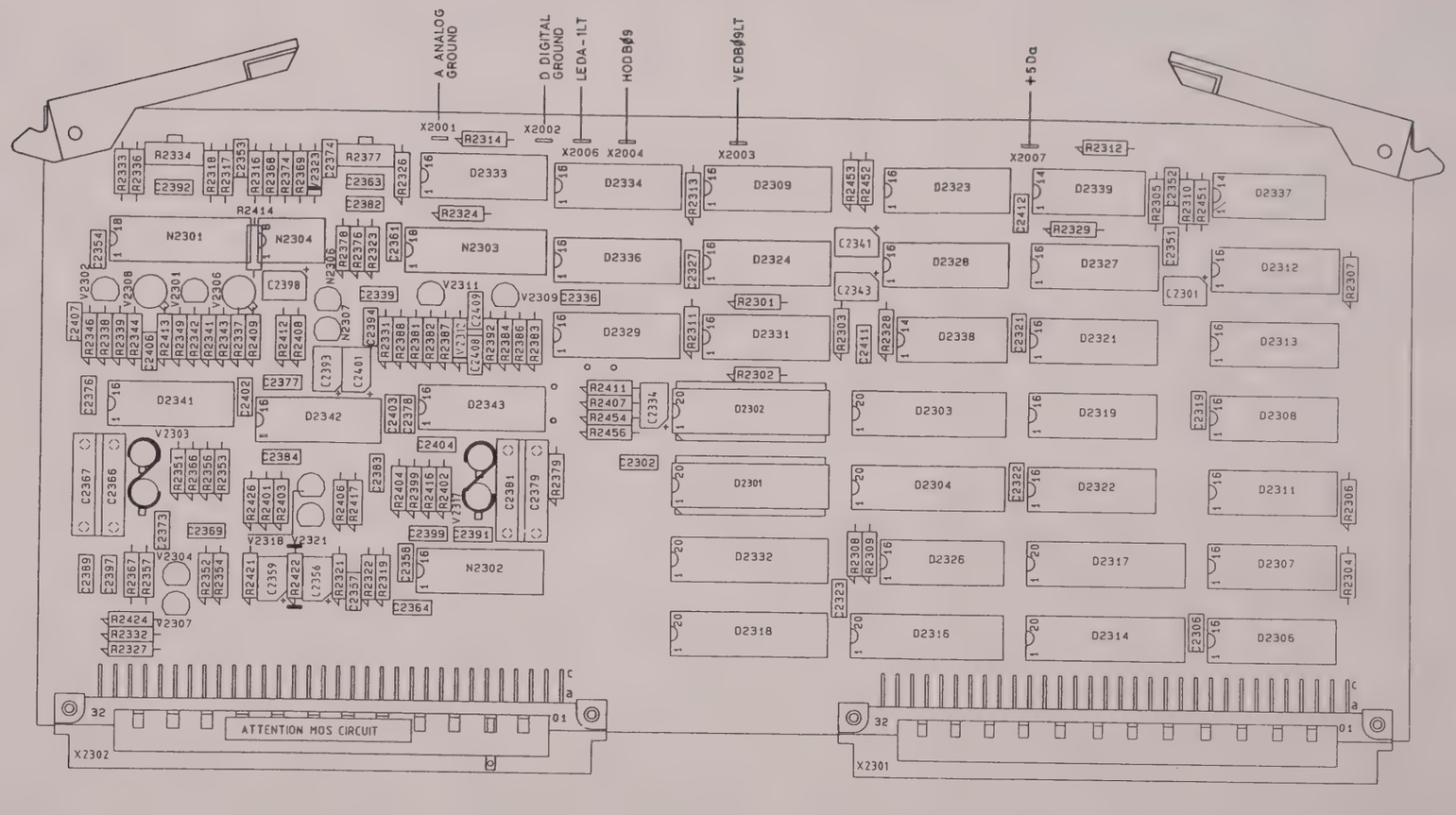


Figure 8.2.4 Unit A2 - DISPLAY DAC UNIT - p.c.b. lay-out.

MAT2532B
890217

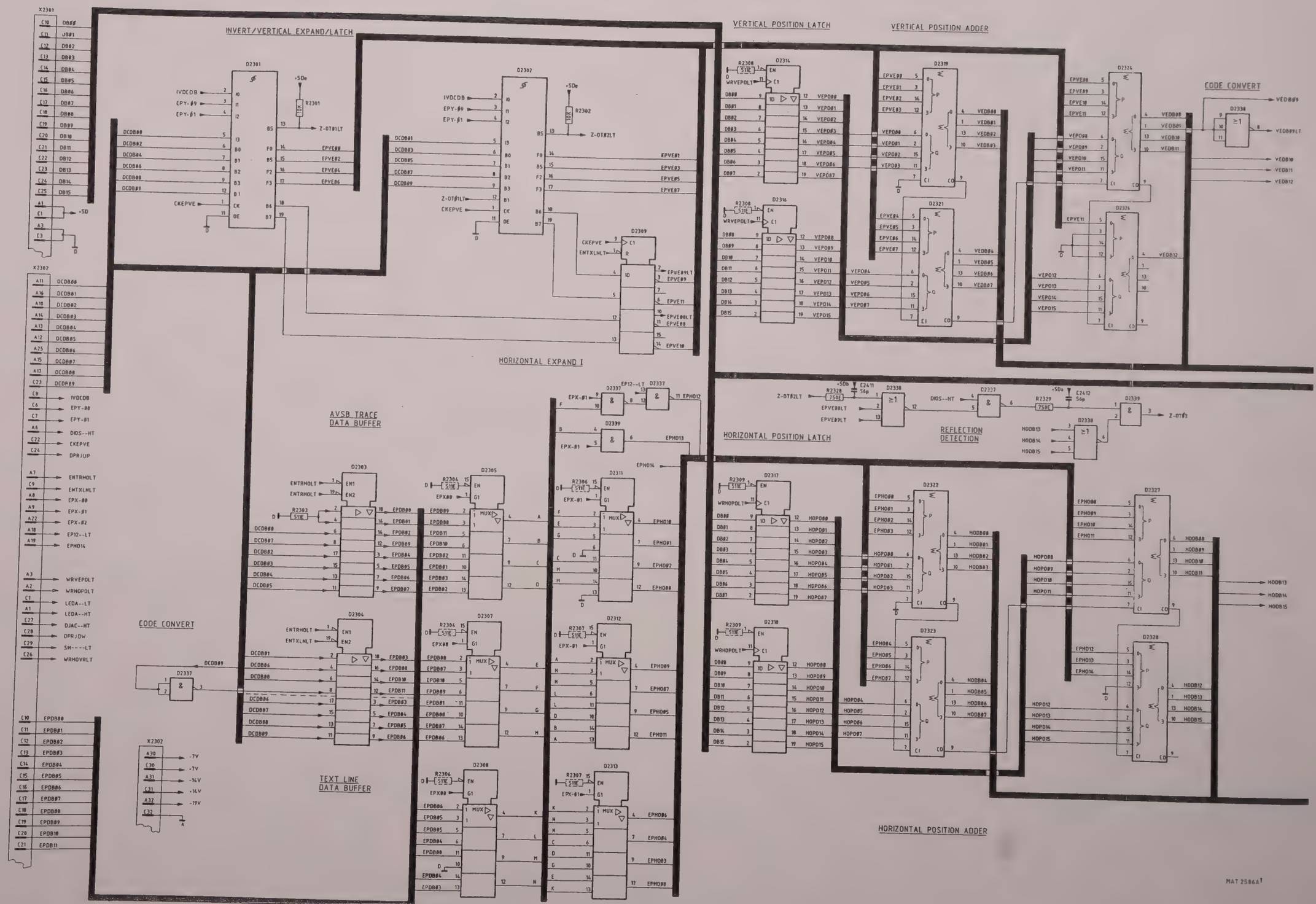
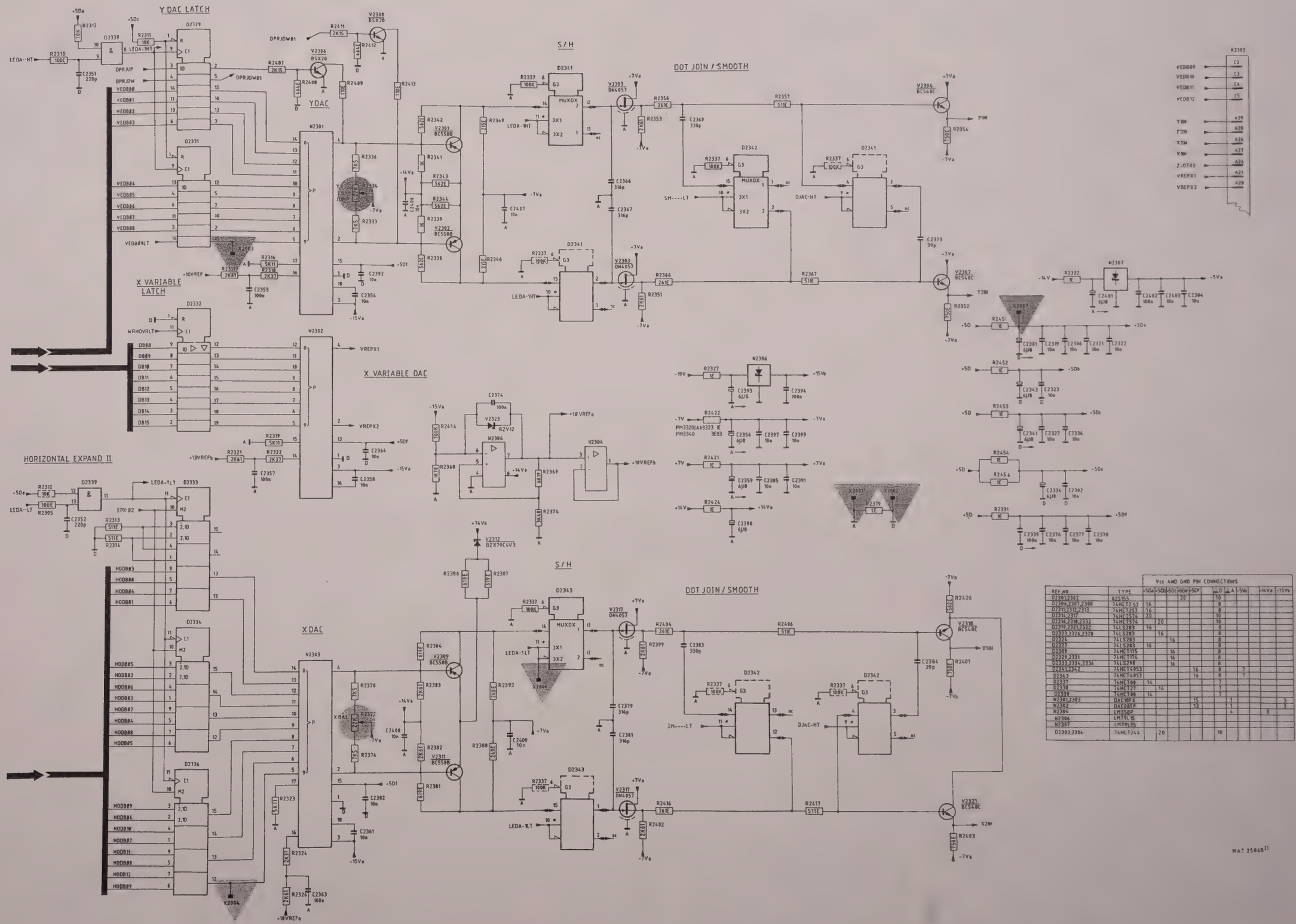


Figure 8.2.5 Unit A2 – DISPLAY DAC UNIT



REF.NR	TYPE	Vcc AND GND PIN CONNECTIONS									
		+5Da	+5Dc	+5Df	-5Df		D	A	+5Va	-14Va	-15Va
D2301,2302	825155				20		10				
D2306,2307,2308	74HCT257	16					8				
D2311,2312,2313	74HCT257	16					8				
D2314,2317	74HCT574	20					10				
D2316,2318,2332	74HCT574		20				10				
D2319,2321,2322	74LS283	16					8				
D2323,2326,2328	74LS283		16				8				
D2324	74LS283			16			8				
D2327	74LS283	16					8				
D2309	74HCT139			16			8				
D2329,2331	74HCT174			16			8				
D2333,2334,2336	74LS298			16			8				
D2341,2342	74HCT4053				16		8	7			
D2343	74HCT4053				16		8	7			
D2337	74HCT00	14					7				
D2338	74HCT27		14				7				
D2339	74HCT08	14					7				
W2301,2303	DACMDFX					15		1			3
W2302	DACDBEP					13		1			2
W2304	LM358P							4		8	
W2306	LM79L15										
W2307	LM79L05										
D2303,2304	74HCT244	20					10				

MAT 2506B[1]

Figure 8.2.6 Unit A2 - DISPLAY DAC UNIT - circuit diagram.

Signal-name	Description	Signal source	Signal destination(s)
SAVE--LT	Save	A3	A3
SLTR1LLT	Select trace 1L	A3	A12-A4
SLTR1HLT	Select trace 1H	A3	A12-A4
SLTR2LLT	Select trace 2L	A3	A12-A4
SLTR2HLT	Select trace 2H	A3	A12-A4
SM----LT	Smooth	A3	A12-A2
SMDL--LT	Smooth delay	A3	A3
STDP	Start display	A3	A3
SVR1	Save register R1	A3	A3
SVR2--LT	Save register R2	A3	A3
SVR3	Save register R3	A3	A3
SYDP	Synchronize display	A3	A12-A8
TRAB13	Trace address bus 13	A3	A12-A4
TXAB13	Text address bus 13	A3	A12-A4
TXLNSKLT	Text line softkey	A3	A3
UPCKØ8	Microprocessor clock 8 Mhz	A6	-
UPRD--LT	Microprocessor read	A6	-
UPRD--HT	Microprocessor read	A3	A3
UPRSOTLT	Microprocessor reset out	A6	-
UPWR--LT	Microprocessor write	A6	-
VEDBØ9...12	Vertical data bus Ø9...12	A2	-
WETRØ1LT	Write enable trace Ø1	A3	A4
WETRØ2LT	Write enable trace Ø2	A3	A12-A4
WETX--LT	Write enable text (WRØ2--LT)	A3	A12-A4
WRAQ--LT	Write acquisition	A3	A3
WRAQ--HT	Write acquisition (SARYAKLT)	A3	A3
WRDPPALT	Write display parameters	A3	A3
WRDPSTLT	Write display start	A3	A3
WRHOPOLT	Write horizontal position	A3	A12-A2
WRHOVRLT	Write horizontal variable	A3	A12-A2
WRPSDPLT	Write preset display	A3	A3
WRVEPOLT	Write vertical position	A3	A12-A2
WRØØ--LT	Write ØØ	A3	A3
WRØ1--LT	Write Ø1	A3	A3
WRØ2--LT	Write Ø2 (WETX--LT)	A3	A12-A4
Z-AC--LT	Z - active	A3	A3
Z-BL--HT	Z - blanking signal	A3	A12-A1
Z-DP	Z - display	A3	A3
Z-OTØ3	Z - output Ø3	A2	-

Signal-name	Description	Signal source	Signal destination(s)
DPMYRDHT	Display memory read	A3	A3
DPMYWRHT	Display memory write	A3	A3
DPMYØØ...Ø2	Display memory ØØ...Ø2	A3	A3
DPMYØ2LT	Display memory Ø2	A3	A3
DPRJUPLT	Display reject up	A3	A12-A2
DPRJDWLT	Display reject down	A3	A12-A2
DRTXTR	Direction text trace buffer	A3	A12-A4
DPTR--HT	Display trace (DPMYØ2LT)	A3	A12-A1
ENDPCN	Enable display counter	A3	A3
ENTRHOLT	Enable trace horizontal	A3	A12-A2
ENTRHOHT	Enable trace horizontal	A3	A3
ENTXLNLT	Enable text line	A3	A12-A2
ENTXSKLT	Enable text softkey	A3	A3
EPDBØØ...11	Expanded data bus	A2,A3	A12-A2
EPH014	Expanded horizontal bus 14	A3	A12-A2
EPX-ØØ...Ø2	Expand X ØØ...Ø2	A3	A12-A2
EPY-ØØ...Ø1	Expand Y ØØ...Ø1	A3	A12-A2
EP12--LT	Expand 12	A3	A12-A2
HOMO	Horizontal mode	A3	A3
ILØ5--LT	Interrupt level Ø5	A3	A12-A6
ILØ5DPLT	Interrupt level Ø5 display	A3	A3
IOSLØ5LT	I/O select Ø5	A6	-
IVDCDB	Invert display control address bus	A3	A12-A2
LEDA--LT	Latch enable DAC	A3	A12-A2
LEDA--HT	Latch enable DAC	A3	A12-A2
LEDC	Latch enable display control	A3	A12-A4
MXCPAD (WRAQ--HT)	Multiplex copy address	A3	A12-A4
MYSLØ2LT	Memory select Ø2	A6+option	-
MYSLØ2HT	Memory select Ø2 (CLUPAB)	A3	-
OETRØ1LT	Output enable trace Ø1	A3	A12-A4
OETRØ2LT	Output enable trace Ø2	A3	A12-A4
OETX--LT	Output enable text	A3	A12-A4
PFPY	Penlift polarity	A3	A12-A1
PLOT	Plot	A3	A3
PLZEOT	Plot zero output	A3	A12-A1
PSDPØØ...11	Present display bus ØØ...11	A3	A3
PU----LT	Pen-up signaal	A3	A12-A1
RDDM--LT	Read display memory	A3	A12-A4
RDDPDALT	Read display data	A3	A3
RSDAAKLT	Reset data acknowledge	A3	A3
RTDP--LT	Restart display	A3	A3
SAPL	Sample plot	A3	A12-A1
SAPL--LT	Sample plot	A3	A3
SARY	Sample ready	A4	-
SARYAKLT	Sample ready acknowledge (DITRDB) (WRAQ--RT)	A3	A12-A4

8.3.4 Signal-name list

UNIT A3

Signal-name	Description	Signal source	Signal destination(s)
ABØ1...15	Address bus Ø1...15	A6	-
ANCPY-HT	Analog compress Y	A3	A12-A1
ANEPY-HT	Analog expand Y	A3	A12-A1
BUAB13...15	Buffered address lines 13...15	A3	A3
BUHISBLT	Buffered high strobe	A3	A3
BULOSBLT	Buffered low strobe	A3	A3
CHID	Channel indentification	A3	A3
CKEPVE	Clock expand vertical	A3	A12-A2
CKSVLA	Clock save latch	A3	A12-A4
CK/2--LT	Clock /2	A3	A3
CK/2--HT	Clock /2	A3	A3
CK/3	Clock /3	A3	A3
CK/6-ØLT	Clock /6-Ø	A3	A3
CK/6-ØHT	Clock /6-Ø	A3	A3
CK/6-1LT	Clock /6-1	A3	A3
CK/6-1HT	Clock /6-1	A3	A3
CK/6-2LT	Clock /6-2	A3	A3
CK/6-2HT	Clock /6-2	A3	A3
CLDPAB	Clock display address bus (CK/6-1HT)	A3	A12-A4
CLUPAB	Clock microprocessor bus (MMYSLØ2HT)	A3	A12-A4
CSTX--LT	Chip select text	A3	A12-A4
CSZ-CNLT	Chip select Z-counter	A3	A3
DAAK--LT	Data acknowledge	A3	A12-A4
DAAK--HT	Data acknowledge	A3	A12-A4
DAHISBLT	Data high strobe	A6+option	-
DALOSBLT	Data low strobe	A6+option	-
DATRAKLT	Data trace acknowledge	A3+A5+A6+A8 +option	A12-A6, A12-option
DBØØ...15	Data bus ØØ...15	A6+option	-
DCDBØ9...15	Display control data bus Ø9...15	A4	-
DIDBTX	Disable data bus text-buffer	A3	A12-A4
DIDJ	Disable dot join	A3	A3
DIDPCN	Disable display counter	A3	A3
DIDPPS	Disable display preset	A3	A3
DIOS--HT	Disable overscan	A3	A12-A1,A12-A2
DISVLA	Disable save latch	A3	A4
DITXTR	Disable text trace buffer	A3	A12-A4
DJAC--HT	Dot join active	A3	A12-A2
DPABØØ...11	Display address bus ØØ...11	A3	A12-A4
DPCKØ8LT	Display clock 8 Mhz	A3	A3
DPCKØ8HT	Display clock 8 Mhz	A3	A3
DPCNCK	Display counter clock	A3	A3
DPDBØØ...15	Display data bus ØØ...15	A3	A3
DPMO--LT	Display mode	A3	A3

8.3.3.14 Start + smooth delay flip flop

The START flip flop is blocked by signal IL05DPLT on input 11 as long as a display preset sequence is performed. At the end of such a sequence a display start signal WRDPSTLT is generated and the start flip flop D2127 produces a 3 us start signal STDP. This STDP signal is applied to the synchronization flip flop D2114 to start the display of a new block.

A new display action can also be started via a RTDP--LT output pulse from the restart-timer.

If SMOOTH is selected, an additional delay of 12 us is introduced by smooth delay flip flop D2127 and a smooth delay signal SMDL--LT is then applied to sychronization flip flop D2116. This is done at the end of a sweep to avoid connection of the last dot of a sweep with the first one of the next sweep.

8.3.3.15 Plot one-shot

If a plot function is selected (signal PLOT active) the plot one-shot D2144 will generate a sample plot pulse SAPL for the analog plot interface on unit A1 at the beginning of the plot block. This is the last block of a display cycle.

In this way one dot per display cycle can be plotted. The minimum plot time is therefore 20 ms/dot. Slower plot speeds can be selected via the PLOT menu.

The microprocessor knows how many dots have to be plotted and which actual dot has to be plotted. The memory addres of the actual dot to be plotted, is presetted in the display address counter and the data which is stored in this addres location is applied to the plot interface on unit A1.

The penlift (pen up/pen down) can be controlled via the microprocessor generated signal PU----LT.

The polarity of the penlift is also generated by the microprocessor by generating signal PFPY.

If the Z-signal is blanked (during overscan for example) the pen is also lifted automatically.

If no plot function is selected, the plot outputs are short circuited via signal PLZEOT.

8.3.3.9 Memory select

The MEMORY SELECT circuit which mainly consists of the FPLA circuit D2151 generates a number of memory select, output enable and write enable signals.

8.3.3.10 Z-detection

The Z-DETECTION circuit which mainly consists of FPLS circuit D2142 generates one output signal Z-BL--HT which carries the blanking/unblanking information for the C.R.T. This signal is derived from a number of input conditions from a number of display circuits.

8.3.3.11 Z-timer

The Z-TIMER is for each block presetted with a value which is calculated by the microprocessor. The value depends on the total number of dots to be displayed during the actual display block. The counter starts counting down latch enable pulses LEDA--HT when enable display count signal ENDPCN is active. Until the end of the counting, when the zero state of the counter is reached, an output signal Z-DP is applied to the Z-DETECTION circuit. The C.R.T. trace can only be unblanked as long as the Z-TIMER is counting and signal Z-DP is generated.

8.3.3.12 Restart timer

This timer especially has a function when X-EXPAND is selected and is for each block presetted with a value which is calculated by the microprocessor. The value depends on the X-EXPAND factor and the total number of dots to be displayed during the actual display block.

If for example the X-EXPAND factor is *4, the display block will be displayed four times in order to reach a same trace intensity on the C.R.T. screen as there is without X-expansion.

After the first display action, when the zero state of the restart timer is reached, and restart display signal RDDP--LT is generated to start the second display action and so on. After display action four (in this example) the end of the complete display block is given by the ILØ5--LT output signal from the interrupt timer.

8.3.3.13 Interrupt timer + flip flop

This timer is for each display block presetted with a value which is calculated by the microprocessor. The value depends on the total number of dots to be displayed during the actual display block. The counter starts counting down latch enable pulses LEDA--HT when enable display count signal ENDPCN is active. At the end of the counting, when the zero state of the counter is reached, an output signal is applied to the interrupt flip flop D2133 and an interrupt signal ILØ5--LT for the microprocessor is generated to indicate the end of the actual display cycle.

8.3.3.6 Address decoder

An address decoder D2132 is able to decode a number of addresses which are generated by the microprocessor.
This results in a number of signals (see also the preset sequence under section 8.3.2) according to the following table.

IOSLØ5LT	UPWR--LT	ABØ4	ABØ3	ABØ2	ABØ1	Output signal
0	0	1	0	0	0	WRDPSTLT
0	0	1	0	0	1	--
0	0	1	0	1	0	--
0	0	1	0	1	1	WRVEPOLT
0	0	1	1	0	0	WRHOPOLT
0	0	1	1	0	1	WRPSDPLT
0	0	1	1	1	0	WRDPPALT
0	0	1	1	1	1	WRHOVRLT

A chip select signal CSZ-CNLT for the Z-counter is generated via D2129 if IOSLØ5LT is active and ABØ4 is logic "0".

The signal overflow status can be read by the microprocessor via data bit DBØØ (D2128-6), which is derived from signal DCDB10 via flip flop D2114. The overflow status (one or more bits in a display block) is read by the microprocessor after each display cycle.

8.3.3.7 Clock fase generator

A binary counter D2134 which can be resetted via the microprocessor reset signal UPRSOTLT counts the pulses from the 8 MHz microprocessor clocksignal DPCKØ8HT.
During each counter cycle, the counter is presetted to the value eleven when its fourth output bit is zero and a new clockpulse appears. The counter then continuous counting which results in the timing clock signals as shown in figure 8.3.6.

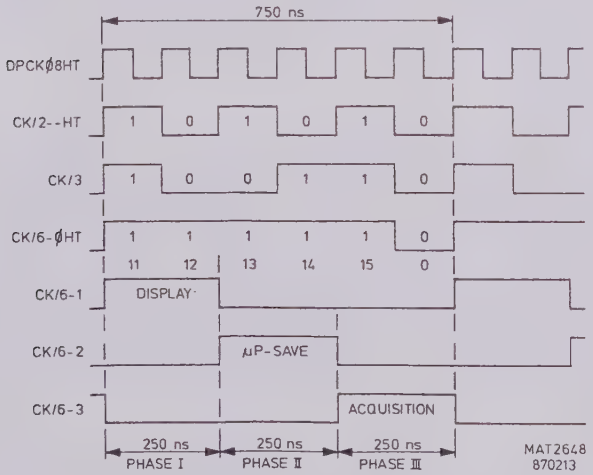


Figure 8.3.6 Clock signals.

8.3.3.8 Copy synchronization one-shot

The COPY SYNCHRONIZATION ONE-SHOT D2144 is used in the ROLL-mode for the synchronization between the display system and the DPU system by generating the synchronize display signal SYDP.
Signal SYDP indicates the end of the display block for register RØ.

8.3.3.4 Display address counter

The DISPLAY ADDRESS COUNTER, consisting of the counters D2111, D2112 and D2113, generates the addresses of the TRACE MEMORY locations to be displayed.

The counter is normally (in single channel mode) presetted to its zero state before a display block starts and the counter counts through ist complete range during a display block.

In dual channel mode however, the counter needs to know whether channel A or channel B has to be displayed. The correct start address of the channel in the TRACE MEMORY has to be presetted by the microprocessor system. The counter counts then with a speed which is twice the speed in single channel mode.

The counter is always presetted by the value which is present in the PRESET REGISTER at the beginning of a display block. Presetting is done under the control of signal DIDPPS. Presetting is stopped at the start of a display block with signal STDP via flip flop D2114. Counting is started then under the control of signal DIDPCN.

The first output bit DPABØØ of the display counter is via multiplexer D2118 applied to the display address bus and influenced depending on the selection of single or dual channel mode.

Single channel mode: (HOMO = "0" and DPMO--LT = "1")

DPABØØ = DPABØØ

Dual channel mode: (HOMO = "0" and DPMO--LT = "0")

DPABØØ = CHID (Channel identification)

CHID = "0" means channel B (odd locations in memory)

CHID = "1" means channel A (even locations in memory)

In dual channel mode, the display counter clockpulse DPCNCK is switched to a speed which is twice the speed used in single channel mode.

The speed is:

1 1/3 MHz in single channel mode (derived from CK/6-ØHT)
2 2/3 MHz in dual channel mode (derived from CK/3)

8.3.3.5 Data buffers

There are buffers D2121 and D2122 (partly) for display addresses, D2122 (partly) and D2123 for softkey text and D2124 for line text.

If R1 or R3 is selected, the output of the SAVE latch is placed on the trace data bus during FASE III, address line TRAB13 is switched to "1" to point to R1 or R3 and the relevant chip select signal is activated.

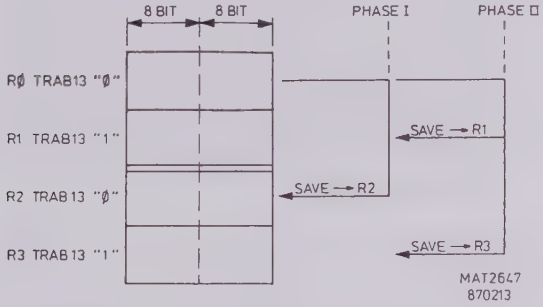


Figure 8.3.5 Save actions.

8.3.3 Circuit descriptions

8.3.2.1 Data buffer

Data from the microprocessor system on the data lines DBØØ...15, which is meant for the DISPLAY CONTROL unit A3, is applied to the internal display data bus lines DPDBØØ...15 of this unit. This data is transferred via the DATA BUFFER, which consists of D2101 and D2102 when the I/O select signal IOSLØ5LT is activated.

8.3.3.2 Preset register

Preset data from the microprocessor system can be latched in the PRESET REGISTER D2103 and D2104 (partly) when the write pulse WRPSDPLT is generated at the beginning of each new display block.
The data on the data lines PSDPØØ... PSDP11 is used to preset the DISPLAY ADDRESS COUNTER with a start value for the next display action. This value depends on the channel which is selected for display, the selected horizontal expand factor or the value which has to be plotted.

8.3.3.3 Output ports display parameters

A number of display parameters can be latched in the OUTPUT PORTS DISPLAY PARAMETERS D2104 (partly), D2106, D2107 and D2108 as described under section 8.3.2.

8.3.2.4 Display timing

The display timing is arranged in such a way that one dot is displayed per 750 ns. Each period of 750 ns is divided into three fases of 250 ns each like shown in the following figure.

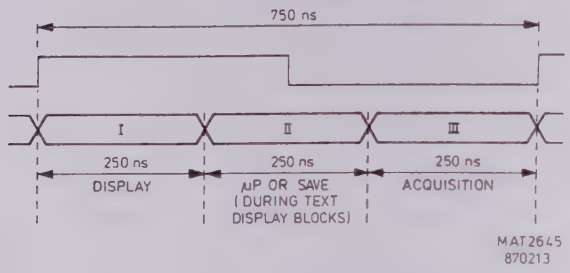


Figure 8.3.3 Display timing.

Fase I is for display actions, fase II for UP or SAVE actions and during fase III acquisition actions can be performed.

8.3.2.5 SAVE timing

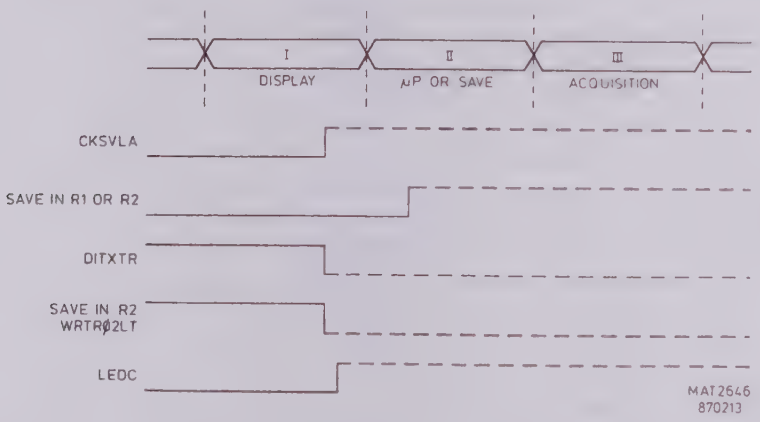


Figure 8.3.4 Save timing.

A save action from RØ to R1, R2 or R3 is done during the display of text blocks. It is done with the first 4096 addresses of the total of 8192 addresses which are generated by the display address counter. Each address is applied to register RØ, to the selected register and to the text memory.

The output data of RØ is latched in the SAVE latch during FASE I with signal CLKVLA.
If R2 is selected for a save action, this register is enabled directly to store the data value.
When this is done, the output of RØ is disabled and the output of the text memory is placed on the trace data bus via the TEXT/TRACE buffer via signal DITXTR. The text can be displayed then.

6 WRHOVRLT Write data to the OUTPUT PORT DISPLAY PARAMETERS D2108 on unit A3 and to the X VARIABLE LATCH D2332 on unit A2.

This is done together with the following signals:

EPY-Ø1	EPY-ØØ	Y-EXPAND
0	0	* 1/4 - Trace
0	1	* 1 - Trace + MSC text
1	0	* 4 - Text (Other)
1	1	* 4 - Trace

EPX-Ø2	EPX-Ø1	EPX-ØØ	X-EXPAND
0	0	0	*1
0	0	1	*2
0	1	0	*4
0	1	1	*8
1	0	0	--
1	0	1	*16
1	1	0	*32
1	1	1	*64

TXLNSKLT Text line + softkey
0 = TAT, RAT, BAT, SKT
1 = Trace + MSC

DIOS--HT Disable overscan
0 = Overscan
1 = No overscan

7 Initialization of Z-counter Ø

8 Initialization of Z-counter 1

9 Initialization of Z-counter 2

10 Preset of LSB countvalue of Z-counter Ø

11 Preset of MSB countvalue of Z-counter Ø

12 Preset of LSB countvalue of Z-counter 2

13 Preset of MSB countvalue of Z-counter 2

14 Preset of LSB countvalue of Z-counter 3

15 Preset of MSB countvalue of Z-counter 3

16 Clear instruction (read)

17 WRDPSTLT Start display of the next display block after the setting of the parameters

5 WRDPPALT

Write the display parameters which are listed below, to the OUTPUT PORTS DISPLAY PARAMETERS D2106 and D2107 on unit A3.

DPMYØ2	DPMYØ1	DPMYØØ	DISPLAY BLOCK
0	0	0	RØ
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	Text TAT/RAT
1	0	1	Text BAT/SKT/MSC
1	1	0	--
1	1	1	--

DPMO--LT Display mode
0 = Dual channel
1 = Single channel

CHID Channel identity
0 = Channel A
1 = Channel B

HOMO Horizontal mode
0 = X=t
1 = AvsB (or text)

SM----LT Smooth
0 = Smooth
1 = No smooth

DIDJ Disable dot join
0 = No dots, dot joined
1 = Dots (or text)

IVDCDB Invert display control databus
0 = No invert
1 = Invert

SVR1 Save to R1
0 = No save
1 = Save

SVR2--LT Save to R2
0 = No save
1 = Save

SVR3 Save to R3
0 = No save
1 = Save

SAVE--LT Save
0 = Save
1 = No save

ENTXLNLT Enable text lines
0 = TAT, RAT, BAT
1 = Other text

ENTXSKLT Enable text softkey
0 = SKT
1 = Other text

Z-AC Z-active
0 = No light
1 = Light

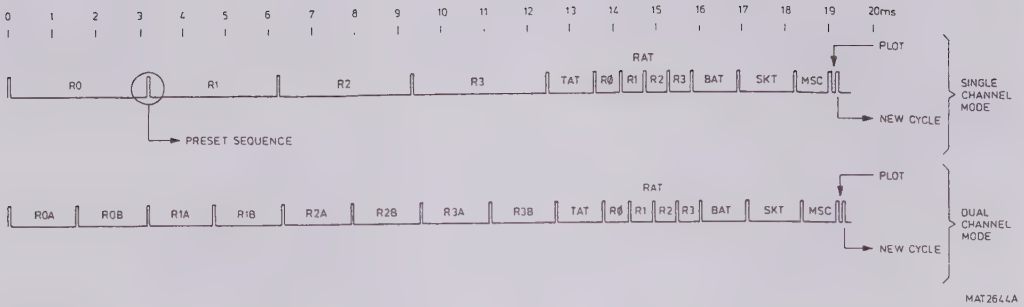


Figure 8.3.2 Display cycle.

8.3.2.3 Preset sequence

After the display of each display block an interrupt level signal ILØ5--LT is send to the microprocessor. The processor in turn starts a preset sequence of new preset values and new parameters for the display circuits. At the end of this preset sequence, signal WRDPSTLT is generated and the display of the next display cycle is started.

Presetting is done in the following sequence:

1 Read overflow bit from DBØØ

2 WRVEPOLT Write the vertical position data to the VERTICAL POSITION LATCH D2314 and D2316 on unit A2.

3 WRHOPOLT Write the horizontal position data to the HORIZONTAL POSITION LATCH D2317 and D2318 on unit A2.

4 WRPSDPLT Write the preset data for the display address counter to the PRESET REGISTER D2103 and D2104 on unit A3.

This is done together with the setting of the signals for the PLOT interface:

PLOT	0 = No sample in S&H
	1 = Sample in S&H
PU----LT	0 = Pen-up
	1 = Pen-down
PFPY	0 = Pen-up (high)
	1 = Pen-up (low)
PLZEOT	0 = Plot output active
	1 = Plot output not active

These four signals are only generated when a plot action has to be performed.

8.3.2 Display system and timing

8.3.2.1 Screen lay out

The screen lay out is as follows.

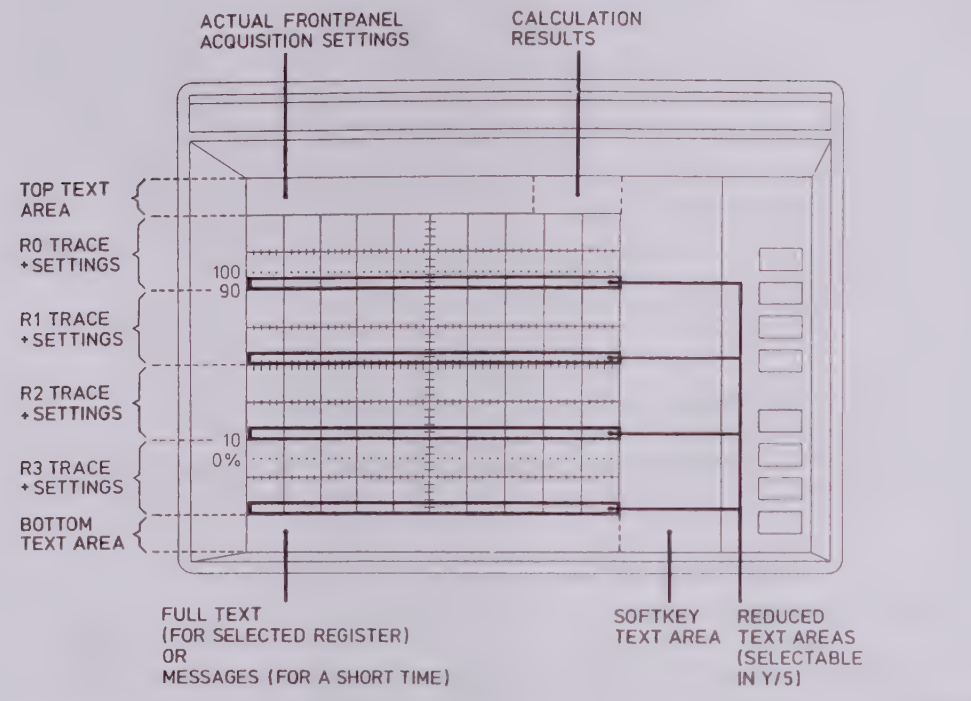


Figure 8.3.1 Screen lay out.

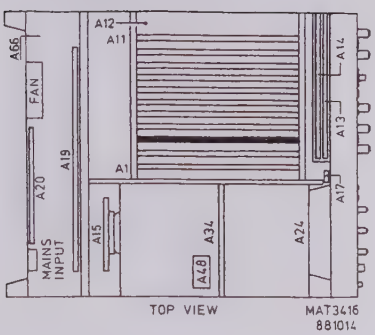
8.3.2.2 Display cycle

During each complete display cycle of about 19 ms the complete contents of the trace memory as well as the text memory is displayed on the C.R.T. screen.

Each display cycle consists of the following display blocks in sequence:

RØ A and/or RØ B	}
R1 A and/or R1 B	} Contents of the
R2 A and/or R2 B	} trace memory
R3 A and/or R3 B	}
TAT	Top text area
RAT RØ	Reduced area text RØ
RAT R1	Reduced area text R1
RAT R2	Reduced area text R2
RAT R3	Reduced area text R3
BAT	Bottom text area
SKT	Softkey area text
MSC	Miscellaneous text (like cursors and channel identification)
PLOT	One dot to plot

UNIT A3 - DISPLAY CONTROL UNIT



CONTENTS

8.3.1 General information..... 8.3-1
8.3.2 Display system and timing..... 8.3-2
8.3.3 Circuit descriptions..... 8.3-7
8.3.4 Signal-name list..... 8.3-12

8.3.1 General information

This unit contains the circuits needed to control the display circuits on units A2 and A4.

It contains the following circuits:

Data buffer
Preset register
Output ports for display parameters
Display address counter
Data buffers for:
- Display address data
- Softkey text data
- Line text data

Timing circuits:
- Synchronization flip flops
- Data acknowledge flip flop
- Start flip flop
- Smooth delay flip flop

Z + interrupt timer
Z - counter
Interrupt counter + interrupt flip flop
Restart counter
Address decoder
Z - detection circuit
Clock-fase generator
Memory select circuit

DATA BUFFER

PRESET REGISTER

DISPLAY ADDRESS COUNTER

HORIZONTAL EXPAND I [PART]

DISPLAY ADDRESS DATA BUFFER

SOFTKEY TEXT DATA BUFFER

LINE TEXT DATA BUFFER

SYNCHRONIZATION FLIP FLOPS

OUTPUT PORTS DISPLAY PARAMETERS

Z-INTERRUPT TIMER

INTERRUPT FLIP-FLOP

DATA ACKNOWLEDGE FLIP-FLOP

START FLIP-FLOP

SMOOTH DELAY FLIP-FLOP

MAT 25 87A

Figure 8.3.8 Unit A3 - DISPLAY CONTROL UNIT - circuit diagram

ADDRESS DECODER

Z-DETECTION

PLOT ONE-SHOT

COPY SYNCHRONIZATION ONE-SHOT

CLOCK-FASE GENERATOR

MEMORY SELECT

REF.NR	TYPE	PEN	Vdd	PEN
D2103,2104,2106,2107,2108	74HCT574	20	0	10
D2158	74 F 32	14	0	7
D2136	74F04	14	0	7
D2156	74HCT174	16	0	8
D2157	74HCT27	14	0	7
D2133	74HCT107	14	0	7
D2147	74 F 32	14	0	7
D2137	74HCT32	14	0	7
D2138	74HCT08	14	0	7
D2111,2117,2113	74HCT191	16	0	8
D2121,2122,2123,2124	74HCT244	20	0	10
D2132	74HCT138	16	0	8
D2131	74HCT139	16	0	8
D2146	74HCT27	14	0	7
D2139,2141	74F109	16	0	8
D2114	74HCT109	16	0	8
D2109	74F04	14	0	7
D2118	74HCT257	16	0	8
D2119	74HCT08	14	0	7
D2143	74HCT00	14	0	7
D2154	74 F00	14	0	7
D2129	74HCT32	14	0	7
D2117	74HCT02	14	0	7
D2116	74HCT74	14	0	7
D2101,2102	74HCT541	20	0	10
D2148	74F74	14	0	7
D2127,2144	74HCT123	16	0	8
D2128	74LS30	14	0	7
D2153	74 F 11	14	0	7
D2126	P8254	24	0	12
D2134	74F163	16	0	8
D2152	74F32	14	0	7
D2142	S155	20	0	10
D2151	S109	28	0	14
D2149	74F08	14	0	7

Figure 8.3.9 Unit A3 - DISPLAY CONTROL UNIT - circuit diagram.

8.4.8 Trigger address comparator

The TRIGGER ADDRESS COMPARATOR is part of the address generator on the DPU CONTROL (Unit A8).
D2022 and D2023 form a 12 bit latch, in which data from the DPU address bus (DUABØØ...11) can be loaded by the DAVA signal. It is reset when the DPU (Unit A9) is reset by RSDU--LT.
The address data from the latch is compared with address data on the DPU address bus by a 12 bit comparator (D2024, D2026 and D2027). When both addresses are the same, the signal OTCM is high. This signal is led to the status multiplexer on unit A8.

8.4.9 Signal name list

UNIT A4

Signal name	Description	Signal source	Signal destination(s)
ABØ1...12	Address bus Ø1...12	A6+option	-
CKSVLA	Clock save latch	A3	-
CLDPAB	Clock display adress bus	A3	-
CLUPAB	Clock microprocessor bus	A3	-
CNCPCN	Count copy address counter	A8	-
CPABØØ...11	Copy counter address bus ØØ...11	A4	A4
CSTR1LLT	Chip select trace 1L	A4	A4
CSTR1HLT	Chip select trace 1H	A4	A4
CSTR2LLT	Chip select trace 2L	A4	A4
CSTR2HLT	Chip select trace 2H	A4	A4
CSTX--LT	Chip select text	A3	-
DAAK--LT	Data acknowledge	A3	-
DAAK--HT	Data acknowledge	A3	-
DAVA	Data valid	A5	-
DBØØ...15	Data bus ØØ...15	A6+option	-
DCDBØØ...15	Display control data bus ØØ...15	A4	A12-A2,A12-A3
DIDBTX	Disable data bus text-buffer	A3	-
DIDCLA	Disable display control latch	A4	-
DISVLA	Disable save latch	A3	-
DITRDB	Disable trace data bus (SARYAKLT)	A3	-
DITXTR	Disable text trace buffer	A3	-
DPABØØ...11	Display address bus ØØ...11	A3	-
DRTXTR	Direction text trace buffer	A3	-
DUABØØ...11	DPU address bus ØØ...11	A8	-
ENCPSA	Enable copy sample	A4	A12-A8
LEDC	Latch enable display control	A3	-
LEDP	Latch enable display	A8	-

8.4.5 Reading trace data for display purposes

The display memory addresses which are needed during the display cycle for trace data are generated by a display address counter which is located on the display control unit A3.

The display counter output address bits DPABØØ ... DPAB11 are applied via address multiplexer I and address multiplexer II to the address inputs of the four display registers RØ, R1, R2 and R3.

Each register can be selected for display by the generation of its chip select signal, its output enable signal and the register select signal TRAB13.
The selected register places its output data word on the trace data bus lines TRDBØØ ... TRDB15. This data is applied to the display control latch by latch enable display control latch signal LEDC.
The output data bits DCDBØØ ... DCDB15 are applied then to the display DAC unit A2 for further handling.

8.4.6 Reading text data for display purposes

The text memory addresses which are needed during the display cycle for text data are generated by the display address counter. These display address counter address bits DPABØØ ... DPAB11 are applied via address multiplexer I to the address inputs of the text memory.
The text memory is selected by the generation of its chip select signal, its output enable signal and the register select signal TXAB13. The text output data word is placed on the text data bus lines TXDBØØ ... TXDB15 and via the text/trace buffer consisting of D2006 and D2007 applied to the display control latch.
The output data bits DCDBØØ ... DCDB15 are applied then to the display DAC unit A2 for further handling.

8.4.7 Data communication via options

Instruments which are equipped with option can communicate with the trace memory as well as the text memory via the following signal paths.

Trace memory:

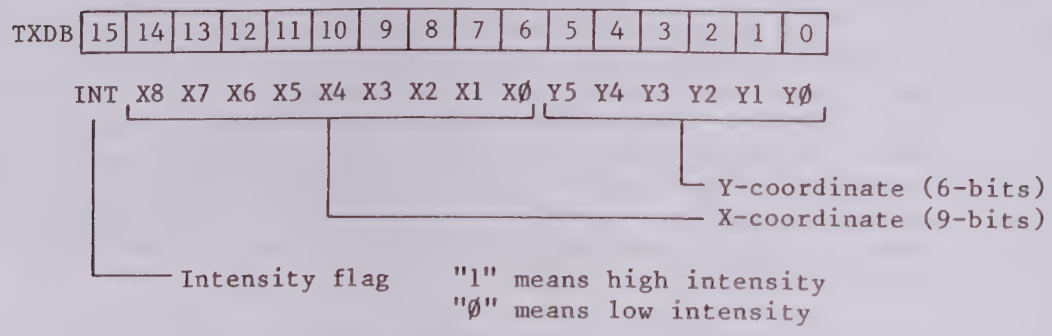
Addresses are generated by the microprocessor and via address multiplexers I and II applied to the display memory.
Data communication is done via the microprocessor data bus, the bidirectional text/trace buffer and the trace data bus or vice versa.

Text memory:

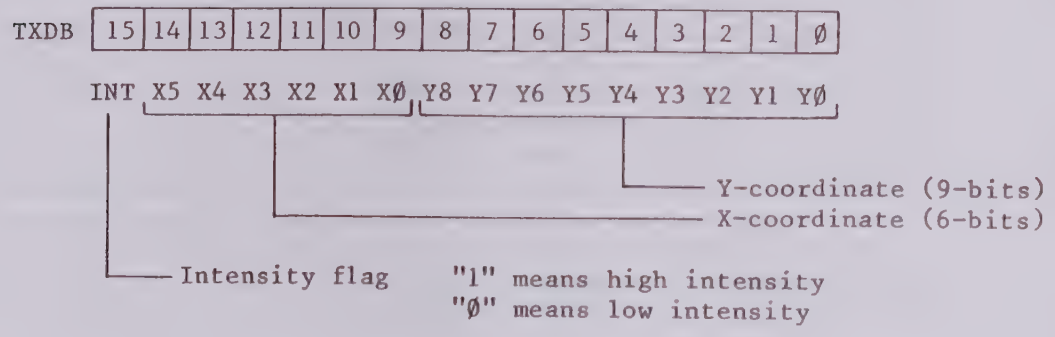
Addresses are generated by the microprocessor and via address multiplexer I applied to the text memory.
Data communication is done via the microprocessor bus, the bidirectional data/text latch and the text data bus or vice versa.

The following text data formats exist:

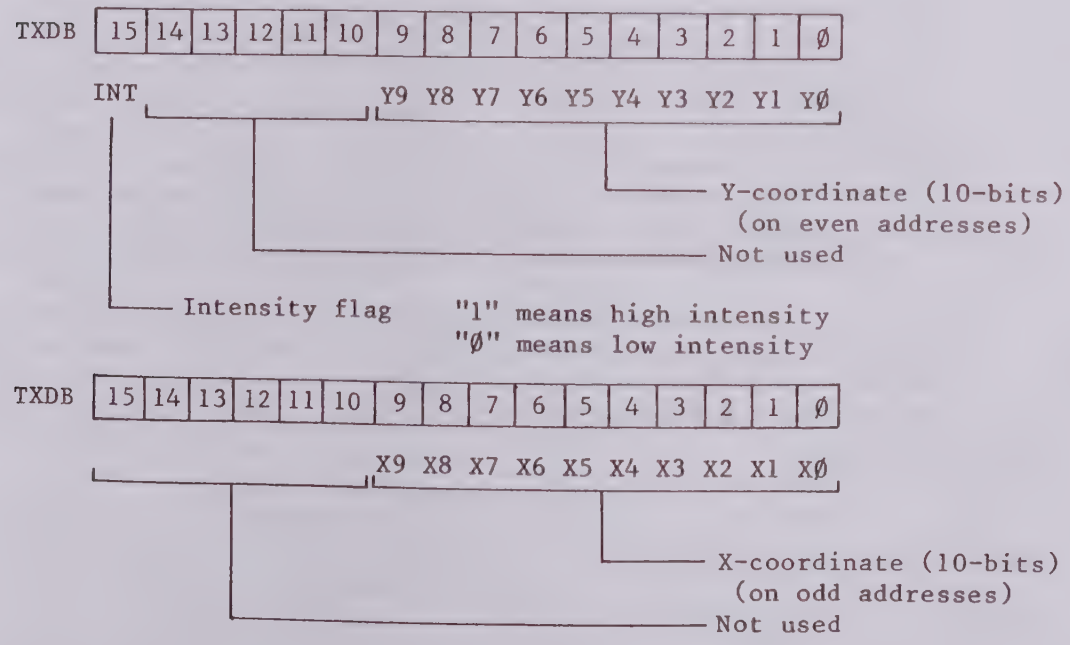
Top area text (TAT)
Trace area text (TRAT)
Bottom area text (BAT)



Softkey text (SKT)



Miscellaneous text (MSC)



For storage of miscellaneous texts, two words are stored, one for the Y-coordinate and the intensity flag and the other one for the X-coordinate.
If no text has to be displayed, a word of only one's will be stored in the text memory and the trace will be suppressed.

8.4.3 Saving trace data from register RØ into one of the registers R1, R2 or R3.

The address information needed for register RØ and the selected register is generated by the display address counter. The address lines DPABØØ ... DPAB11 are applied to the registers RØ, R1, R2 and R3 via address multiplexer I consisting of D2031, D2033, D2032 and D2041 when cycle counter display address bus signal CLDPAB is active and via address multiplexer II consisting of D2037, D2038 and D2039 as TRABØ ... TRAB12 when multiplexed copy address signal MXCPAD is active.

Each trace data word on the register RØ trace data output lines TRDBØØ...TRDB15 is first saved in a save latch consisting of D2028 and D2029 with the clock save latch signal CKSVLA.
The saved word is then afterwards saved in the selected memory by using exactly the same display address. Address line TRAB13 is switched to point to the selected register which is activated via its chip select signal and write enable signal.
The output of the save latch is disabled by the disable save latch signal DISVLA. For the next word the microprocessor increases the address number and so on. After 4096 of these actions the save action is completed. The save latch is not used when data has to be saved in register R2 or R3. Save is then done directly from RØ to R2 and to R3.

8.4.4 Storage of text in the text memory

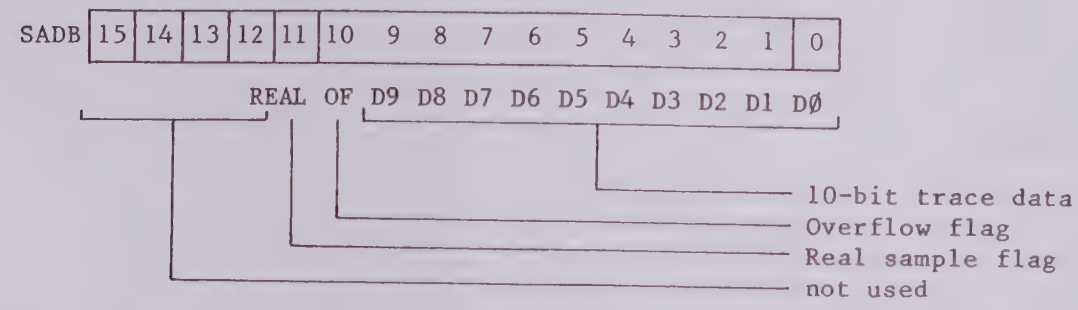
All used kinds of texts are generated by the microprocessor system and stored when they are needed in a 8kx16 bit text memory consisting of D2014 and D2016.
The addresses needed for the storage of text in the text memory are generated by the microprocessor. The microprocessor address lines ABØ1 ... AB12 are applied to the text memory via address multiplexer I consisting of D2031, D2032, D2033 and D2041 as TXABØ1 ... TXAB12.

The text data consists of vertical and horizontal coordinates and an intensity flag. This data is generated by the microprocessor system. The data bits DBØØ ... DB15 are applied via a bidirectional latch consisting of D2003 and D2004 as TXDBØØ ... TXDB15 to the text memory.

8.4.2 Copying trace data from the DPU into display register RØ

On receipt of a trigger pulse, a coupling is realized between the DPU (digital processing unit) and register RØ of the trace memory unit. The DPU places its 12-bit (two - complement) trace data on the sample data bus lines SADBØØ...SADB12. This bus is connected to the trace data latch consisting of D2001 and 2002. Each trace data word is clocked in the latch with signal latch enable display (LEDP). This is done in the rhythm of the acquisition system.

Trace data format:



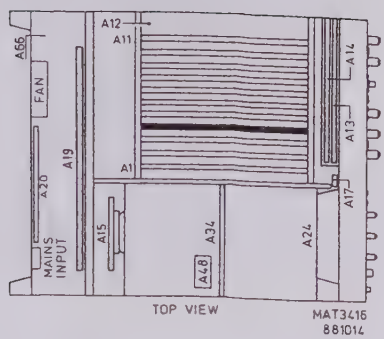
Signal LEDP switches also a handshake flipflop D2017, resulting in an active SARY (sample ready) signal. When the trace data word is copied to register RØ, the SARYAKLT signal resets the handshake flip flop, which informs the DPU that the next trace data word can be sent to the trace data latch.
In this way the display unit is informed that new trace data is available on the output bus lines TRDBØØ ... TRDB15 of the trace data latch. This trace data bus is connected to the four display registers. New trace data however is always stored in register RØ. This is done in a rhythm which is determined by the acquisition system.
RAM's D2008 and D2009 form together the two 4kx16 registers RØ and R1 and D2011 and D2012 form together the two 4kx16 registers R2 and R3.

Addresses for register RØ needed during the copy cycle of trace data from the DPU into register RØ, are generated by a copy address counter which consists of D2018, D2019 and D2021.
The copy counter address bits CPABØØ ... CPAB11 are applied to the trace register RØ via address multiplexer II consisting of D2037, D2038 and D2039 as TRABØ1 ... TRAB12.
Address line TRAB13 us separately generated and is used for the switching between RØ and R1 or between R2 and R3.

The counter is first resetted to its zero state by signal RSDU--LT (reset DPU). After an active trigger the copy cycle is started and the register will be completely filled once with trace data from the acquisition system. The counter is counting (and thus producing addresses for register RØ. CNCPCN pulses (count pulses for the copy address counter) which are generated in the rhythm in which the acquisition system offers the new trace data. At the end of the copy cycle, the counter generates a signal TCCPCN (terminal count copy adress counter) and the cycle is stopped.

Register RØ is furthermore controlled by its chip select signals CSTR1LLT and CSTR1HLT which can only be active when the memory select down signal MYSLDWLT is not active and by the write enable signal WETRØ1LT.

UNIT A4 - DISPLAY MEMORY UNIT



CONTENTS

8.4.1	General information	8.4-1
8.4.2	Copying trace data	8.4-2
8.4.3	Saving trace data	8.4-3
8.4.4	Storage of text	8.4-3
8.4.5	Reading trace data	8.4-5
8.4.6	Reading text data	8.4-5
8.4.7	Data communication via options	8.4-5
8.4.8	Trigger address comparator	8.4-6
8.4.9	Signal name list	8.4-6

8.4.1 General information

This unit basically comprises the four random-access registers RØ, R1, R2 and R3 of the trace memory, the text memory, the copy address counter and their associated control circuits.

Signal-name	Description	Signal source	Signal destination(s)
MXCPAD	Multiplex copy address	A3	-
MYSLDWLT	Memory select down	A6	-
MYSLØ2LT	Memory select Ø2	A6+option	-
OETRØ1LT	Output enable trace Ø1	A3	-
OETRØ2LT	Output enable trace Ø2	A3	-
OETX--LT	Output enable text	A3	-
OFDP	Overflow display	A9	-
OTCM	Output comparator	A4	A12-A8
RDDM--LT	Read display memory	A3	-
RLDP	Real sample display	A9	-
RSDU--LT	Reset DPU	A8	-
SADBØØ...Ø9	Sample data bus ØØ...Ø9	A9+A11	-
SARY	Sample ready	A4	A3
SARYAKLT	Sample ready acknowledge (DITRDB)	A3	-
SLTR1LLT	Select trace 1L	A3	-
SLTR1HLT	Select trace 1H	A3	-
SLTR2LLT	Select trace 2L	A3	-
SLTR2HLT	Select trace 2H	A3	-
TCCPCN	Terminal count copy address counter	A4	A12-A8
TRABØ1...12	Trace address bus Ø1...12	A4	A4
TRAB13	Trace address bus 13	A3	-
TRDBØØ...15	Trace data bus ØØ...15	A4	A4
TXABØ1...12	Text address bus ØØ...12	A4	A4
TXAB13	Text address bus 13	A3	-
TXDBØØ...15	Text data bus ØØ...15	A4	A4
UPCKØ8	Microprocessor clock 8 MHz	A6	-
WETRØ1LT	Write enable trace Ø1	A3	-
WETRØ2LT	Write enable trace Ø2	A3	-
WETX--LT	Write enable text	A3	-

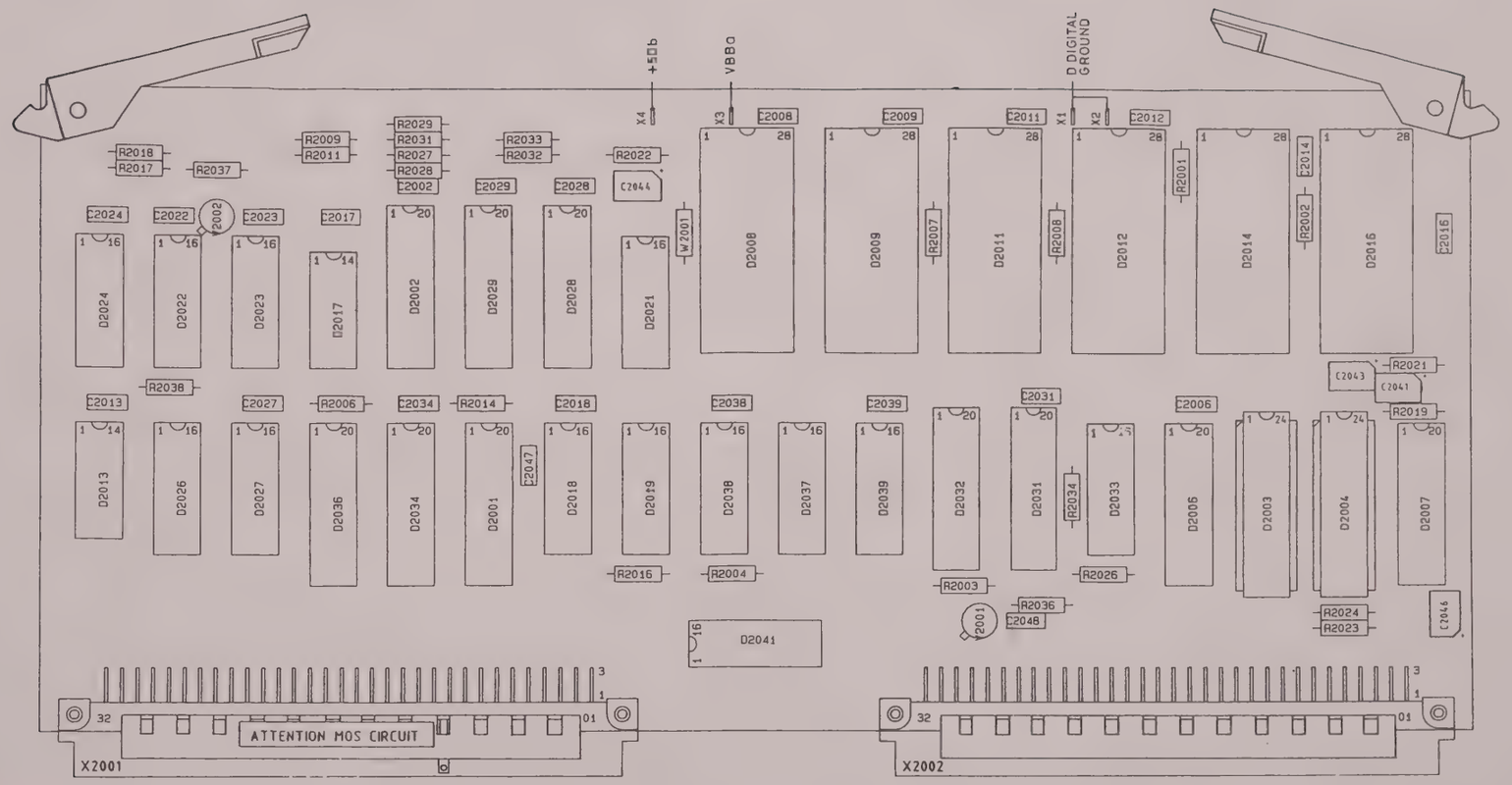


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Figure 8.4.1 Unit A4 - DISPLAY MEMORY UNIT - p.c.b. lay-out.

TRACE MEMORY

R0 - R1

R2 - R3

SAVE LATCH

DISPLAY CONTROL LATCH

TRACE DATA LATCH

CHIP SELECT

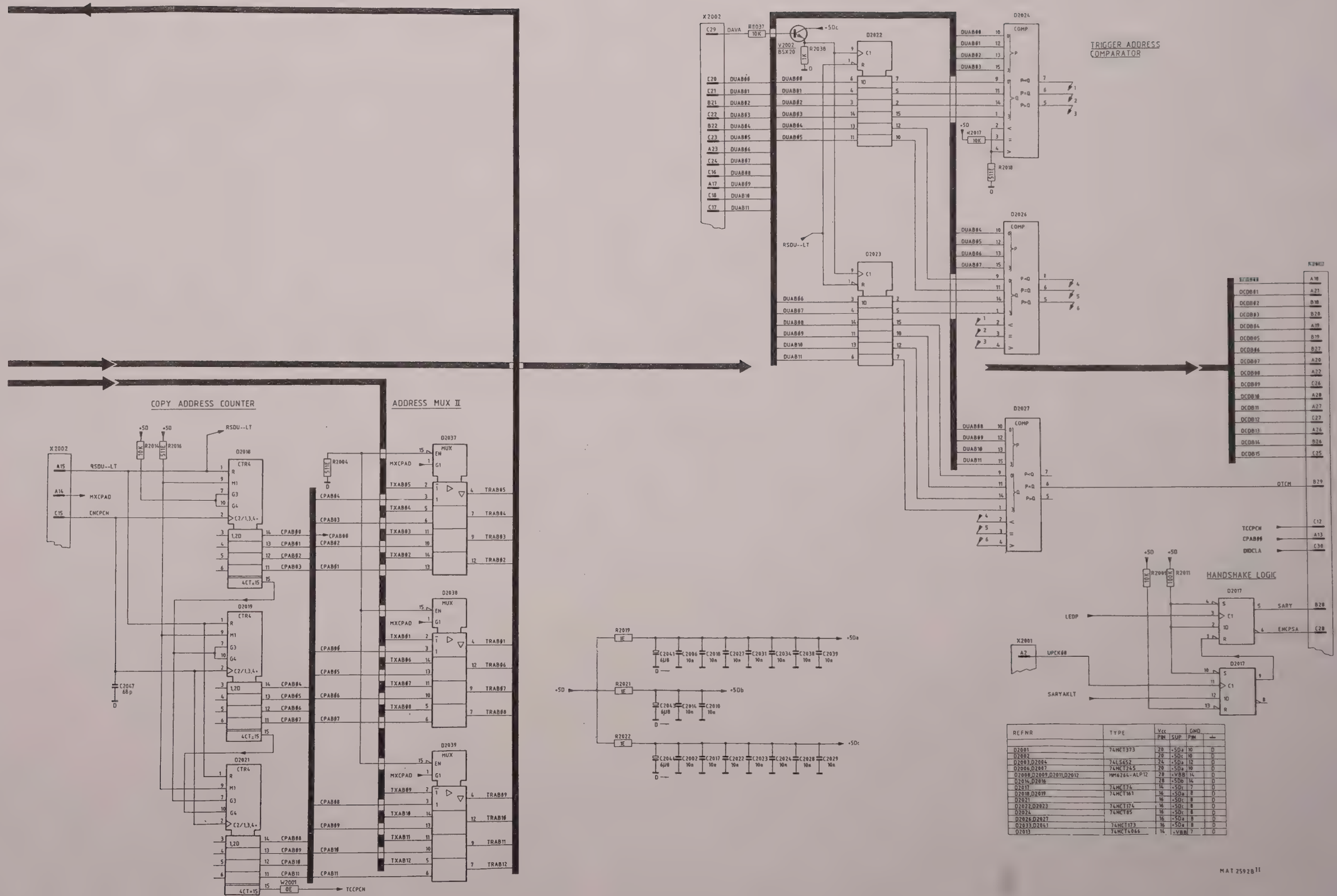
DATA/TEXT BIDIRECTIONAL LATCH

TEXT/TRACE BIDIRECTIONAL BUFFER

ADDRESS MUX I

TEXT MEMORY

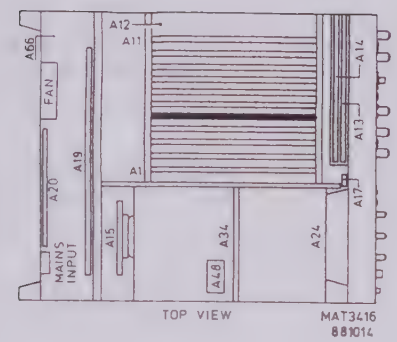
MAT 2592A



REFNR	TYPE	Vcc PIN	Vcc SUP	GND PIN	GND
D2001	74HCT373	20	+5Da	10	0
D2002		20	+5Dc	10	0
D2003,D2004	74LS652	24	+5Da	12	0
D2006,D2007	74HCT245	20	+5Da	10	0
D2008,D2009,D2011,D2012	MM6264-ALP12	28	+VBB	14	0
D2014,D2016		28	+5Db	14	0
D2017	74HCT74	14	+5Dc	7	0
D2018,D2019	74HCT161	16	+5Da	8	0
D2021		16	+5Dc	8	0
D2022,D2023	74HCT174	16	+5Dc	8	0
D2024	74HCT85	16	+5Dc	8	0
D2026,D2027		16	+5Da	8	0
D2033,D2041	74HCT173	16	+5Da	8	0
D2013	74HCT4066	14	+VBB	7	0

Figure 8.4.3 Unit A4 - DISPLAY MEMORY UNIT - circuit diagram.

UNIT A5 - MRAM UNIT



CONTENTS

8.5.1 General information..... 8.5-1
8.5.2 Memory circuit..... 8.5-1
8.5.3 ACL circuit..... 8.5-2
8.5.4 Signal name list..... 8.5-4

8.5.1 General information

This unit basically consists of the microprocessor memory circuit (RAM) and the acquisition control logic (ACL).

8.5.2 Memory circuit

The microprocessor memory circuit consists of a RAM and some control logic.

The RAM consists of RAM Ø (D1834 and D1836), which is backed up by the battery, and RAM 1 (D1837 and D1838). All devices are 32 kbyte types. If 8 kbyte types are used for D1834 and D1836, then soldering joint J1801 should be changed over.

The ADDRESS REGISTER latches the data of the microprocessor address lines. It is clocked by CKAB--HT, which is active when addresses on the address bus are stable.

The BIDIRECTIONAL DATA buffer buffers the data lines to the microprocessor. It is enabled by CKAB--LT. The direction of data transfer is determined by RARD--LT.

The SELECT LOGIC generates the RAM select signals.
When the power goes down, MYSLDWLT goes low. Now D1833 separates SLØØLOLT and SLØØHILT from the select logic and so they go to VBBa level. The RAMs (only RAM Ø) are deselected, their contents remain.

The remaining select logic generates delayed CKAB signals and DATRAKLT, when this unit is selected.
The delay of the CKAB signals (R1802 and C1851) ensures stable data on the address bus and the data bus when they are clocked in.
The delay of DATRAKLT (R1839 and C1852) ensures enough data setup time for the RAM.

8.5.3 ACL circuit

The ACL circuit consists of the following parts:

- Mode register
- Slow clock generator
- Slow time base logic
- Acquisition control logic
- Shift logic

The MODE REGISTER latches and decodes data from the microprocessor, which are used to control the slow time base logic, the acquisition control logic and the shift logic.

The SLOW CLOCK GENERATOR generates signals, which are used in slow time base modes. These signals are derived from UPCK16, the 16 MHz microprocessor clock. The generated signals are:

Name	Frequency
CKCDOC	16 MHz
TBCKØ8	8 MHz
CKSWTB	1,6 MHz
CK16ØØ	1,6 MHz

The SLOW TIME BASE LOGIC consists of D1801, D1821, D1803 and D1811. It generates various control signals which are used in the slow time base modes.
These are the modes in the time base range500 us/div...360 s/div and the read out cycles of the P^2CCD mode and the random sampling mode.
D1801 is a triple programmable counter; the time base counter.
Counter 1 and counter 2 are cascaded to achieve a dividing range which is big enough to divide the CKSWTB signal down to the desired frequency at the time base setting 360 s/div. The divide ratio is determined by RADBØØ...RADBØ7, which come from the microprocessor.
The output of counter 2 is led to pin 2 of D1811, where it is latched with various other control signals, which may arrive at slightly different times, due to propagation delay times.
At the output of D1811 all signals are available at the same moment.
Counter 3 in D1801 counts down the filling of the P^2CCD with samples, when a new time base setting is selected. When the P^2CCD is filled, a clock is given to pin 11 of D1821, which activates ENSWTB.
The counter is a mono stable count down counter, which is triggered by the RSTB--LT signal.
IC D1803 is an FPLS (Field Programmable Logic Sequencer) that generates 4 acquisition control signals, depending on the selected time base mode.
The ENSWTB signals enables the output signals.
SYSWTBØ1 is a 1,25 us long clock pulse at the falling edge of SWTB.
TKSAØ2 is a 2,5 us long clock pulse at the falling edge of SWTB.
RSMNØ1 and RSMXØ1 are used for the generation of reset pulses on unit A49 for the peak detectors on unit A33. They are only present when MIN / MAX is on.
When an external clock is selected (SLETCK) the external clock (ETCK) is synchronised with SCEVØ1 by D1803.

The ACQUISITION CONTROL LOGIC consists of an FPLS (D1804), a latch (D1822) and a triple programmable counter; the ACL counter (D1802). The counter and the FPLS together generate a number of control signals, depending on the selected time base mode. They are buffered by D1822.

The SHIFT LOGIC generates a TKSA signal for the DPU when a sample, that has to be used, leaves the P^2CCD (see figure 8.5.1).

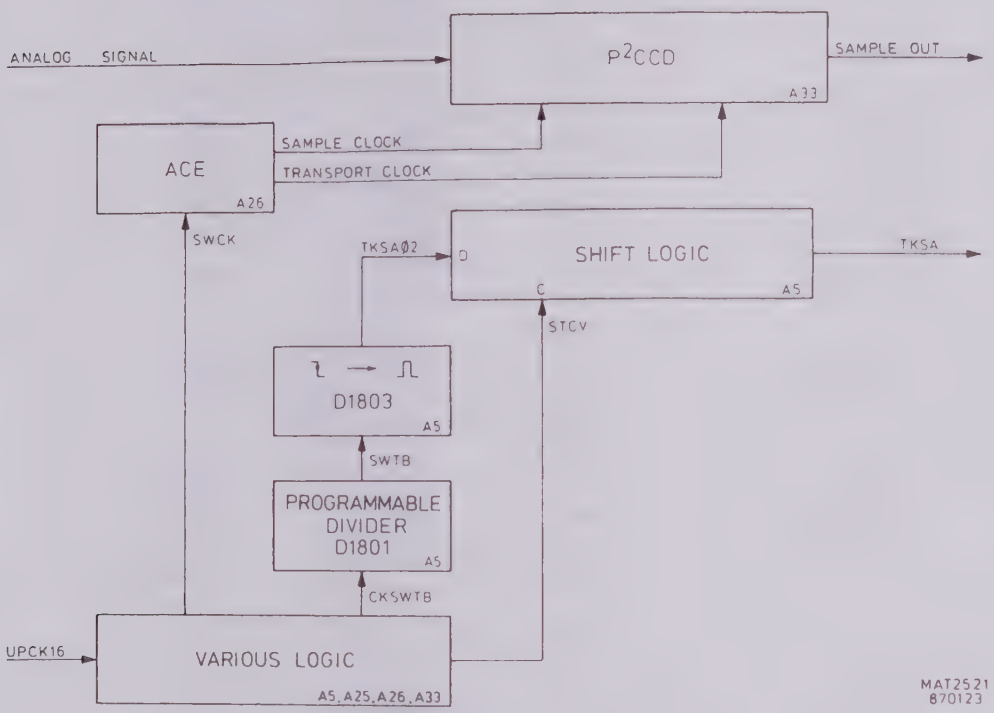


Figure 8.5.1 SHIFT LOGIC

In Direct mode Single channel, the frequency of the sample clock and the transport clock is 400 kHz. So every 2,5 us a sample is taken and transported.
At a time base setting of 100 ms/div every 250 us a sample is used to be displayed (100 ms x 10 div/4K samples). So only 1 of 100 samples is used.
The moments on which a sample is taken, that is to be displayed later, is marked by TKSAØ2, which is derived from SWTB. As the sample is transported through the P^2CCD, TKSAØ2 is synchronously shifted through the SHIFT LOGIC under control of the STCV signal.
When the sample shifts out of P^2CCD the TKSØ2 signal, which is now called TKSA, shifts out the shift logic.

The shift logic consists of IC's D1812...1814 and D1816...1819. D1813 is a quadruple 64-stage shift register, which is connected in cascade to obtain a 256-stage shift register. The number of stages is extended by D1814.
The shift register is clocked by STCV--LT. TKSAØ2 at pin 9 determines wether a "1" or a "Ø" shifts in the register.
D1816 is used to delay some signals and to synchronize them on STCV--LT.
D1817 and D1818 form together a multiplexer, which selects the correct signal in the various modes (TKSAØ1).
D1819 latches TKSAØ1 together with some other signals to offer them

8.5.4 Signal name list

UNIT A5

Signal name	Description	Signal source	Signal destination(s)
ABØ1...16	Address bus Ø1...16	A6+option	-
AB19	Address bus 19	A6	-
CD	P^2CCD mode	A5	A5
CDRD	P^2CCD read	A25	-
CDRDØ1	P^2CCD read Ø1	A5	A5
CDRD-2	P^2CCD read 2	A26	-
CHPT	Channel pointer	A5	A12-A8
CHPTØ1	Channel pointer Ø1	A33	-
CK16ØØ	Clock 1,6 MHz	A5	A12-A25
CKAB--HT	Clock address bus	A5	A5
CKAB--LT	Clock address bus	A5	A5
CKCDOC	Clock P^2CCD output control	A5	A12-A25
CKSWTB	Clock slow time base	A5	A5
CSALCNLT	Chip select ACL counter	A5	A5
CSTBCNLT	Chip select time base counter	A5	A5
DAHISBLT	Data high strobe	A6+option	-
DALOSBLT	Data low strobe	A6+option	-
DATRAKLT	Data transfer acknowledge	A3+A5+A6+A8 +option	A12-A6, A12-option
DAVA	Data valid	A5	A12-A8, A12-A4
DAVAØ1	Data valid Ø1	A5	A5
DAVA--LT	Data valid	A5	A5
DBØØ...15	Data bus ØØ...15	A6;option	-
DS	Direct special mode	A5	A5
DUAL	A and B mode	A5	A5
ENDBBFLT	Enable data bus buffer	A5	A5
ENSWTB	Enable slow time base	A5	A5
ENSWTBLT	Enable slow time base	A5	A5
ETCK	External clock	A25	-
ETCKØ1	External clock Ø1	A5	A5
HDOF--LT	Hold off	A5	A12-A25-A26
IOSLØ8LT	I/O Select Ø8	A6	-
MM	Min/max mode	A5	A5
MMPT	Min/max pointer	A5	A12-A8
MMPTØ1	Min/max pointer Ø1	A33	-
MMPTØ2	Min/max pointer Ø2	A5	A5
MYSLDWLT	Memory select down	A6	-
MYSLØ1LT	Memory select Ø1	A6	-
RAABØ1...16	RAM address bus Ø1...16	A5	A5
RAAB19	RAM address bus 19	A5	A5
RADBØØ...15	RAM data bus ØØ...15	A5	A5
RARD--LT	RAM read	A5	A5
RAWR--LT	RAM write	A5	A5

Signal name	Description	Signal source	Signal destination(s)
ROMN	Roll mode manual	A5	A5
RSMO	Random sampling mode	A5	A5
RSMN	Reset min	A5	A12-A25-A26-A49
RSMNØ1	Reset min Ø1	A5	A5
RSMX	Reset max	A5	A12-A25-A26-A49
RSMXØ1	Reset max Ø1	A5	A5
RSSW	Reset slow	A5	A12-A25-A26
RSTB--LT	Reset time base	A5	A5
SCEVØ1	Sample clock even Ø1	A5	A5
SCEV--HT	Sample clock even	A25	-
SLETCK	Select external clock	A5	A5
SLØØHILT	Select ram ØØ high byte	A5	A5
SLØØLOLT	Select ram ØØ low byte	A5	A5
SLØ1HILT	Select ram Ø1 high byte	A5	A5
SLØ1LOLT	Select ram Ø1 low byte	A5	A5
STCV	Start conversion	A33	-
STDAVA	Set data valid	A5	A5
STSW	Set slow	A5	A12-A25-A26
SWCK--LT	Slow clock	A5	A5
SWCKØ1	Slow clock Ø1	A25	-
SWCKØ2	Slow clock Ø2	A5	A5
SWTB	Slow time base	A5	A5
SYSWTB	Synchronised slow time base	A5	A12-A25-A26-A49
SYSWTBØ1	Synchronised slow time base Ø1	A5	A5
TBCKØ8	Time base clock 8 MHz	A5	A5
TC1...3	Timer counter 1...3	A5	A5
TCEVØ1	Transport clock even Ø1	A5	A5
TCEV--LT	Transport clock even	A25	-
TDLD	Trigger delay load	A5	A12-A25-A26
TDUF	Trigger delay underflow	A25	-
TDUFØ1	Trigger delay underflow Ø1	A5	A5
TKSA	Take sample	A5	A12-A8
TKSAØ1	Take sample Ø1	A5	A5
TKSAØ2	Take sample Ø2	A5	A5
TRRY	Transfer ready	A8	-
UPCK16	Microprocessor clock 16 MHz	A6	-
UPRD--LT	Microprocessor read	A6	-
UPWR--LT	Microprocessor write	A6	-
VBB	Voltage battery backup	A6	-
VBBa	Voltage battery backup a	A5	A5
ZECH	Zero channel	A5	A12-A25-A33

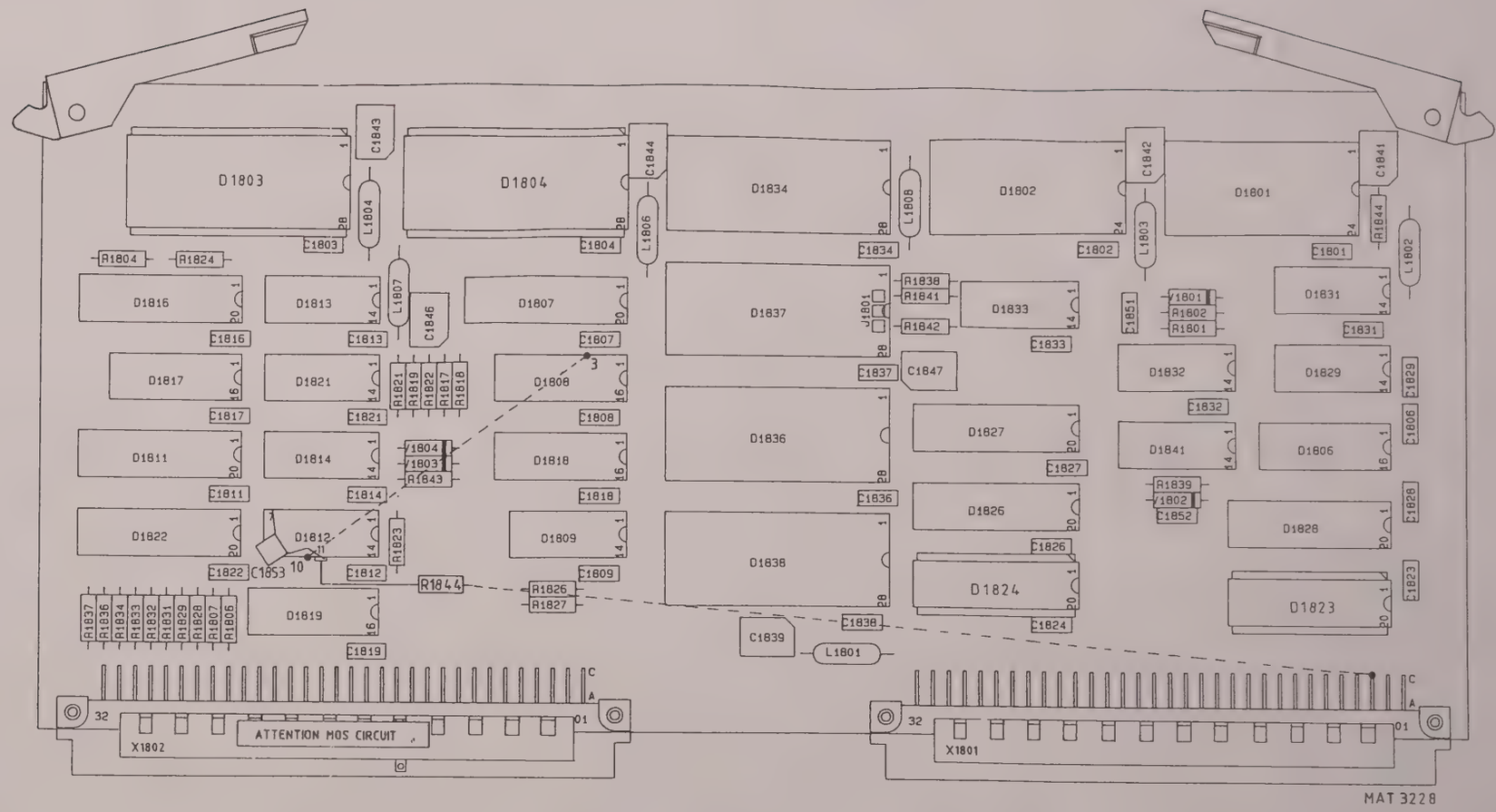


Figure 8.5.2 Unit A5 - MRAM UNIT - p.c.b. lay-out.

ROM 0

ROM 2

ADDRESS BUFFER

BIDIRECTIONAL DATA BUFFER

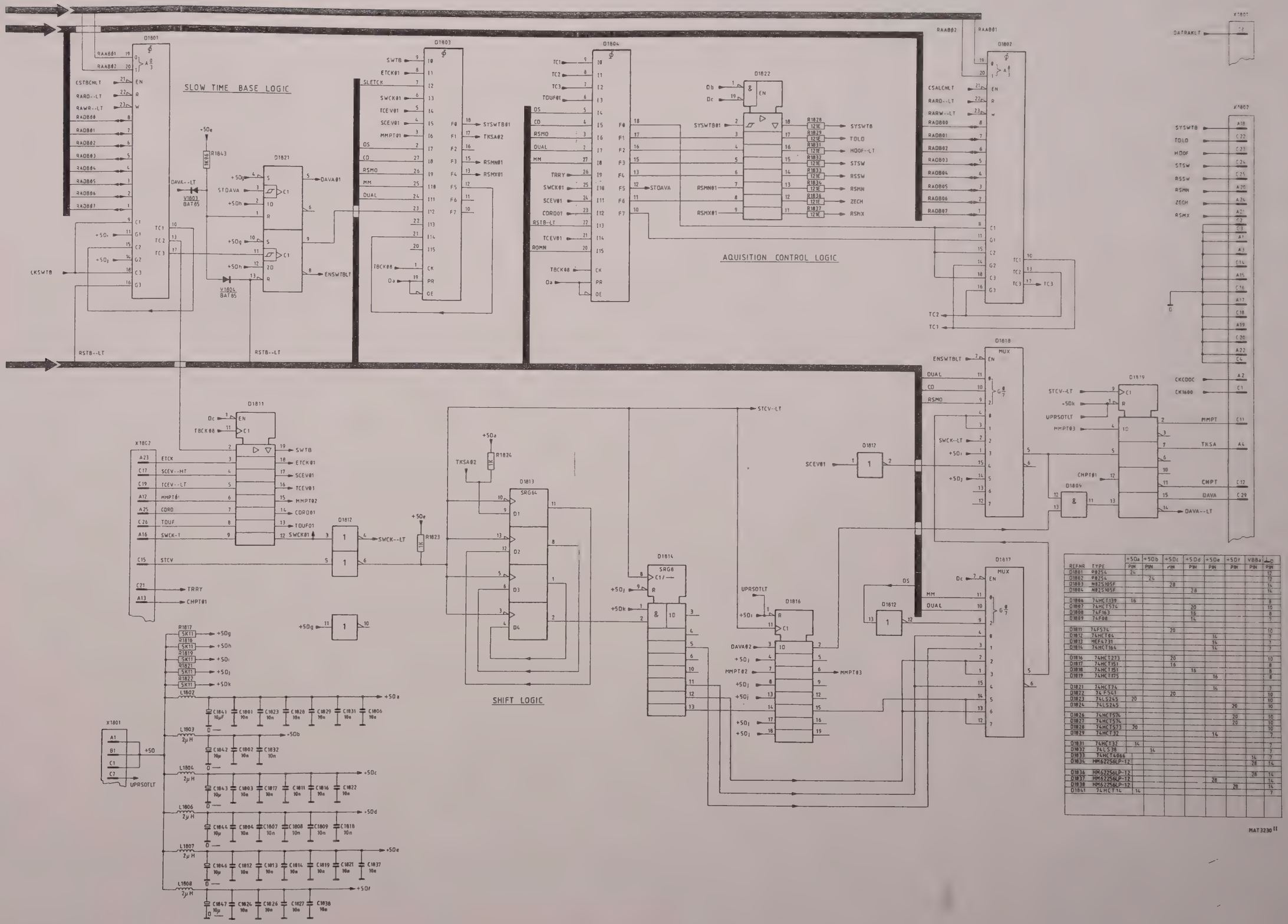
BUFFER

SELECT LOGIC

MODE REGISTER

SLOW CLOCK GENERATOR

Figure 8.5.3 Unit A5 - MRAM UNIT - circuit diagram



REFNR	TYPE	+5Oa PIN	+5Ob PIN	+5Oc PIN	+5Od PIN	+5Oe PIN	+5Of PIN	VBBa PIN	⊥0 PIN
D1801	P8754	24							12
D1802	P8254		24						12
D1803	M82S105F			28					14
D1804	M82S105F				28				14
D1806	74HCT139	16							8
D1807	74HCT574				20				10
D1808	74F163				16				8
D1809	74F08				14				7
D1811	74F574			20					10
D1812	74HCT86					14			7
D1813	MC4731					14			7
D1814	74HCT164					14			7
D1816	74HCT273			20					10
D1817	74HCT151			16					8
D1818	74HCT151				16				8
D1819	74HCT155					16			8
D1821	74HCT74					14			7
D1822	74F541			20					10
D1823	74LS245	20							10
D1824	74LS245						20		10
D1826	74HCT574						20		10
D1827	74HCT574						20		10
D1828	74HCT573	20							10
D1829	74HCT32					14			7
D1831	74HC132	14							7
D1832	74LS38		14						7
D1833	74HCT4066							14	7
D1834	MM62256LP-12							28	14
D1836	MM62256LP-12							28	14
D1837	MM62256LP-12					28			14
D1838	MM62256LP-12						28		14
D1841	74HCT74	14							7

Figure 8.5.4 Unit A5 - MRAM UNIT - circuit diagram.

Signal name	Description	Signal source	Signal destination(s)
RQCL	Request clock	A6	A6
SLBUENLT	Select bus enable	A6	A6
SLRØØ	Select ROM Ø	A6	A6
SLRO1	Select ROM 1	A6	A6
TCRS--LT	TIC reset	A6	A6
TIC	Timer interrupt clock	A6	A6
TSLMA-LT	Timing slave to master	A6	A6
UPABØ1...23	Microprocessor address bus Ø1...23	A6	A6
UPADSBHT	Microprocessor address strobe	A6	A6
UPADSBLT	Microprocessor address strobe	A6	A6
UPCK	Microprocessor clock	A6	A6
UPCKØ8	Microprocessor clock 8 MHz	A6	A12-A4,A12-A8,A12-option A12-A3,A12-A9
UPCK16	Microprocessor clock 16 MHz	A6	A12-A5 A12-A8 A12-A11
UPDASBLT	Upper data strobe	A6	A6
UPDBØØ...15	Microprocessor data bus ØØ...15	A6	A6
UPHA--LT	Microprocessor halt	A6	A6
UPIN--HT	Microprocessor input port	A6	A6
UPOT--HT	Microprocessor output port	A6	A6
UPRD--LT	Microprocessor read	A6	General
UPRDWR	Microprocessor read/write	A6	General
UPRSOTLT	Microprocessor reset out	A6	A12-A3,A12-option
UPWR--LT	Microprocessor write	A6	General
VAPEADLT	Valid peripheral address	A6	A6
VAPESLLT	Valid peripheral select	A6	A6
VBB	Voltage battery backup	A6	A12-A5,A12-option
WD----LT	Watch dog	A6+option	A6
WRSB--LT	Write strobe	A6	A6
Z-MO--XT	Z-modulation	A6	A12-A1

8.6.5 Signal name list

UNIT A6

Signal name	Description	Signal source	Signal destination(s)
ABØ1...2Ø	Address bus Ø1...2Ø	A6+option	General
ABBUENLT	Address bus enable	A6	A6
BAST	Battery status	A6	A6
BATS	Battery test	A6	A6
BAVO	Battery voltage	A66	-
BSBU--LT	Bus busy	A6+option	A6,option
BSGROTHT	Bus grant output	A6	Option (1)
BSRQ--LT	Bus request	A6+option	A6,option
CLWR--LT	Clocked write	A6	A6
DAAK--LT	Data acknowledge	A6	A6
DAAKBSLT	Data acknowledge bus	A6	A6
DAHISBLT	Data high strobe	A6+option	A12-A3,A12-A5
DALOSBLT	Data low strobe	A6+option	A12-A3,A12-A5
DASB--HT	Data strobe	A6	A6
DATRAKLT	Data transfer acknowledge	A3+A5+A6+A8 +option	A6,option
DBØØ...15	Data bus ØØ...15	A6+option	General
ENAD--LT	Enable address	A6	A6
FCØ...2	Function code Ø...2	A6	A6
ILØ1--LT	Interrupt level Ø1	A6	A6
ILØ2--LT	Interrupt level Ø2	A8	-
ILØ3--LT	Interrupt level Ø3	A14	-
ILØ4--LT	Interrupt level Ø4	Option	-
ILØ5--LT	Interrupt level Ø5	A3	-
ILØ6--LT	Interrupt level Ø6	A25	-
ILØ7--LT	Interrupt level Ø7	A20	-
IPLØ...2	Interrupt priority level Ø...2	A6	A6
IOSLØ3LT	I/O Select Ø3	A6	A12-Option
IOSLØ4LT	I/O Select Ø4	A6	A12-A14
IOSLØ5LT	I/O Select Ø5	A6	A12-A3
IOSLØ6LT	I/O Select Ø6	A6	A12-A25-A26
IOSLØ7LT	I/O Select Ø7	A6	A12-A25
IOSLØ8LT	I/O Select Ø8	A6	A12-A5
IOSLØ9LT	I/O Select Ø9	A6	A12-Option
IOSL1ØLT	I/O Select 1Ø	A6	A12-Option
LODASBLT	Lower data strobe	A6	A6
MASL--LT	Master selected	A6+option	A6,option
MYSLØ1LT	Memory select Ø1	A6+option	A12-A5
MYSLØ2LT	Memory select Ø2	A6+option	A12-A3,A12-A4
MYSLØ3LT	Memory select Ø3	A6	A12-A8
MYSLØ4LT	Memory select Ø4	A6	A12-Option
MYSLALHT	Memory select all	A6	A6
MYSLALLT	Memory select all	A6	A6
MYSLDWLT	Memory select down	A6	A12-A4,A12-A5,A12-option
RDRO	Read ROM	A6	A6
RDSB--LT	Read strobe	A6	A6

(1) Becomes BSGRINHT on option.

The INPUT PORT enables the microprocessor to read the status of 3 service switches and the status of the battery.
Service switch X1703 should always be open in this instrument.
Service switches X1704 and X1706 have functions for the diagnostic software (see section 11.4.4).

Via the OUTPUT PORT, the microprocessor generates the watchdog signal WD----LT with the open collector gate D1714. The battery test circuit is also controlled via the output port.

The SUPPLY VOLTAGE SWITCH switches +5D off, when this voltage is too low.
When the power is on, +5D supplies the memories via V1712 and charges the batteries via R1715.
When +5D goes low as the instrument is switched off, V1711 and V1712 block, which prevents that the batteries supply back to +5D.
Now the memories are supplied by the batteries via V1707 and R1715.
V1708 will also block and MYSLDWLT will go down, which will deselect the memories. Their contents will remain.

The BATTERY TEST circuit loads the battery via V1702 and R1712, when the condition of the battery has to be tested after a (re)start of the microprocessor. Because of feedback from +5D via R1715 this circuit is of no use in this instrument. It is present for compatibility with other instruments in which this board is used together with normal (non rechargeable) batteries. In that case R1715 is not present and diode V1707 prevents the batteries from being charged from +5D.

The COMPARATOR compares the battery voltage with a reference voltage from V1701. When the battery voltage is too low, BAST goes high, which is read by the microprocessor via the input port.
When rechargeable batteries are used, the battery voltage should not be too low, due to the feedback via R1715, unless one of the batteries is broken.

The CLOCK GENERATOR consists of a compact integrated crystal oscillator of 16 MHz (G1701) and a number of divider stages. The table below gives the frequency of the generated signals.

Name	Frequency
UPCK16	16 MHz
UPCKØ8	8 MHz
UPCK	8 MHz
Z-MO-XT	200 kHz
TIC	25 Hz

By changing over soldering joint J1707 all frequencies are divided by 2. This can be used to detect access time problems.

The INTERRUPT PRIORITY LEVEL ENCODER (D1708) encodes 7 offered interrupt levels to a 3 bit binary code (IPLØ...2), which is applied to the microprocessor. A reaction of the microprocessor on ILØ1--LT might be postponed a while, because interrupts with a higher priority are present. Now flipflop D1704 keeps ILØ1--LT low, when TIC goes high after 20 ms. When the interrupt is acknowledged the flipflop is reset by TCRS--LT.
Gate D1739 is a buffer between the HCT logic on unit A3 and the LS TTL logic of D1708.
ILØ7--LT (power down) is also routed to the reset/halt logic, to halt the microprocessor.

The WATCHDOG consists of a retriggerable monostable multivibrator (D1709), an oscillator (D1712) and the reset/halt logic.
When the microprocessor program runs normally, the multivibrator is retriggered within every 2 seconds by WD----LT. This keeps pin 12 of D2709 low. Via D1712 UPRSOTLT and UPHA--LT stay high.
When another microprocessor has taken over control over the system, WD----LT is generated by this microprocessor.
If the WD----LT signal does not come within 2 seconds (e.g. due to an abnormal program sequence) pin 12 of D1709 goes high. Now the microprocessor is halted by UPHA--LT and the hardware is reset by UPRSOTLT.
The gate of D1712 pins 1, 2 and 3 forms an oscillator, so after about 2 seconds UPHA--LT and UPRSOTLT become inactive. The microprocessor will restart, generate the WD----LT signal and so on.
If for some reason the microprocessor should not restart correctly the oscillator of D1712 gives a halt plus reset after 2 seconds and after another 2 seconds the microprocessor can restart again. The strap X1708 allows disabling of the watchdog, which is used for the diagnostic software (see section 11.4).
A start of the microprocessor and a restart caused by the watchdog initiates the power up routine (see section 11.4).
If the power goes down ILØ7--LT halts the microprocessor via pin 5 of D1712. Capacitor C1753 keeps ILØ7--LT long enough low at power up, to be sure that all supply voltages are present when the microprocessor starts.
The signal ILØ7--LT is also connected to testpoint X1713, which is located next to ground testpoint X1714.
By interconnecting these testpoints the microprocessor can be restarted.

8.6.4 Circuit description

The MICROPROCESSOR (D1717) is connected via the microprocessor data bus to the BIDIRECTIONAL DATA BUS BUFFER and to ROMØ and ROM1.
ROMØ and ROM1 consists each of two 128K x 8 ROMS, together forming two 128K x 16 ROMs.
If software releases with 64K x 8 ROMS are used, then the soldering joints J1701 and J1702 should be changed over.
The ROMs are addressed via the microprocessor address bus. This bus is buffered to the other units by the ADDRESS BUS BUFFER.
The circuit consisting of D1737, D1741 and D1747 generate the memory select signals and some strobe signals.
The circuit consisting of D1744 and D1746 generate the I/O select signals. Via D1743 and D1714 DATRAKLT goes down with a short delay as one of the I/O select signals goes down.
DATRAKLT can also be pulled down by circuits on other units via pin C8 on connector X1701 and the service switch X1707. This switch can be changed over to generate a data transfer acknowledge by the SLBUENLT signal, which is used by the diagnostic software (see chapter 11.4.4).
The circuit around D1741 generates ROM select signals and some other control signals.
The 3 function control signals are applied to a gate in D1737, which detects the interrupt acknowledge status of the microprocessor, when all function code signals are high. This is used to generate VAPEADLT and memory select control signals.
The monostable multivibrator D1709 keeps the bus busy signal a while active, after the microprocessor has accessed the display RAM. This prevents other microprocessors on options to take over the bus, when the microprocessor has transferred data to the display memory, to assure enough time for the display memory control logic to write the data in the display memory (unit A4).

The BUS ARBITER

The BUS ARBITER consists of a dedicated IC (D1731) and associated logic.
It's main function is to assign control of the microprocessor busses to the microprocessor that claims the control.
When no options are installed in the instrument there is only one microprocessor, so the bus arbiter has no real arbiter function.
If UPAB23 at D1734 pin 13 goes high, then RQCL to the BUS ARBITER goes high. Now the BUS ARBITER circuit makes ABBUENLT and SLBUENLT low, which enables all buffers to the CCU-bus. This enables the microprocessor to access memory and I/O ports on other units via the CCU-bus.
The BUS ARBITER circuit is reset by the microprocessor reset signal (UPRSOTLT) from the RESET/HALT logic.
The capacitors C1754...C1761 and resistor network R1726 give delay times, which time the taking over of the microprocessor busses by another microprocessor.

The associated logic generates a number of control signals for the arbiter function as well as for normal microprocessor functions. The shift register D1748 generates the CLWR--LT signal that lies with its edges between the edges of one of the memory select signals. So first the memory select signal goes down, next the CLWR--LT pulse and UPWR--LT pulse at D1721 come and finally the memory select signal goes high.

A number of I/O select signals select address ranges in the I/O part of the memory map, according to the following table:

Select signal	Selected address range	Used for
IOSLØ3LT	C00000-C1FFFFF	Option
IOSLØ4LT	C20000-C3FFFFF	Front units A13 + A14
IOSLØ5LT	C40000-C5FFFFF	Display unit A3
IOSLØ6LT	C60000-C7FFFFF	CCD logic unit A26
IOSLØ7LT	C80000-C9FFFFF	Management unit A25
IOSLØ8LT	CA0000-CBFFFFF	A.C.L. part unit A5
IOSLØ9LT	CC0000-CDFFFFF	Not used
IOSL1ØLT	CE0000-CFFFFFF	Option

The data acknowledge signal for the microprocessor is generated on this unit (A6) when an I/O select signal is active.When a memory select signal is active the data acknowledge signal is generated on the selected unit via a wired or open collector circuit (DATRAKLT).

8.6.3 Interrupts

Peripheral circuits can generate an interrupt to the microprocessor to ask for special actions. Each interrupt has a priority level according to the table below. The higher the interrupt number is, the higher it's priority level is. Interrupts with a priority level which is lower than or equal to the priority level of the currently being handled interrupt are inhibited, until the higher priority level interrupt is handled.

Interrupt signal	Comes from
ILØ1--LT	Microprocessor unit A6
ILØ2--LT	DPU unit A9
ILØ3--LT	Front unit A14
ILØ4--LT	Option
ILØ5--LT	Display unit A3
ILØ6--LT	Management unit A25
ILØ7--LT	Power 2 unit A20

The functions of the interrupts are:

ILØ1--LT Comes every 40 ms. It starts a scan of the front panel keys and updates the status of the pilot lamps.

ILØ2--LT Marks the end of a DPU program or that the DPU has started to transfer data to the display register RØ.

ILØ3--LT Marks that one of the rotaries on the front panel has been turned.

ILØ4--LT Is reserved for use by an option.

ILØ5--LT Marks the end of a display cycle.

ILØ6--LT Marks that delta-t information is available on the management unit.

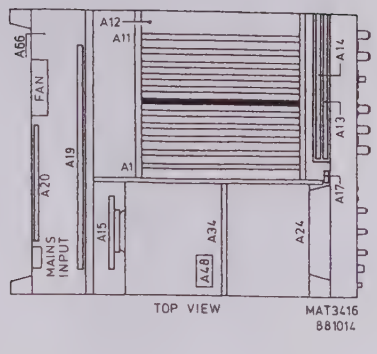
ILØ7--LT Marks that the power goes down.

8.6.2 Memory map

Only a part of the complete address range is used, according to the following memory map which also gives the memory select signals.

Address (Hex)		
ØØØØØØ Ø3FFFF	ROMØ	Unit A6
Ø4ØØØØ Ø7FFFF	ROM1	
Ø8ØØØØ ØBFFFF	Not used	
ØCØØØØ ØFFFFF	uP I/O	
	Not used	Outside unit A6
CØØØØØ CFFFFF	I/O	I/O Select
DØØØØØ D1FFFF	RAMØ	MYSLØ1LT Unit A5
	Not used	
D2ØØØØ D3FFFF	Display RAM	MYSLØ2LT Unit A4 + unit A3
D4ØØØØ D5FFFF	DPU RAM + I/O	MYSLØ3LT Unit A8
D6ØØØØ D7FFFF	OPTION 2	MYSLØ4LT
D8ØØØØ D9FFFF	RAM1	MYSLØ1LT Unit A5
DAØØØØ FFFFFF	Not used	

UNIT A6 - UP UNIT



CONTENTS

8.6.1 General information..... 8.6-1
8.6.2 Memory map..... 8.6-2
8.6.3 Interrupts..... 8.6-3
8.6.4 Circuit description..... 8.6-4
8.6.5 Signal name list..... 8.6-7

8.6.1 General information

This unit mainly consists of a powerfull 68000 microprocessor configuration with EPROM, address decoders, I/O buffers and a clock generator. The microprocessor runs at a clock frequency of 8 MHz.
A bus arbiter has been provided to allow a multiprocessor system, which is used when options are installed in the instrument. The microprocessor has an asynchronous bus structure with a 24 bit address bus and a 16 bit data bus.
Asynchronous means that the microprocessor waits for a "data acknowledge" signal from selected I/O circuitry, before continuing. This enables the microprocessor to handle different access times in I/O circuitry.

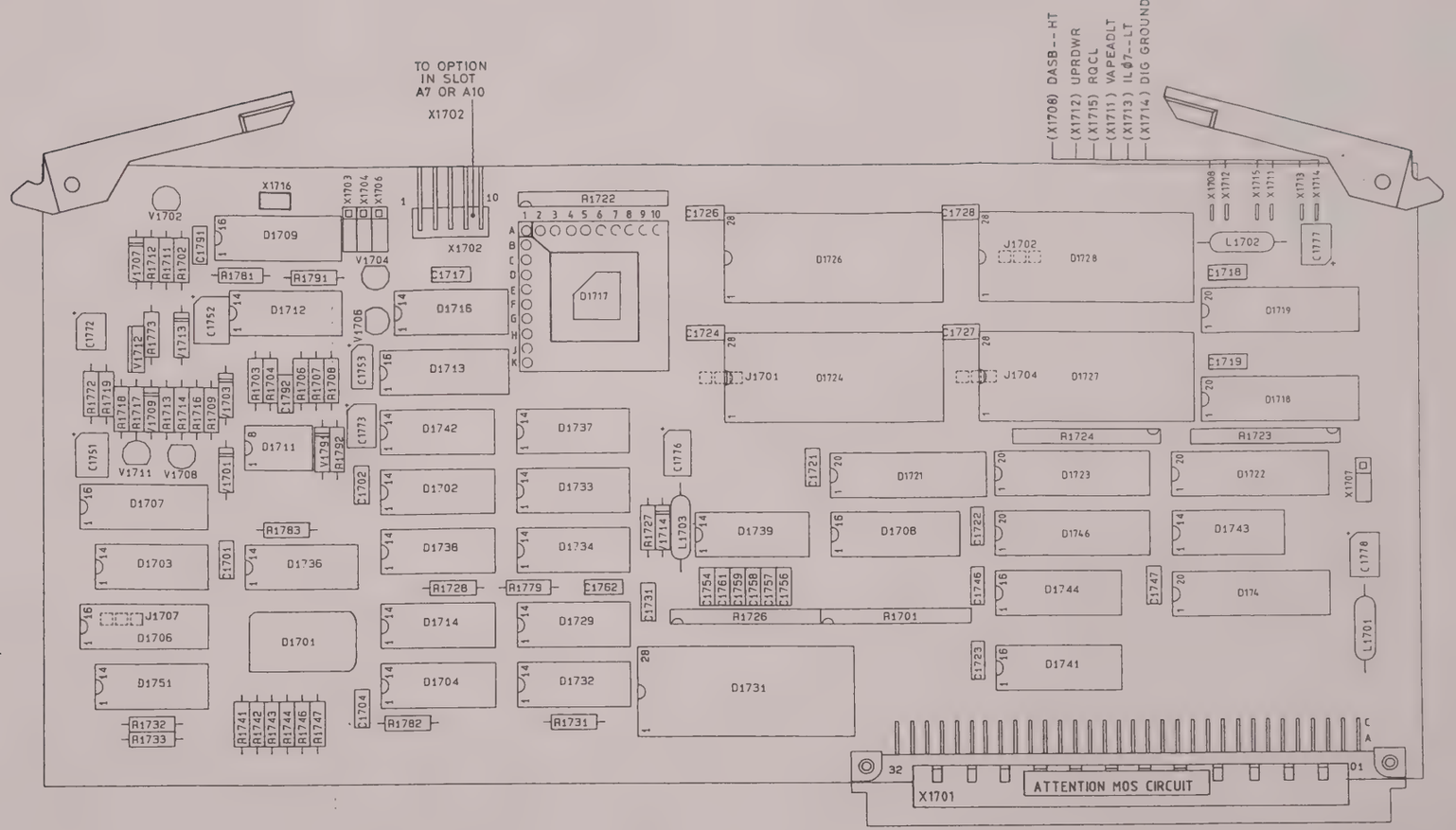


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Figure 8.6.1 Unit A6 - UP UNIT - p.c.b. lay-out.

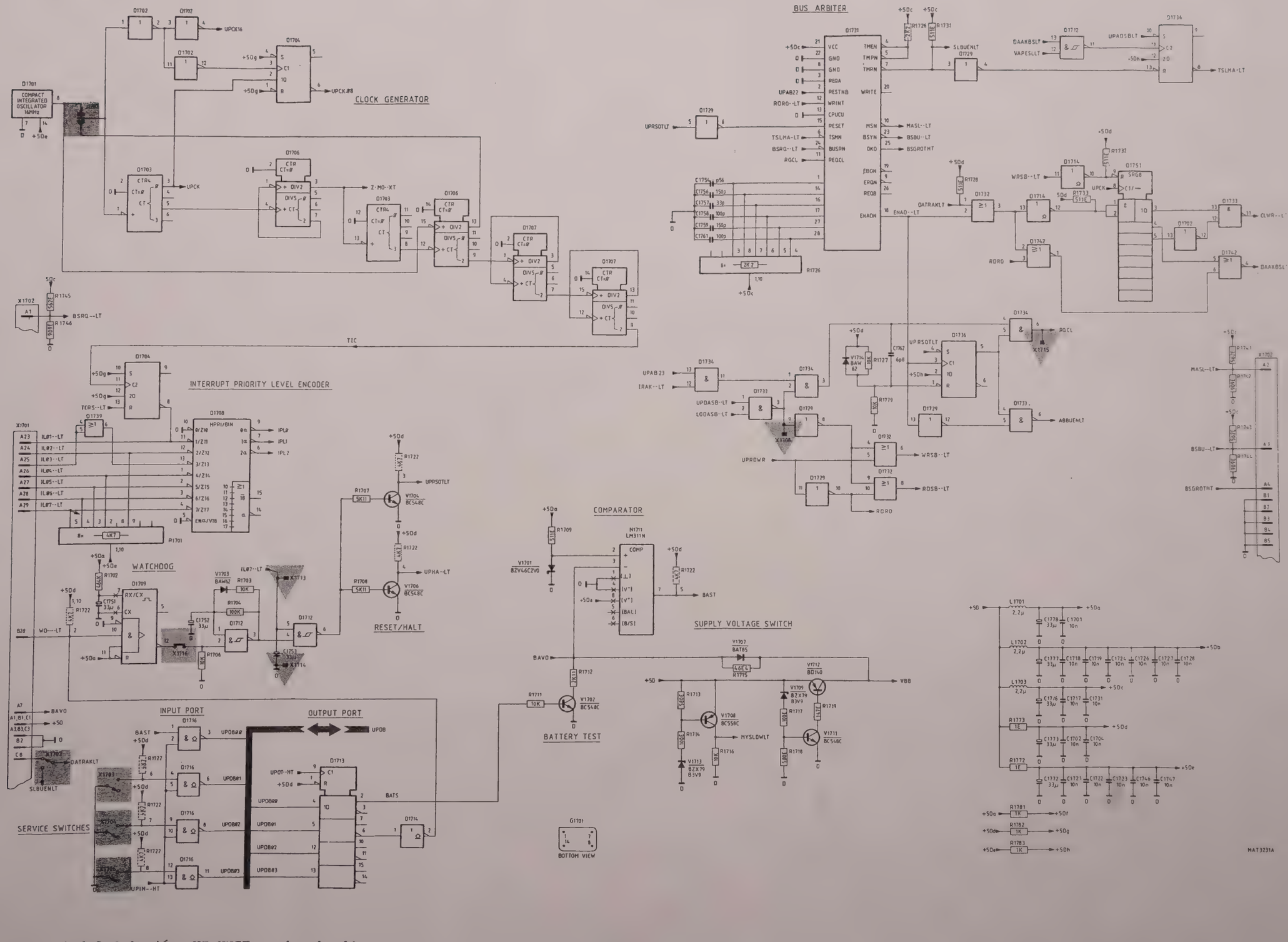


Figure 8.6.2 Unit A6 - UP UNIT - circuit diagram.

REFNR	TYPE	VCC AND GND NUMBERS					
		+5Da	+5Db	+5Dc	+5Dd	+5De	⊥D
D1702	74F04				14		7
D1703	74HCT393	14					7
D1704	74F74				14		7
D1706, D1707	74HCT390	16					8
D1708	74LS148					16	8
D1709	74HCT123	16					8
D1712	74HCT132	14					7
D1713	74HCT175				16		8
D1714	74LS05				14		7
D1716	74HCT03				14		7
D1717	MC68000RC8			D2,E9			D9,E2
D1718, D1719	74LS541		20				10
D1721, D1746, D1747		14				20	10
D1722, D1723	74LS245					20	10
D1724, D1726, D1727 D1728	27010		1, 30, 31, 32				16
D1729	74HCT04				14		7
D1732, D1738	74HCT32				14		7
D1739		14					7
D1733	74HCT00				14		7
D1734	74HCT08				14		7
D1736	74HCT74	14					7
D1737	74HCT10				14		7
D1741	74HCT139					16	8
D1742	74HCT02				14		7
D1743	74HCT30						7
D1744	74HCT138					16	8
D1751	74HCT164			14			7

Figure 8.6.3 Unit A6 - UP UNIT - circuit diagram.

8.8.3 Signal name list

UNIT A8

Signal name	Description	Signal source	Signal destination(s)
ABØ2...12	Address bus Ø2...12	A6+option	-
CDRSMO	P2CCD/RS mode	A8	not used
CHPT	Channel pointer	A5	-
CKAD	Clock address register	A8	A8
CKCL	Clock cycle counter	A8	A8
CKCR	Clock control register	A8	A8
CKDUR1	Clock DPU register I	A8	A12-A9
CKDUR2LT	Clock DPU register II	A8	A12-A9
CKDUR3	Clock DPU register III	A8	A12-A9
CKDUØ8LT	Clock DPU 8 MHz	A8	A8
CKDU16LT	Clock DPU 16 MHz	A8	A8
CKF	Clock flags	A8	A12-A9
CKIR	Clock instruction register	A8	A8
CKOR	Clock offset jump register	A8	A8
CKPL	Clock pipeline register	A8	A8
CLØ...1	Cycle Ø...1	A8	A8
CNCPCN	Count copy address counter	A8	A12-A4
CO	Complement	A8	A12-A9
CSDURM	Chip select DPU ram	A8	A12-A9
CYAA	Carry address adder	A8	A8
CYOT	Carry out	A9	-
DATRAKLT	Data transfer acknowledge	A8+A3+A5+ A6+option	A12-A6, A12-option
DAVA--03	Data valid	A5	-
DBØØ...15	Data bus ØØ...15	A6+option	-
DUABØØ...11	DPU address bus ØØ...11	A8	A12-A9, A12-A4
DUCRØØ...11	DPU control register ØØ...11	A8	A8
DUIRØØ...31	DPU instruction register ØØ...31	A8	A8
EC	End of conversion	A11	-
ENCP	Enable copy	A8	A8
ENCPSA	Enable copy sample	A4	-
ENOFD	Enable overflow detection	A8	A12-A9
ENPRCN	Enable pretrigger counter	A8	A8
FBRY	Feedback ready	A8	A12-A9
ILØ2--LT	Interrupt level Ø2	A8	A12-A6
IRABØØ...1Ø	Instruction register address bus ØØ...1Ø	A8	A8
IS	Initialisation	A8	A8
LDPRCNLT	Load pretrigger counter	A8	A8
LEDP	Latch enable display	A8	A12-A4
MMPT	Min/max pointer	A5	-
MYSLØ3LT	Memory select Ø3	A6	-

The ADDRESS GENERATOR generates addresses for the pretrigger ram, the average ram and the flag ram on the DPU.
It consists of the following parts:

- buffer
- offset jump register
- address register
- adder
- pretrigger counter
- multiplexer
- trigger address comparator

The BUFFER is a 12 bit buffer (D1421 + D1422), which latches data from the microprocessor. It is clocked by SLOT4.
When OTDIPR is low the data are put on the DPU address bus (DUABØØ...11).DUABØØ is also led to the status multiplexer.

The OFFSET JUMP REGISTER (D1436, D1419 + D1437) consists of two parts. If OTENDT is low, D1436 and D1437 latch DUCRØØ...11, which is the offset jump. D1436 and D1437 are clocked by CKOR, which is derived from bit 14 of the program word. The output signals are applied to the adder.
If OTENDT is high DBØ8...DB15, which represent delta-t information is latched by D1419 on SLOT2. D1437 is reset.
The output signals of D1419 and D1437 are applied to the adder.
Due to the inverter D1406 either the outputs of D1436 or D1419 are enabled.

The ADDRESS REGISTER (D1443 + D1444) is a 12 bit latch, which latches data from the DPU address bus. It is clocked by CKAD. It can be reset by RSAD--LT.

The ADDER is a 12 bit adder, which adds data from the offset jump register and the address register. The carry signal (CYAA) is led to the status multiplexer.

The PRETRIGGER COUNTER (D1453, D1454 + D1456) is a 12 bit presetable up/down counter.
The preset value is loaded from the DPU address bus by LDPRCNLT. The counter value is applied to the pretrigger address bus (PRABØØ...11). When all counter bits are "1" TCPRCN is generated by D1404. It is led to the status multiplexer.
In the direct mode and the roll mode the counter is used as a pretrigger counter. In the other modes it is used for various functions.

The MULTIPLEXER (D1449, D1451 and D1452) selects data from the adder or from the pretrigger counter. The data are applied to the DPU address bus.
When SLPRAB is low, the data from the adder are selected, otherwise data from the pretrigger is selected.
Because OTDIPR and OTDIMX are in antiphase (D1406 pin 3 and 4) either the buffer or the multiplexer writes data to the DPU address bus.

The TRIGGER ADDRESS COMPARATOR is fitted on unit A4. Therefore it is described in chapter 8.4.

The START/STOP LOGIC mainly consists of FPLS D1452 (Field Programmable Logic Sequencer). It generates a number of control signals depending on the status of its input signals.
Three outputs and the output of the status multiplexer are latched by IC D1458. The four outputs determine via the address multiplexer the four most significant address bits of the next instruction. If output pin 16 or pin 17 of D1457 goes low ILØ2—LT is generated via D1404. The microprocessor reads then via D1423 the status of both outputs. The going low of pin 16 marks that the DPU has started to fill display register RØ with samples (ROLL mode and DIRECT mode). The going low of pin 17 marks that the DPU has finished its program.

The STATUS MULTIPLEXER consists of two 1 of 8 multiplexers (D1402 and D1403), which form together a 1 of 16 multiplexer.
The status signal that is selected is determined by the SLSSØØ...Ø3 signals from the pipeline register b.

The ADDRESS MULTIPLEXER (D1409, D1411 and D1412) is a 12 bit multiplexer of which 11 bits are used.
When a DPU program is executed SLAB is low. NXABØØ...NXØ6 and four output signals of D1458 are selected. The address of the next word in the control memory is determined by the 7 less significant bits of the current word and the signals SS1, IS, CLØ and CL1.
When a DPU program is loaded in the control memory by the microprocessor, SLAB is high. The address where the word is loaded is determined by the address selected by the microprocessor.

The CONTROL MEMORY is a 2048 x 32 ram. It is built with four 2048 x 8 ram´s (D1426...1429). SLOTØ is the write signal for the lower 16 bits of a word, SLOT1 is the write signal for the higher 16 bits of a word.
When a DPU program is executed both are high, which results in the read status of the ram. The data on the DUIR bus are determined by the address on the IRAB.

The buffer is a 32 bit buffer (D1413, D1414, D1416 and D1417) between the microprocessor data bus and the DUIR bus. It seperates data on both buses when a DPU program is executed.
When a DPU program is loaded, data from the microprocessor are transferred to the control memory by the SLOTØ and SLOT1 signals, which also control the control memory.

The PIPELINE register is a 32 bit register (D1431...1434), which holds the current instruction, while the next instruction is fetched from the control memory. It is clocked by CKPL, which is generated by the start/stop logic.
At the outputs of the register the definition of the program word can be recognized.

The INSTRUCTION REGISTER (D1441 + D1442) is a 12 bit latch, that latches 12 signals for the DPU. It is clocked by CKIR, which is derived from bit 12 of the program word via D1459.

The CONTROL REGISTER (D1438 + D1439) is a 12 bit latch, that latches 12 signals, which are mainly used on this unit. It is clocked by CKCR, which is derived from bit 13 of the program word.

bits ØØ...Ø6	are the 7 less significant bits of the address of the next instruction
bit Ø7	marks the end of a program
bits Ø8...11	selects statusbit in case of a conditional jump
bit 12	if set bits 16...27 are data for the instruction register
bit 13	if set bits 16...27 are data for the control register
bit 14	if set bits 16...27 are data for the offset jump register
bit 15	if set it generates the signal CSDURM for the DPU
bits 16...27	data for the instruction register or control register or offset jump register, depending on the status of bits 12...14
bits 28...31	if set they generate respectively the signals CKDUR1, CKDUR2LT, CKDUR3 and RDDURM for the DPU.

The control memory may contain one or more programs with a maximum length of 128 words (7 address bits).
The program which is selected depends on the 4 most significant address lines (bits Ø8...11).
The DPU CONTROL consists of the following parts:

- address decoder
- mode register
- start/stop logic
- status multiplexer
- address multiplexer
- control memory
- buffer
- pipeline register
- instruction register
- control register
- address generator

The ADDRESS DECODER, which mainly consists of IC D1401, decodes some address lines from the microprocessor to the select signals SLOTØ...6. Because the logic on this unit is fast enough, the DATRAKLT signal can go low immediately when MYSLØ3LT goes low.
IC D1424 generates a clock signal for the mode register when SLOT2 goes low and the SLAB signal when UPSL goes high.
Furtheron this part contains some buffers for clock signals.

The MODE REGISTER (D1418) is an 8 bit latch that latches data from the microprocessor for the control of the start/stop logic.

Other functions are:

- Roll mode:	roll effect
	digital Min / Max
- Direct mode:	pretrigger
	digital Min / Max
- P^2CCD mode:	digital leakage correction
	linear interpolation
	delta-calculation in maximum resolution mode
- Random sampling mode:	digital leakage correction
	delta-t calculations
- All modes:	flag handling (e.g. overflow)
	averaging

Digital leakage correction is explained in chapter 8.33.3.3.
Digital Min / Max is explained in chapter 8.33.3.5.

To perform these functions there are lines to the Acquisition Control Logic on unit A5, the ADC on unit A11 and the Display Memory + Control on units A3 and A4.
The Data Processor gets its programs for the various modes from the microprocessor.
When a program is finished or other DPU actions have to be reported, an interrupt to the microprocessor (ILØ2--LT) is generated.
A part of the DPU CONTROL is fitted on unit A4. This trigger address comparator (TACM) is marked with a dashed square in figure 8.8.1.
Normally it is rather difficult to check the proper operation of the Data Processor. Therefore it is recommended to use the "DPU test", which is in the diagnostic software (see chapter 11).

8.8.2 Circuit description

The DPU (unit A9) performs the calculations on the sample data. To be able to do this, it receives a number of control signals and addresses from the DPU CONTROL.
These are derived from program words that are stored in the control memory.
The format of these 32 bit program words is defined as follows:

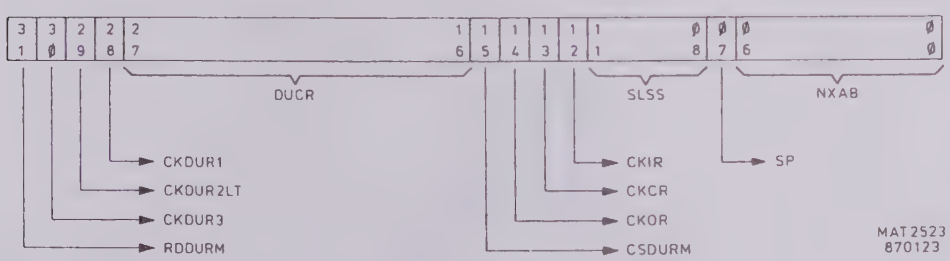
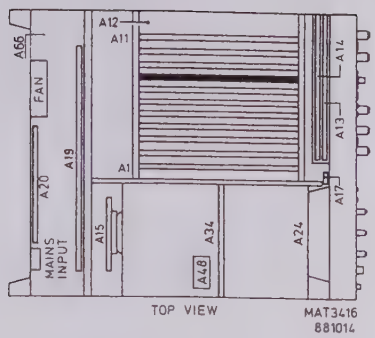


Figure 8.8.2 Program word format.

UNIT A8 - DPU CONTROL UNIT



CONTENTS

8.8.1 General information..... 8.8-1
8.8.2 Circuit description..... 8.8-2
8.8.3 Signal name list..... 8.8-6

8.8.1 General information

The DPU control forms together with the DPU (Data Processing Unit) a fast Data Processor with an instruction cycle time of 125 ns.
The main function of the Data Processor is to accept sample data from the ADC, to perform calculations on it and to load the data in register RØ of the Display unit (see figure 8.8.1).

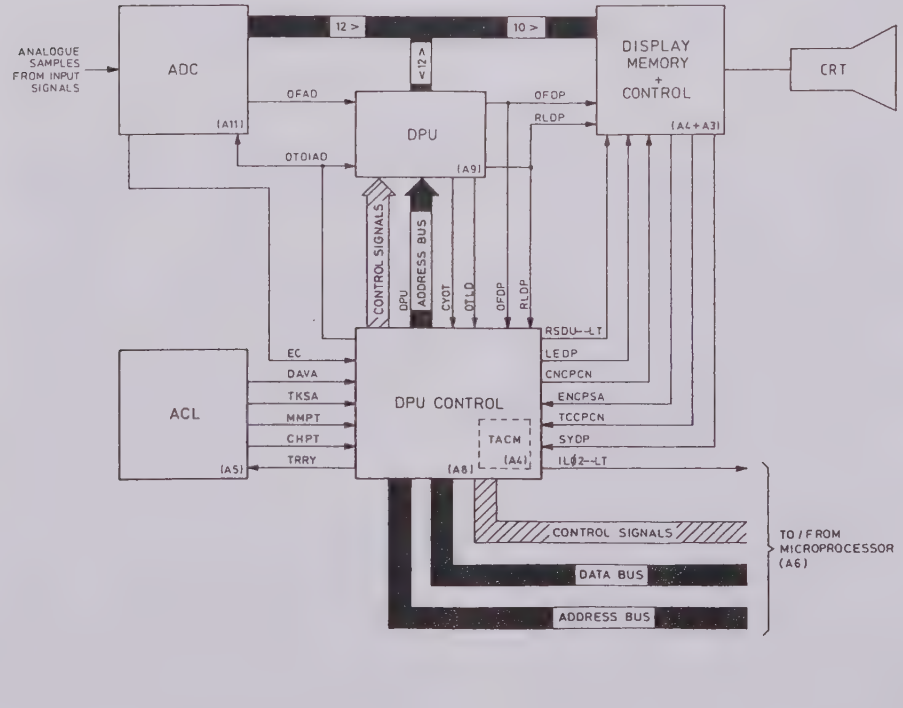
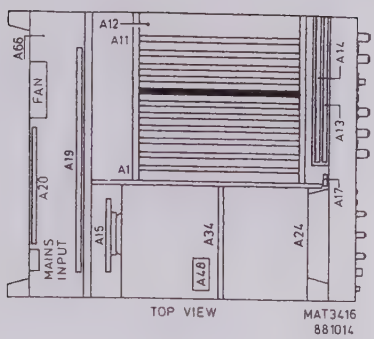


Figure 8.8.1 Data Processor.

UNIT A7 - OPTION 1



CONTENTS

8.7.1 General information..... 8.7-1

8.7.1 General information

This OPTION 1 slot is reserved for an optional printed circuit board.

An optional printed circuit board in this slot is not available in standard instruments.

A second slot (OPTION 2) is also available in this instrument (see section 8.10.1).

NOTE: The first option to be installed in this instrument must always be placed in the OPTION 1 slot. The OPTION 2 slot may only be used if an option is installed already in the OPTION 1 slot.

Signal name	Description	Signal source	Signal destination(s)
NXABØØ...Ø6	Next address bus ØØ...Ø6	A8	A8
OEDUØØ	Output enable DPU ØØ	A8	A12-A9
OEDUØ1	Output enable DPU Ø1	A8	A12-A9
OFDP	Overflow display	A9	-
OTCM	Output comparator	A4	-
OTDIAD	Output disable ADC	A8	A12-A9, A12-A11
OTDIMX	Output disable multiplexer	A8	A8
OTDIPR	Output disable pretrigger	A8	A8
OTENDT	Output enable delta-t	A8	A8
OTLD	Output limit detection	A9	-
PRABØØ...11	Pre-trigger address bus ØØ...11	A8	A8
RDDURM	Read DPU ram	A8	A12-A9
RLDP	Read sample display	A9	-
RSAD--LT	Reset address register	A8	A8
RSDU--LT	Reset DPU	A8	A12-A4
RSDUR--LT	Reset DPU registers	A8	A12-A9, A12-A4
SFSRØØ	Select function shift register ØØ	A8	A12-A9
SFSRØ1	Select function shift register Ø1	A8	A12-A9
SLAB	Select microprocessor address bus	A8	A8
SLAM	Select average memory	A8	A12-A9
SLOFAD	Select overflow ADC	A8	A12-A9
SLOTØ...6	Select output Ø...6	A8	A8
SLPRAB	Select pretrigger address bus	A8	A8
SLSSØ...6	Select status Ø...6	A8	A8
SP	Stop	A8	A8
SS	Status	A8	A8
SS1	Status 1	A8	A8
STRLF	Set real sample flag	A8	A12-A9
SYDP	Synchronize display	A3	-
TCCPCN	Terminal count copy address counter	A4	-
TCPRCN	Terminal count pre-trigger counter	A8	A8
TKSA	Take sample	A5	-
TRRY	Transfer ready	A8	A12-A5
UPCKØ8	Microprocessor clock 8 MHz	A6	-
UPCK16	Microprocessor clock 16 MHz	A6	-
UPDO	Up/Down	A8	A8
UPRD--LT	Microprocessor read	A6	-
UPWR--LT	Microprocessor write	A6	-
UPSL	Microprocessor select	A8	A8

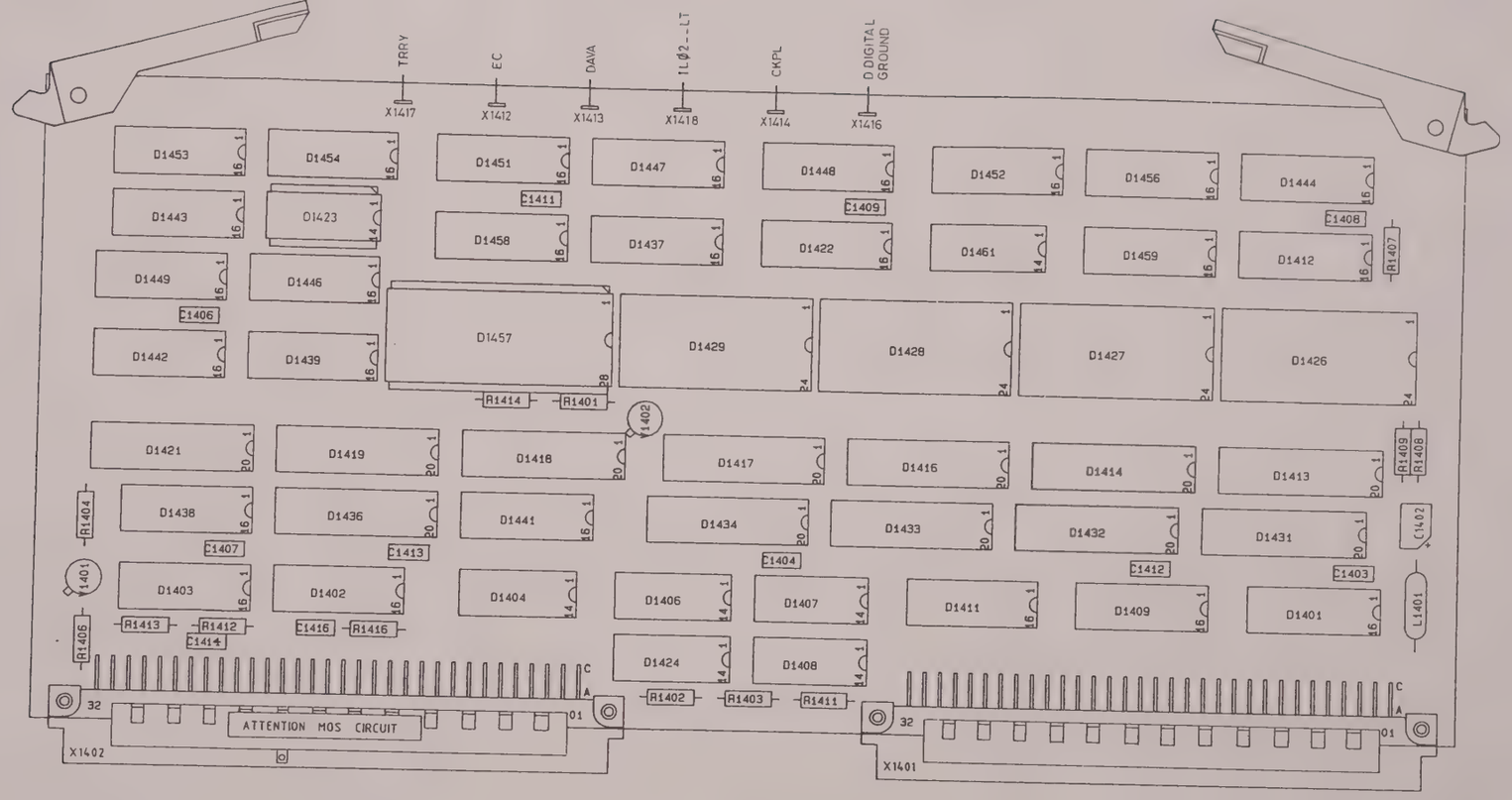


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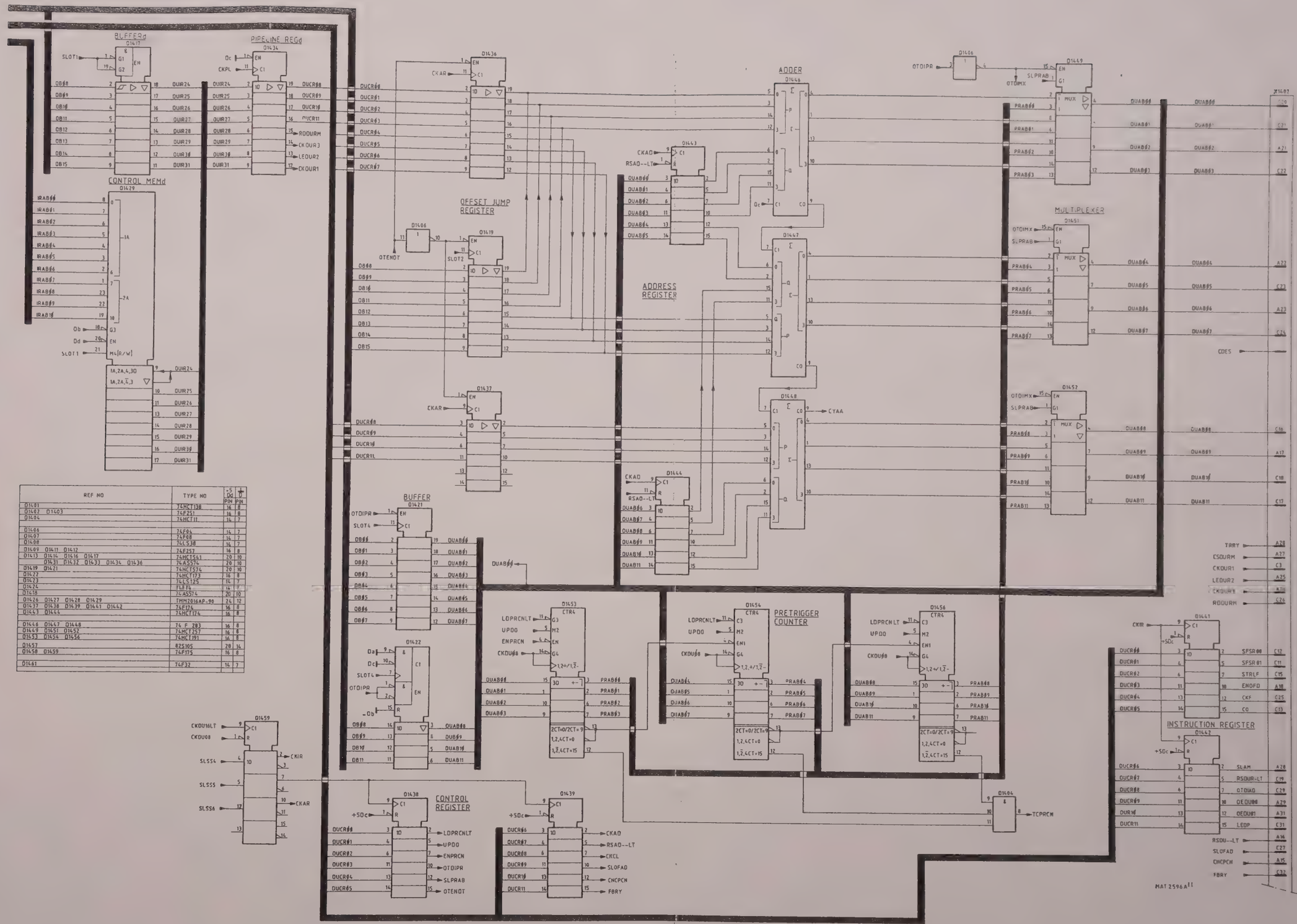
Figure 8.8.3 Unit A8 - DPU CONTROL UNIT - p.c.b. lay-out.

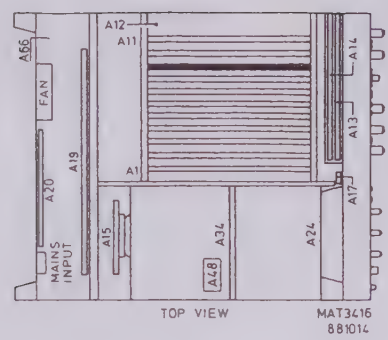
Figure 8.8.4 Unit A8 - DPU CONTROL UNIT - circuit diagram.



REF NO	TYPE NO	-5 Dd PIN	+5 D PIN
D1401	74HCT138	16	8
D1402 D1403	74F251	16	8
D1404	74HCT11	14	7
D1406	74F04	14	7
D1407	74F08	14	7
D1408	74LS38	14	7
D1409 D1411 D1412	74F257	16	8
D1413 D1414 D1416 D1417	74HCT541	20	10
D1431 D1432 D1433 D1434 D1436	74AS574	20	10
D1419 D1421	74HCT574	20	10
D1422	74HCT173	16	8
D1423	74LS125	14	7
D1424	74F74	14	7
D1418	74AS574	20	10
D1426 D1427 D1428 D1429	TMM2016AP-90	24	12
D1437 D1438 D1439 D1441 D1442	74F174	16	8
D1443 D1444	74HCT174	16	8
D1446 D1447 D1448	74 F 283	16	8
D1449 D1451 D1452	74HCT257	16	8
D1453 D1454 D1456	74HCT191	16	8
D1457	82S105	28	14
D1458 D1459	74F175	16	8
D1461	74F32	14	7

Figure 8.8.5 Unit A8 - DPU CONTROL UNIT - circuit diagram.

UNIT A9 - DPU UNIT



CONTENTS

8.9.1 General information..... 8.9-1
8.9.2 Circuit description..... 8.9-1
8.9.3 Example of DPU operation..... 8.9-4
8.9.4 Signal name list..... 8.9-5

8.9.1 General information

The DPU (Data Processing Unit) forms together with the DPU control (unit A8) a fast Data Processor. It is recommended to read first chapter 8.8.1 and 8.8.2 before reading chapter 8.9.2.

8.9.2 Circuit description

The DPU consists of the following parts:

- buffer
- register I
- complementer
- adder
- register III
- overflow detection
- reflection suppression
- shift register
- limit detection
- register II
- pretrigger ram
- average ram
- flag ram
- flag handler

All these parts, excepted the adder and the overflow detection, are interconnected via the 16 bits wide DPU data bus (DUDBØØ...15).

The BUFFER is a bidirectional data buffer (D1203, D1204 and D1206). To convert the 12 sample data bits to 16 DPU data bits SADB11 is applied to DUDB11...15.
Ten processed sample data bits (SADBØØ...Ø9) are applied to the display memory (unit A4).
When OTDIAD is low, data are transferred from the ADC (unit A11) to the DPU. When OTDIAD is high and FBRY or LEDP are high, data is transferred from the DPU to the display memory.

REGISTER I (D1216 + D1217) is a resettable latch, which is clocked by CKDUR1. It is used for various latching functions.

The COMPLEMENTER (+/-) complements data (D1211...D1214). It is used for substractions with the adder.
Because the DPU calculates in two's complement notation, after complemention 1 should be added to get the correct negative number. This is done by the CO signal on the carry input of the adder (D1218 pin 7).

The ADDER (D1218, D1219, D1221, D1222) adds the data from the complementer and register I.
The carry signal at pin 9 of D1222 can generate the CYOT signal via some logic (D1223).

REGISTER III (D1224 + D1226) is a latch, that latches the output result of the adder. It is clocked by CKDUR3.

The OVERFLOW DETECTION (D1231 and associated components) latches on CKDUR3 an overflow bit from D1228 pin 3 and a sign bit from D1222 pin 10 in D1231. So the two bits belong to the data that is clocked in register III. The table below shows which overflow is selected:

SLOFAD	ENOFD	Overflow from
X	0	always "1"
0	1	ADDER
1	1	ADC

Via the logic in D1227 the OTDI3 signal enables wether register 3 by OTEN3-LT or the reflection suppression by OTENRSLT, depending on the presence of overflow.

D1254 decodes the OEDUØØ and OEDUØ1 signals to register control signals, which are active when RDDURM is low.

The REFLECTION SUPPRESSION (D1236...D1239) puts data on the DPU data bus when an overflow occurs, instead of Register III. It consists of a multiplexer, that selects 0000 0000 0011 1111 or 1111 1111 1100 0000, depending on the sign bit from D1231 pin 8.
This circuit prevents the arise of reflection of the input signal in the bottom of the display when high input voltages cause overflow in the display amplitude.
The same is valid in the top of the display with high negative input voltages.

The SHIFT REGISTER (D1242 + D1243) reads data from the DPU data bus, shifts them (left or right) and writes them back to the DPU data bus. This is used for multiplication or division by factors which are a multiple of 2.
The contents of the shift register can be cleared by RSSR--LT, which is used to write zeroes to the DPU data bus.
The signals SFSRØØ and SFSRØ1 determine the function of the register (shift left or right, load or hold) on the clock signal CKSR.

The LIMIT DETECTION detects wether DUDBØ4...11 are all zero or one. This means that the data on the data bus represents a number that is between -16 and +16. This is used for some calculations.

REGISTER II (D1207 + D1208) is a latch, which is used for the intermediate storage of calculation results. It is clocked by CKDUR2LT. When OTDI2 is low, the register writes it's data to the DPU data bus.

The PRETRIGGER + AVERAGE RAM consists of two 8Kx8 rams (D1249 + D1251), forming together an 8Kx16 ram. The lower address range is used as a 4Kx16 pretrigger ram. The higher address range is used as a 4Kx16 average ram.
The addresses for the ram are generated by the address generator on the DPU control (unit A8).
The highest address bit of the ram (pin 2) determines wether the pretrigger or the average ram is selected.
In the pretrigger ram a data word consists of 14 data bits, a real sample flag bit and an overflow flag bit.
In the average ram a data word consists of 16 data bits.

The FLAG RAM consists of a REAL SAMPLE FLAG RAM and an OVERFLOW FLAG RAM. Each consists of a 4Kx1 ram (D1252 and D152), which contain the flags for the data in the average ram.
A real sample flag indicates wether a sample is a real taken sample or a sample that is obtained by means of interpolation between two real samples.
An overflow flag indicates an overflow of a sample. If one or both of two real samples behind each other have an overflow flag, all interpolated samples between them have an overflow flag.

The main functions of the FLAG HANDLER (D1241 and D1232...D1234) are given in the table below.

RDDURM	SLAM	Function of flag handler
0	0	Write flags (STRFL and STOFF) in pretrigger ram.
1	0	Read flags from pretrigger ram and write flags to D1233 and/or to display memory (unit A4) via D1232.
0	1	Write flags in flag ram (D1252 and D1253). Connect DUDB14 and DUDB15 to two MSB's of average ram (D1251 pin 18 + 19)
1	1	Read flags from flag rams to D1233 and to display. Connect two MSB's of average ram to DUDB14 and DUDB15.

The circuit consisting of D1233 and the gates behind, generates an overflow flag for interpolated samples if one of the real samples has an overflow flag.

Note: the overflow flags are not used in this instrument, but they can be read by an option.

8.9.3 Example of DPU operation

The following example describes in a simplified way the calculation of 7 interpolated samples between 2 real samples.

It is supposed that:

- a sweep of real samples is placed in the pretrigger ram.
- the distance between 2 real samples is 8 address locations.
- the intermediate locations have to be filled with interpolated samples.
- none of the real samples has an overflow flag.

The next actions are taken by DPU:

1: copy a real sample from the pretrigger ram to register II and to the shift register.

2: copy the next real sample to register I.

3: enable the register II outputs and activate CO (complement); the inverted first sample is applied to the adder.

4: now the adder subtracts the first sample from the second sample.

5: clock the sample difference in register III.

6: copy the sample difference to register I.

7: in the meanwhile the shift register has shifted left three times, which means that the sample value is multiplied by 8.

8: add the shift register contents and the sample difference.

9: clock the result (interpolated sample x8) in register III.

10: copy the contents of register III in the shift register.

11: by the enabled register III the next interpolated sample x8 is offered to the inputs of this register via the adder and the sample difference in register I.

12: clock this next interpolated sample in register III.

13: the shift register shifts right three times; the result is an interpolated sample.

14: copy the result to the pretrigger ram.

15: repeat steps 10 to 14 another six times for the remaining calculations of interpolated samples.

NOTES: - For obtaining maximum accuracy, the sample difference is not divided by 8, but the sample values are multiplied by 8.
- The complex address generation for the pretrigger ram is done by the address generator on the DPU control.

8.9.4 Signal name list

UNIT A9

Signal name	Description	Signal source	Signal destination(s)
CKDUR1	Clock DPU register I	A8	-
CKDUR2LT	Clock DPU register II	A8	-
CKDUR3	Clock DPU register III	A8	-
CKF	Clock flags	A8	-
CKSR	Clock shift register	A9	A9
CO	Complement	A8	-
CSDURM	Chip select DPU ram	A8	-
CSF	Chip select flags	A9	A9
CYOT	Carry out	A9	A12-A8
DUABØØ...11	DPU address bus ØØ...11	A9	-
DUDBØØ...15	DPU databus ØØ...15	A9	A9
ENOFD	Enable overflow detection	A8	-
ENPM--LT	Enable pretrigger memory	A9	A9
FBRY	Feedback ready	A8	-
LEDP	Latch enable display	A8	-
OFAD	Overflow ADC	A11	-
OFDP	Overflow display	A9	A12-A4, A12-A8
OTDI2	Output disable DPU register II	A9	A9
OTDI3	Output disable DPU register III	A9	A9
OTDIAD	Output disable ADC	A8	-
OTDISR	Output disable shift register	A9	A9
OEDUØØ	Output enable DPU ØØ	A8	-
OEDUØ1	Output enable DPU Ø1	A8	-
OTENRSLT	Output enable reflection suppression	A9	A9
OTEN3-LT	Output enable DPU register III	A9	A9
OTLD	Output limit detection	A9	A12-A8
RDDURM	Read DPU ram	A8	-
RLDP	Real sample display	A9	A12-A4, A12-A8
RSDUR-LT	Reset DPU registers	A8	-
RSSR--LT	Reset shift register	A9	A9
SADBØØ...11	Sample data bus ØØ...11	A9+A11	A12-A4
SFSRØØ	Select function shift register ØØ	A8	-
SFSRØ1	Select function shift register Ø1	A8	-
SLAM	Select average memory	A8	-
SLOFAD	Select overflow ADC	A8	-
STOFF	Set overflow flag	A9	A9
STRLF	Set real sample flag	A8	-
UPCKØ8	Microprocessor clock 8 MHz	A6	-

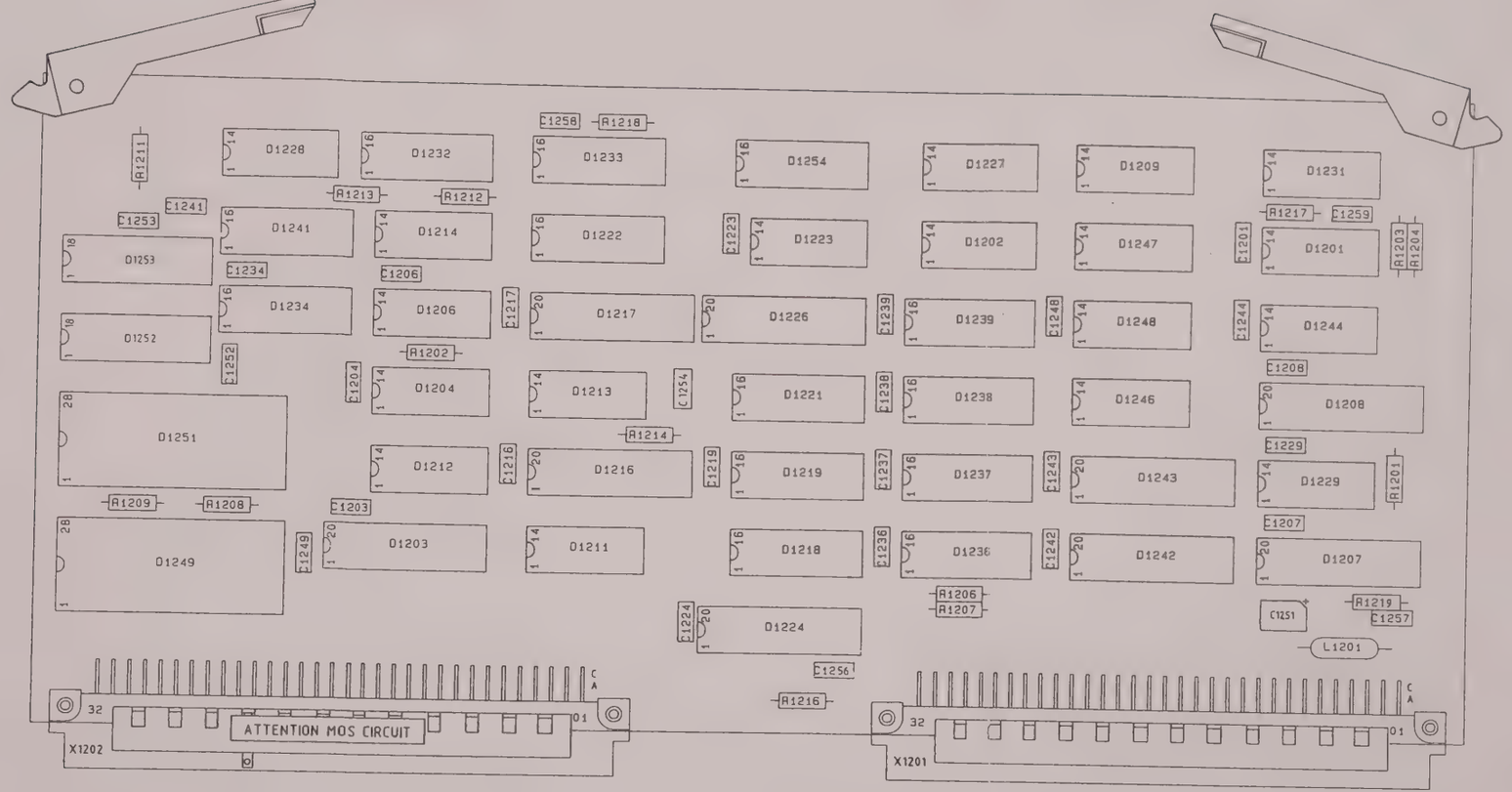


Figure 8.9.1 Unit A9 - DPU UNIT - p.c.b. lay-out.

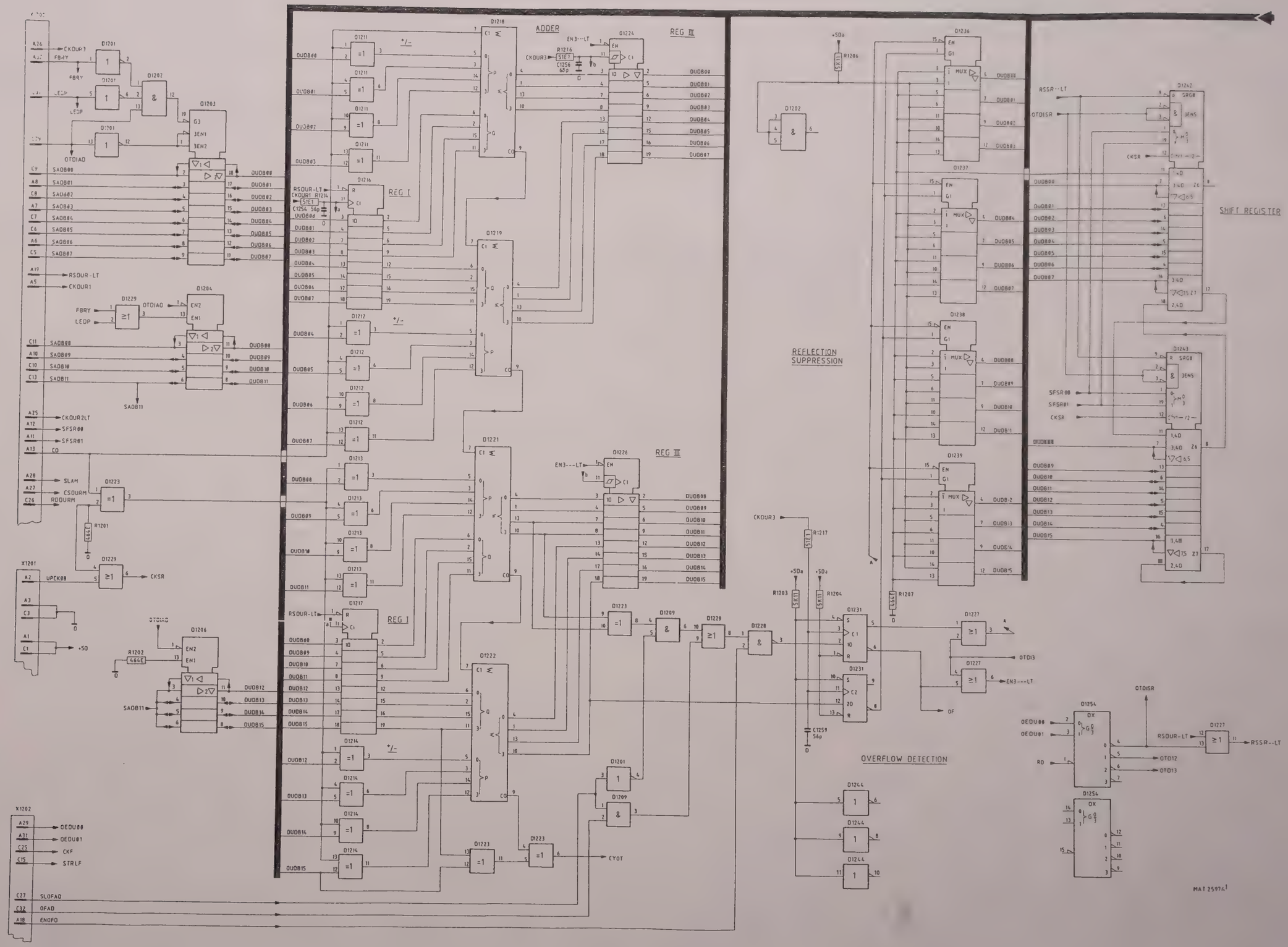


Figure 8.9.2 Unit A9 - DPU UNIT - circuit diagram.

OUTPUT LIMIT DETECTION

PRETRIGGER AVERAGE RAM

REAL SAMPLE FLAG RAM

OVERFLOW FLAG RAM

REG II

FLAG HANDLER

REF.NR.	TYPE	PIN NUMBERS FOR Vcc AND GND -5Vd				⊥ 0
D1201,1244	74HCT04	14				7
D1246	74HCT04	14				7
D1202	74HCT11	14				7
D1203	74HCT245	20				10
D1204,1206	74HCT243	14				7
D1207,1208	74HCT373	20				10
D1209	74F08	14				7
D1211,1213	74HCT86	14				7
D1212,1214	74HCT84	14				7
D1216,1217	74HCT273	20				10
D1218,1219,1221	74F283	16				8
D1222	74F283	16				8
D1223	74F86	14				7
D1224,1226	74HCT374	20				10
D1227	74F32	14				7
D1228	74F00	14				7
D1229	74F32	14				7
D1231	74F24	14				7
D1232	74HCT157	16				8
D1233	74F125	16				8
D1234	74F257	16				8
D1236,1237,1238,1239	74HCT257	16				8
D1242,1243	74HCT299	20				10
D1247,1248	74HCT367	14				7
D1249,1251	BM62644P	28				14
D1252,1253	D314TH	18				9
D1254	74F139	16				8
D1241	74HCT257	16				8

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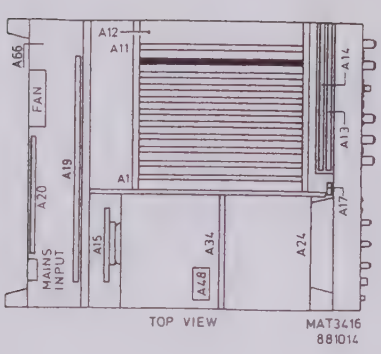
Figure 8.9.3 Unit A9 - DPU UNIT - circuit diagram.

UNIT A10 - OPTION 2



CONTENTS

8.10.1 General information..... 8.10-1

8.10.1 General information

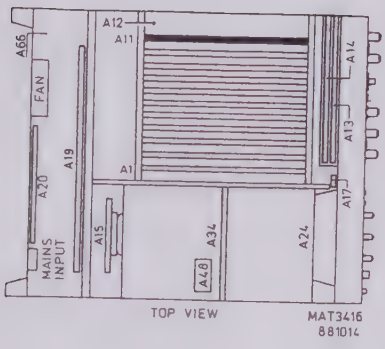
This OPTION 2 slot is reserved for an optional printed circuit board.

An optional printed circuit board in this slot is not available in standard instruments.

A second slot (OPTION 1) is also available in this instrument (see section 8.7.1).

NOTE: The first option to be installed in this instrument must always be placed in the OPTION 1 slot. The OPTION 2 slot may only be used if an option is installed already in the OPTION 1 slot.

UNIT A11 - ADC + T&H UNIT



CONTENTS

8.11.1 General information..... 8.11-1
8.11.2 Circuit description..... 8.11-2
8.11.3 Signal name list 8.11-3

8.11.1 General information

The ADC and T&H unit accepts the samples from one or both input channels from the P^2CCD unit and converts these samples into 12 bits binary codes, which are routed to the DPU (unit A9) for further digital processing.

8.11.2 Circuit description

The samples come from the P^2CCD unit (THINAN) every 2,5 microsecond. They are applied to the CORRECTION CIRCUIT. This circuit compensates some non-linearity of the P^2CCD´s.
IC D616 is a multiplier, whose multiply factor is influenced by the setting of the LINEARITY potentiometer R721, through which correct compensation can be achieved. At the output signals at pin 15 and pin 16 an adjustable offset voltage is added by the circuit around stabiliser N607. The offset can be adjusted with the potentiometer R705.
The signal at pin 15 is applied to a T&H gate (D613 and associated components) via R707.

This T&H tracks the input signal continuously until the signal STCV-1 goes high. Now the output of D613 (pin 12) is held at the momentary value of the input signal.
Its output voltage goes via a buffer amplifier (V607, V608 and V609) to another buffer amplifier; N601 and associated components.
From this buffer amplifier the signal (THOTAN) goes to the ADC.
This buffer amplifier gives a feedback in the track mode (N601 pin 10) to the T&H gate. It is also a separation between the ADC and the T&H gate.

The signal THOTAN is applied to the ADC.
The ADC starts the conversion on the STAD--HT signal from the ADC logic. During this conversion the T&H gate is in the hold mode, to give the ADC a stable input signal.

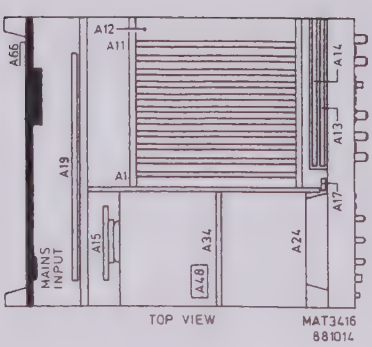
The ADC output lines ADOT00...ADOT10 are led to the overflow detection circuit and to the sample data latch.
Line ADOT11 is buffered by D607. The three buffered lines ADOT11-1...ADOT11-3 are led to the overflow detection and the code converter.

The overflow detection detects whether all 11 ADC output signals are "0" (sample voltage too negative) or "1" (sample voltage too positive). The outputs (wired or) generate via D609 (pin 12 and 9) the OFAD signal to the DPU (unit A9) to indicate that an overflow occured uring the conversion.

The code converter inverts ADOT11-3 (MSB) to convert the ADC output from straight binary code to two´s complement code.
This two´s complement code is latched by the sample data latch and afterwards applied to the DPU by the OTDIAD signal from the DPU.

The ADC logic generates the control signals from the UPCK16 signal. Figure 8.11.1 shows the timing diagram.

UNIT A66 - ASSY FRAME REAR



CONTENTS

8.66.1 Description..... 8.66-1
8.66.2 Signal name list..... 8.66-1

8.66.1 Description

The assy frame rear module consists of a rear plate on which the following parts are mounted:

- power 2 unit (A20)
- mains entrance with fuseholder and fuse
- mains switch
- fan
- battery pack
- several input/output connectors

The circuit diagram can be found in the drawings of the power 1 unit (A19) and the power 2 unit (A20). It needs no further explanation.

WARNING: To avoid any electrical shock, it is strongly recommended to read section 10.1 first.

The rear plate is connected to the chassis of the oscilloscope with an earth cable. For security this cable should never be removed when the rear plate is taken away from the chassis.

ADJUSTING PROCEDURE

ADJUSTING PROCEDURE

CONTENTS

9.0 Adjusting procedure..... 9-1
9.1 General information..... 9-1
9.2 Recommended test and calibration equipment..... 9-1
9.3 Adjusting procedure..... 9-2

Before any adjustment, the instrument must attain ...
operating temperature.

- Warming-up time under average conditions is 30 minutes.
- Where possible, the instrument performance should be checked before any adjustment is made.
- All limits and tolerances given in this section are calibration guides, and should not be interpreted as instrument specifications unless they are also published in chapter 3.
- Tolerances given are for the instrument under test and do not include test equipment error.
- The most accurate display adjustments are made with a stable, well-focussed low intensity display.
- All controls which are mentioned without item numbers are located on the outside of the instrument.

WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts, and also accessible terminals may be live. The instrument shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair during which the instrument will be opened. If afterwards any adjustment, maintenance or repair of the opened instrument under voltage is inevitable, it shall be carried out only by a qualified person who is aware of the hazard involved. Bear in mind that capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.

9.2. RECOMMENDED TEST AND CALIBRATION EQUIPMENT

A complete list of all material necessary for both this adjusting procedure and the performance check is given in chapter 13.1 in this manual.

... are given in figure 9.8
... adjustment step the itemnumber of the
... element (e.g. R4607) and the unit where it is located
(e.g. A20) are given.

NOTE: Use always an isolated adjustment tool.

9.3.2 Power supply adjustments

- Connect a digital voltmeter between the measuring points X4609 and X4611 on unit A20.
- Check for a d.c. voltage of 10 V (+ or - 0,1V). If necessary readjust R4607 on unit A20.
- Connect a digital voltmeter between the measuring points X2517/X2518 on unit A25.
- Check for a d.c. voltage of 5 V (+ or - 100 mV). If necessary readjust R462 on unit A25.

9.3.3 Adjustments in the C.R.T.-section

NOTE: In case that your instrument is completely misadjusted or after exchange of unit A1 it is recommended to turn R2658, R2659, R2678 and R2682 on unit A1 completely counter-clockwise. Moreover it may be necessary to focus the C.R.T. text by means of R2609 on unit A1 and R2832 on unit A15, until it is readable. It may also be necessary to position the C.R.T. text by means of R2513 (vertical gain), R2533 (vertical position), R2566 (horizontal gain) and R2571 (horizontal position) on unit A1.

Switch-on the service menu. Select CHECK & ADJ and then DISPLAY to initiate the menu DISPLAY 0.

Intensity adjustment:

- Turn the knobs INTENS TRACE and INTENS TEXT 90 degrees from their counterclockwise stop.
- Adjust R2637 on unit A1 so that the pattern and the text are just visible.

Focus and astigmatism:

- Put controls FOCUS, INTENS TRACE and INTENS TEXT in their mid position.
- Adjust R2609 on unit A1 (focus) and R2832 on unit A15 (astigmatism) for a sharp and well-defined test pattern. Check also that the points are exactly round; also during changes in the INTENSITY setting.

- Now the display switches ...
  figure 9.1.
  Adjust R2334 on unit A2 so that the vertical jump of the small horizontal lines (marked with a and b in figure 9.1) is minimal (max. allowed jump 0,1 div).

Variable horizontal gain balance:

- Select service menu DISPLAY 2 by depressing softkey NEXT one time.
- Adjust R2377 on unit A2 so that the horizontal jump of the dot in centre of the screen is minimal (max. allowed jump 0,1 div).

Compensation of C.R.T.-tolerances:

- Select service menu DISPLAY 3 by depressing softkey NEXT one time.
- Adjust R2571 on unit A1 so that the horizontal position of the dot is in the centre of the screen (max. deviation 0,1 div).
- Adjust R2533 on unit A1 so that the vertical position of the dot is in the centre of the screen (max. deviation 0,1 div).

Vertical Gain:

- Select service menu DISPLAY 4 by depressing softkey NEXT one time.
- Adjust the Yx5 gain R2531 on unit A1 so that the vertical distance between the two horizontal lines is 8 div (max. deviation 0,1 div).

- Select service menu DISPLAY 5 by depressing softkey NEXT one time.
- Adjust the Yx1 gain R2513 on unit A1 so that the vertical distance between the two horizontal lines (c and d in figure 9.1) is 8 div (max. deviation 0,1 div).

- Select service menu DISPLAY 6 by depressing softkey NEXT one time.
- Adjust the Y/5 gain R2516 on unit A1 so that the vertical distance between the two horizontal lines (a and b in figure 9.1) is 8 div (max. deviation 0,1 div).

Horizontal gain:

- Select service menu DISPLAY 5 by depressing PREVIOUS on time.
- Adjust the horizontal gain R2566 on unit A1 so that the distance between the starting points of the small horizontal lines a and b in figure 9.1 is 10 div (max. deviation 0,1 div).

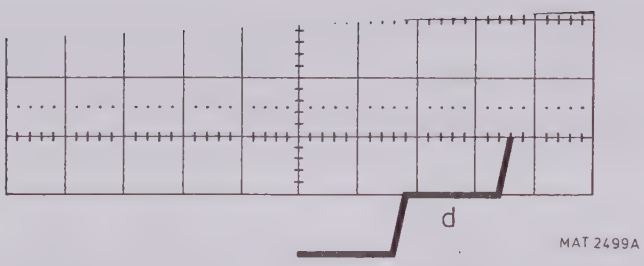


Figure 9.1 Service menu DISPLAY 5.

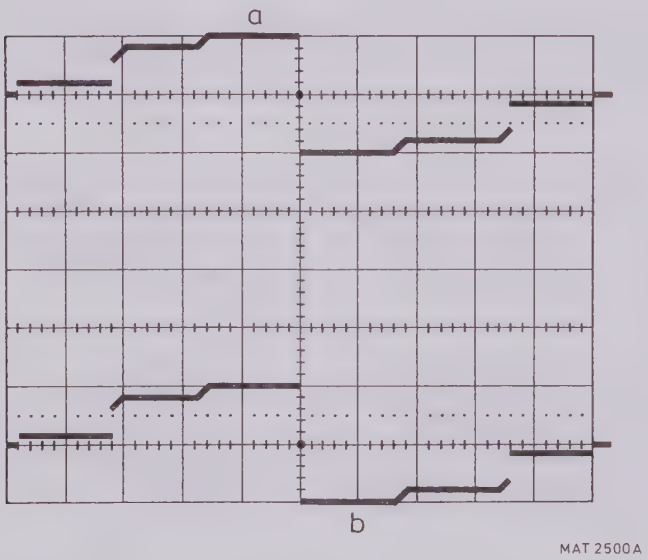


Figure 9.2 Service menu DISPLAY 6.

Overscan suppression:

- Select service menu DISPLAY 7 by depressing softkey NEXT two times.
- Now the pattern of figure 9.3 appears.
- Adjust R2678 on unit A1 so that the test pattern in the left-hand side of the screen is just at its biggest.
- Adjust R2682 on unit A1 so that the test pattern in the right-hand side of the screen is just at its biggest.
- Adjust R2658 on unit A1 so that the test pattern in the bottom side of the screen lies 0,1 div outside the graticule of the screen.
- Adjust R2659 on unit A1 so that the test pattern in the top side of the screen lies 0,1 div outside of the graticule of the screen.
- Now leave the service menu by depressing AUTO SET.

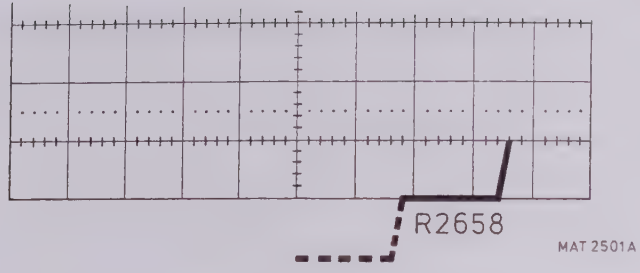


Figure 9.3 Service menu DISPLAY 7.

9.3.5 Adjustment of the frequency doubler:

- Connect a digital d.c. voltmeter between measuring point X8701 on unit A48 and ground (pin 1 of unit A48).
- Set the time-base at 500 ns/div.
- Adjust the voltage at the maximum negative level with C8703 on unit A48.
- Set the time-base at 100 ns/div.
- Adjust the voltage at the maximum negative level with C8702 on unit A48.
- Set the time-base at 500 ns/div.
- Re-adjust the voltage at the maximum negative level with C8703 on unit A48.

9.3.6 P^2CCD pre-adjustment

NOTE: The now following steps must only be done if the instrument is completely misadjusted or after replacement of unit A33.

- Press AUTO SET.
- Set the time-base at 200 us/div.

Jump DIRECT/P^2CCD-mode:

- Connect measuring point X3347 with the ground measuring point X3358 on unit A33.
- Adjust the trace in the mid of the screen with the YPOS control.
- Set the time-base at 500 us/div.
- Adjust the trace in the mid of the screen with R705 on unit A11 (Attainable via side panel).
- Set the time-base at 200 us/div.
- Disconnect the link between measuring point X3347 with ground measuring point X3358.
- Apply a triangular signal of 1kHz/600 mV (pp) to Ch. A and Ch. B.
- Select 100 us/div. 100 mV/div for Ch. A. and Ch. B.

Reference voltage P²CCD gain:

- Connect a digital d.c. voltmeter between measuring point X3343 and the ground measuring point X3358 on unit A33.
- Adjust the voltage to -300 mV (+ or - 20 mV) with R8326. The polarity of X3343 is negative with respect to ground!

BIAS charge:

- Measure the voltage at X3341 (X3348 for ch. B) on unit A33 with a measuring oscilloscope (AC input coupling, 2 ms/div) that is triggered on signal TDUF-2 (X2631 on unit A26).
- Adjust R7939 (R8139 for ch. B) so that the distance between level a and b during the correction stroke in figure 9.4 is 300 mV (+ or - 20 mV).

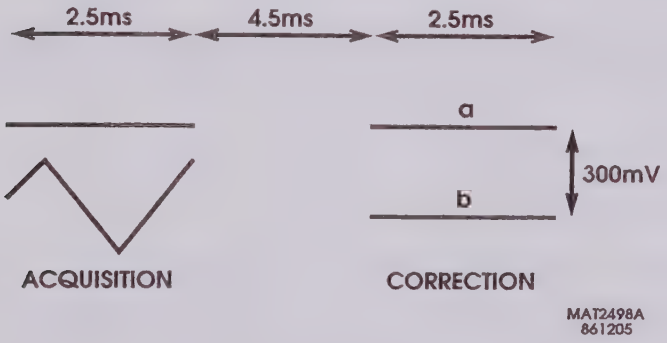


Figure 9.4 Voltage-waveform present at X3341 and X3348.

Pre-adjustment of P²CCD output circuits:

NOTE: The now following steps must only be done if the instrument is completely misadjusted or after replacement of unit A33.

- Put the potentiometers R8419, R8421...R8424, R8426...R8429, R8434, R8436, R8441...R8444, R8446...R8449, R8451 on unit A33 in their mid position.
- Connect the input of the measuring oscilloscope (DC-coupled) with measuring point X3347 on unit A33. The oscilloscope must remain triggered on measuring point TDUF-2 X2631 on unit A26.
- Adjusting of R8419, R8434, R8436 and R8451 on unit A33 influences each a level during the correction stroke. Adjust these four levels to 0 V with these potentiometers.

- Disconnect the measuring oscilloscope and the input signals.

9.3.7 Adjustment of the CORRECTION CIRCUIT (R721).

- Press AUTO SET.
- Select 50 ohm input impedance for channel A.
- Set the input sensitivity at 500 mV/div for both channels.
- Set the time-base at 5 us/div.
- Apply a sine-wave signal with a frequency of 500 kHz and an amplitude of 2 div at channel A.
- Select Average C=4 (VERTICAL MODE - PROCESSING - AVERAGE - C=4).
- Select Peak-Peak measurement (CURSOR/ANALYZE - ON - MEASURE - AMPLITUDE - PEAK).
  1 Position the top of the signal at the top horizontal graticule line with the SHIFT control.
  2 Adjust the amplitude of the generator to 1,05 V peak-peak (+ or - 10 mV) as indicated by the Peak-Peak measurement.
  3 Position the bottom of the signal at the bottom graticule line with the SHIFT control.
  4 Adjust the amplitude to 1,05 V (+ or - 0,01 V) with R721 on A11.
- Repeat the steps 1 to 4 until no more adjustments are needed.
- Check the same (steps 1 to 4) for channel B.
- If the deviation between channel A and B is more than 0,05 div. then the difference must be averaged between both channels.
  eg: Channel A = 1,05 and channel B results in 1,23. Then adjust channel A to 0,96 and check that channel B = 1,14
- Disconnect the input signals.
- Press AUTO SET.

- Apply a calibrated square-wave signal of 2 V/1 kHz to channel A and B and press AUTO.
- Select DC input coupling for Ch. A and B and an input sensitivity of 500 mV/div. Both channels in CAL position.
- Set the time base to 2 ms/div.
- Select ADD mode and B-INVERT via MODE.
- Adjust R5102 on unit A32 for minimal signal display (max. 0,1 div).
- Switch B-INVERT off.
- Disconnect the input signals.

Gain and offset adjustment of P^2CCD output circuits and adjustment of offset single/dual channel:

NOTE: The following adjustments are described for channel A first. The reference numbers for channel B are given between brackets.

- Apply a calibrated square wave signal of 2 V(pp), 1 kHz to the channel A (B) input.
- Switch-on the service menu. Select CHECK & ADJ and then P2CCD A (P2CCD B). The menu P2CCD A Ø (P2CCD B Ø) appears.
- Adjust the trace on the vertical mid of the screen with the frontpanel SHIFT A (SHIFT B) control.
- Depress softkey NEXT to reach service menu P2CCD A 1 (P2CCD B 1).
- Adjust the trace symmetrically around the vertical mid of the screen with R8419 (R8436) on unit A33.
- Adjust the gain (4 div) with R8421 (R8441) on unit A33.
- Depress softkey NEXT to reach service menu P2CCD A 2 (P2CCD B 2).
- Adjust R8434 (R8451) on unit A33, to a minimal jump of the trace (max. allowed jump 0,1 div).
- Depress softkey NEXT to reach service menu P2CCD A 3 (P2CCD B 3).
- If the adjustment is incorrect, the screen shows a square wave with spikes. Adjust with R8426 (R8446) on unit A33 the amplitude of the square wave to minimal (max. amp. 0,1 div).
- Depress softkey NEXT to reach service menu P2CCD A 4 (P2CCD B 4).
- Adjust R8434 (R8451) on unit A33 again to a minimal jump of the trace (max. allowed jump 0,1 div).
- Depress softkey NEXT to reach service menu P2CCD A 5 (P2CCD B 5).
- Adjust the gain (4 div) with R8422 (R8442) on unit A33.

- Increase the frequency of the input signal.
- Adjust the gain (6 div) with R8424 (R8444).
- Depress softkey NEXT to reach service menu P2CCD A 10 (P2CCD B 10).
- Adjust the gain (6 div) with R8429 (R8449).
- Depress softkey NEXT to reach service menu P2CCD A 11 (P2CCD B 11).
- Adjust the gain (6 div) with R8427 (R8447).
- Depress softkey NEXT to reach service menu P2CCD A 12 (P2CCD B 12).
- Disconnect the input signal.
- Adjust R7515 (R7715) to a minimal jump of the trace (max. allowed jump 0,1 div).

- Repeat the steps above, but now for channel B.

- Remove the input signals.

Gain 5 V/div.:

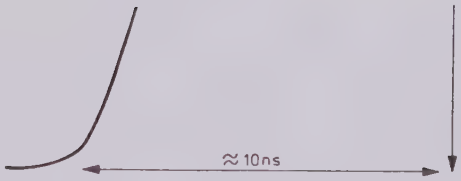
- Apply a calibrated square-wave of 20 V/1 kHz to inputs A and B.
- Press AUTO SET.
- Select DC input coupling for Ch. A and B.
- Check 5 V/div. input sensitivity for Ch. A and B.
- Adjust R5046 on unit A32 (Ch. A) and R5146 on unit A32 (Ch. B) to a vertical deflection of 4 div (max. deviation + or - 0,1 div).
- Remove the input signals.

Offset dual/add:

- Set with shift A and B both traces to the vertical mid of screen
- Select display mode ADD via MODE.
- Adjust the trace in the vertical mid of the screen with R7612 on unit A33.

Offset and gain MIN / MAX and P^2CCD mode:

- Switch on the service menu. Select CHECK & ADJ and then the menu VERTICAL.
- Depress softkey NEXT two times to reach service menu VERTICAL 2. The instrument now switches between MIN/MAX mode on and off.
  When MIN / MAX mode is off, two intensified traces are visible, one for each channel.
  If the adjustment is incorrect each channel shows 2 low intensity traces (when MIN/MAX is on).
- Adjusting of R7566 on unit A33 (P7766 for Ch. B) influences the position of one of these low intensity traces.
  Adjust this trace on the same position as the intensified trace (max. allowed jump 0,1 div.).



MAT2502A
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Figure 9.5 HF-pulse response.

9.3.10 Delta-t adjustment:

- Select the DOTS mode.
- Apply a 50 MHz sine-wave signal to Ch. A.
- Depress AUTO SET.
- Adjust the generator to a sine-wave amplitude to 6 div.
- Set the time base in position 5 ns/div.
- Adjust R8607 on unit A34 so that a continuous smooth sine-wave signal is displayed.
- Depress WRITE and check if the displayed sine-wave stays without discontinuities.
- Select 1 Mohm input impedance for ch. A and B.

9.3.11 Triggering

AC/DC balance EXT TRIG input:

- Apply a 100 Hz/600 mV sine-wave to inputs Ch. A and EXT TRIG.
- Switch-on the service menu. Select CHECK & ADJ and then the menu TRIGGER Ø.
- Adjust R7022 on unit A32 so that the trigger point does not shift (max. allowed shift 0,1 div).

AC/DC balance internal triggering via Ch. A and B:

- Depress softkey NEXT in order to come in the service menu TRIGGER 1.
- Apply a 100 Hz/600 mV sine-wave signal to Ch. A and Ch. B.
- Adjust R5030 on unit A33 so that the trigger point does not shift (max. allowed shift 0,1 div).
- Depress softkey NEXT in order to come in the service menu TRIGGER 2.
- Adjust R5130 on unit A33 so that the trigger point does not shift (max. allowed shift 0,1 div).

- Apply a 100 Hz/120 mV (pp) sine-wave signal to Ch. A.
- Put R7046 on unit A32 fully counterclockwise.
- Adjust R7084 on unit A32 so that the trigger gap lies exactly in the mid between the top and the bottom level of the signal.
- Decrease the generator output signal to 0,4 div.
- Adjust R7156 on unit A32 to a correctly triggered display.
- Increase the signal amplitude to 6 div.
- Check that the trigger point lies exactly in the mid between the top and the bottom level of the signal (max. allowed deviation + or - 0,1 div). If not readjust R7084 and R7156.

LEVEL sensitivity:

NOTE: This adjustment is also done with the use of service menu TRIGGER 4.

- Decrease the generator output signal to 0,4 div.
- Adjust R7046 on unit A32 so that the signal is just triggered.

AUTO/DC balance:

- Apply a 100 Hz/600 mV (pp) sine-wave to Ch. A.
- Depress softkey NEXT in order to come in the service menu TRIGGER 5.
- Adjust R7036 on unit A32 so that the trigger point does not shift (max. allowed shift 0,1 div).

Adjustment of dual triggering:

- Depress softkey NEXT in order to come in the service menu TRIGGER 6.
- Apply a sine-wave signal of 6 div (pp) and a frequency of 100 Hz approx. Adjust the frequency so that the trigger slope flashes between positive and negative triggering.
- Adjust the gap between positive and negative slope to a minimal value with R7116 on unit A32.
- Adjust the vertical symmetry between positive and negative slope with R7129 on unit A32 (max. allowed deviation + or - 0,1 div).

[illegible] (around vertical mid of screen).
Max allowed deviation + or - 0,1 div.

NOTE: If necessary re-adjust R2533 on unit A1 by using service menu DISPLAY 3, so that the vertical position of the dot is in the centre of the screen (max. deviation 0,1 div).

- Depress AUTO SET.

LF square-wave response EXT and EVENTS inputs:

- Apply a square-wave signal of 10 kHz/3 V to input EXT TRIG.
- Select EXT as trigger source.
- Connect the probe of a measuring oscilloscope to pin 1 of mini unit A40 (on unit A32).
- Adjust R4751 on unit A31 to a straight pulse top.
- Increase the generator's square-wave amplitude to 30 V.
- Select EXT:10 as trigger source.
- Adjust R4753 on unit A31 to a straight pulse top.
- Apply a square-wave signal of 10 kHz/3 V to input EVENTS.
- Connect the probe of the measuring oscilloscope to pin 1 of mini unit A43 (on unit A32).
- Adjust R4851 on unit A31 to a straight pulse top.

NOTE: R4853 on unit A31 needs no adjustment.

AUTO offset level:

- Apply a sine-wave voltage 1 kHz/100 mV to Ch. A.
- Press AUTO SET.
- Select 100 mV/div for Ch. A.
- Adjust R7052 on unit A32 so that the voltage at measuring point X7007 on unit A32 is 0 V (max. allowed deviation 100 mV). Voltage must be measured with a digital multimeter (d.c. voltage range).

9.3.12 Output voltage calibration generator:

The amplitude of the calibration signal must lay between 0 and +1 Volt. This must result in a read-out of 500 mV on a digital a.c.-r.m.s. or d.c. millivoltmeter since the duty cycle of the signal is 50%. If not, re-adjust R2703 on unit A1.

right in the bottom of the screen.

- Measure with a digital multimeter (d.c. voltage range) the maximum voltage at the vertical plot output (red banana plug, black is mass). This voltage must be adjusted to 1000 mV by means of R2738 on unit A1.
- Measure with a digital multimeter (d.c. voltage range) the maximum voltage at the horizontal plot output (blue banana plug, black is mass). This voltage must be adjusted to 1000mV by means of R2728 on unit A1.
- Select 20 ms/DT via the menus PLOT, SELECT and ANALOG.
- Press AUTO SET.

9.3.14 Fan Check

- Check that the fan runs.
- Measure the d.c. voltage between X4611 and the positive pole of capacitor C4629 on unit A20 with a digital voltmeter. This voltage should be higher than 16 V.

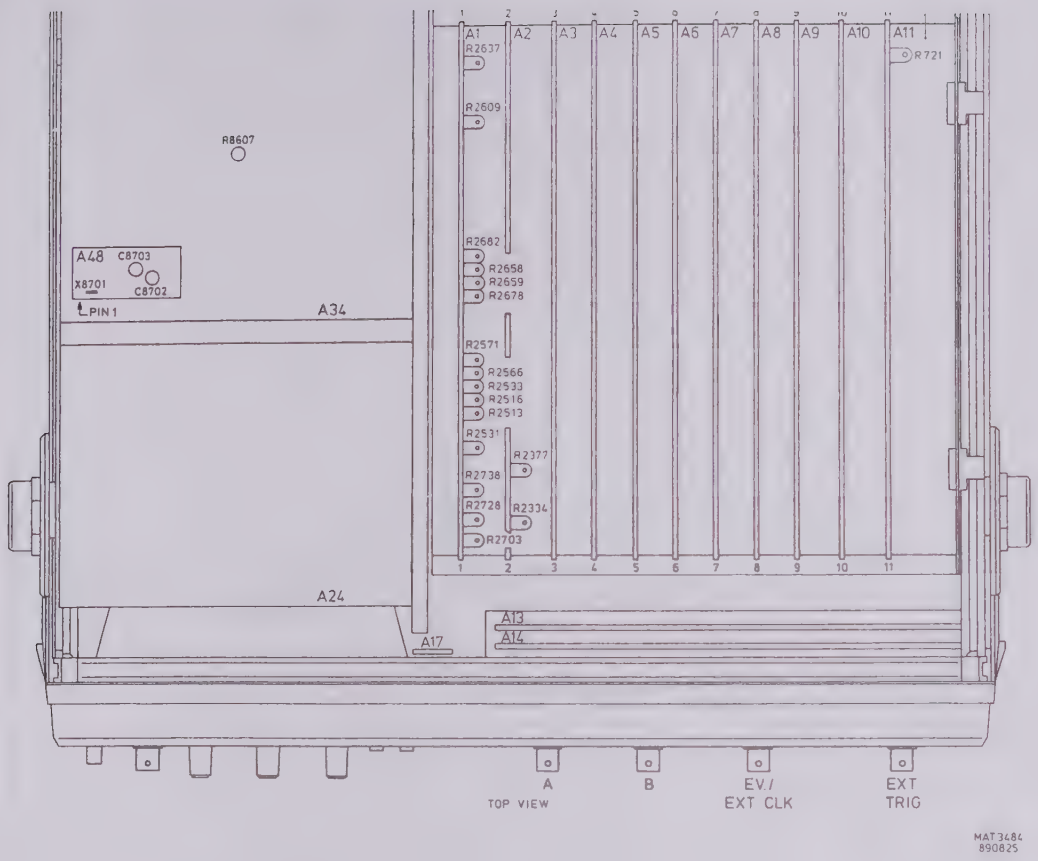


Figure 9.6 Position of adjusting elements - top side.

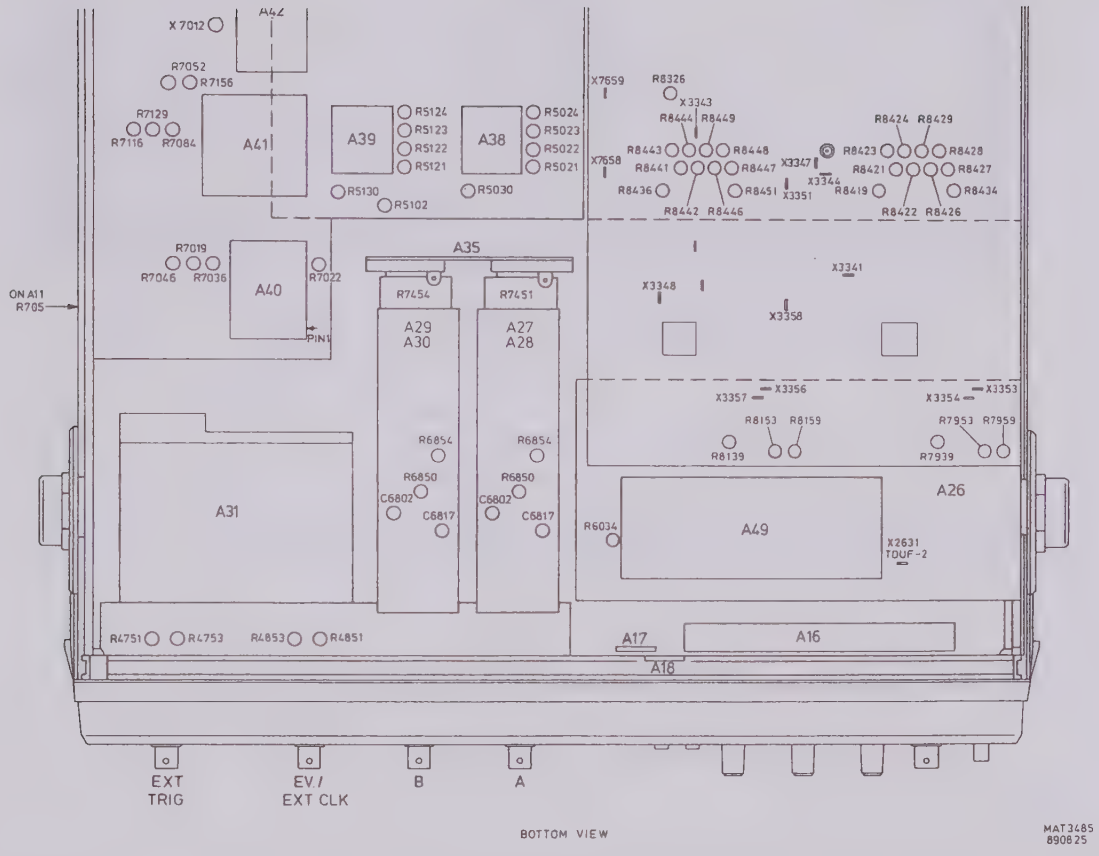


Figure 9.7 Position of adjusting elements - bottom side.

DISASSEMBLING AND ASSEMBLING 10

DISASSEMBLING AND ASSEMBLING

CONTENTS

10.0	Disassembling and assembling	10-1
10.1	Removing the instrument covers	10-1
10.2	Replacements	10-1
10.3	Removing the plug-in printed circuit boards	10-2
10.4	Removing and mounting the rear panel	10-2
10.5	Access to the management unit and the ccd logic unit	10-5
10.6	Removing the adaption unit, the vertical attenuators and the external trigger unit	10-7
10.6.1	Removing the adaption unit	10-7
10.6.2	Removing the vertical attenuator units	10-7
10.6.3	Disassembling of a vertical attenuator unit	10-7
10.6.4	Removing the external trigger unit	10-9
10.7	Removing the front unit	10-9
10.7.1	Removing the complete front unit	10-9
10.7.2	Removing the knobs of the rotary controls	10-10
10.7.3	Removing the textplate	10-10
10.8	Removing the C.R.T. control unit	10-10
10.9	Removing the softkey unit	10-10
10.10	Removing and installing the cathode ray tube	10-11
10.11	Removing the carrying handle	10-12

10.0 DISASSEMBLING AND ASSEMBLING

10.1 REMOVING THE INSTRUMENT COVERS

See chapter 5, section 5.2.

WARNING: The opening of the covers exposed live parts and also accessible terminals may be live.
The instrument shall be disconnected from all voltage sources before any replacement or maintenance or repair, during which the instrument will be opened.
Capacitors inside the instrument may still be charged, even if the instrument has been separated from all voltage sources.

To avoid shocks the high voltage capacitor C4616 on POWER 2 unit A20 at the inner side of the rear panel has to be discharged. This can be done by connecting a 1 Mohm resistor from the node of capacitor C4616 and the EHT transformer D4601 to the chassis of the oscilloscope. This node is marked with an X in figure 10.1.

The E.H.T. cable is permanently connected to the E.H.T. unit (disconnection at C.R.T.).
When the E.H.T. cable to the post-acceleration anode of the C.R.T. is disconnected at the C.R.T. end, the E.H.T. cable must be discharged immediately by shortening it to the chassis of the oscilloscope.

10.2 REPLACEMENTS

Standard parts

Electrical and mechanical replacement parts can be obtained through your local Philips organisation or representative. However, many of the standard electronic components can be obtained from other local suppliers.
Before purchasing or ordering replacement parts, check the parts list for value tolerance, rating and description.

NOTE: Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special parts

In addition to the standard electronic components, some special components are used.
These components are manufactured or selected by Philips to meet specific performance requirements.

Transistors and integrated circuits

Transistors and integrated circuits should not be replaced unless they are actually defective. If removed from their sockets during routine maintenance return them to their original sockets. Unnecessary replacement or switching of semiconductor devices may affect the calibration of the instrument.
When a transistor is replaced, check the operation of the part of the instrument that may be affected.

WARNING: Handle silicone grease with care. Avoid getting silicone grease in the eyes. Wash hands thoroughly after use.

Any replacement component should be of the original type or a direct replacement. Bend the leads to fit the socket and cut the leads to the same length as on the component being replaced.

10.3 REMOVING THE PLUG-IN PRINTED CIRCUIT BOARDS

The plug-in boards are:

A1 Final amplifier
A2 Display dac
A3 Display control
A4 Display memory
A5 MRAM + ACL
A6 UP board
A7 Option
A8 DPU control
A9 DPU
A10 Option
A11 ADC + T&H

These plug-in units can easily be removed (after removing the bracket and the various cables) with the aid of the red handles.

If a plug-in board is removed it can be placed on an extension board to do measurements.
For more information about the extension board see section 13.3.4.

WARNING: The plug-in boards have to be replaced at the correct locations to prevent damage.

10.4 REMOVING AND MOUNTING THE REAR PANEL

- Take security measures (see section 10.1).
- Remove 4 screws marked with A in figure 10.1.
- Remove 4 opposite screws at the bottom side.

WARNING: If the screws are removed the oscilloscope may not stand on its rear side.

- Remove 2 screws marked with B.
- Remove the remaining opposite screw at the bottom side.
- Remove 4 nuts (2 on each side) with washers, marked with C.
- Slacken 4 screws (2 on each side) marked with D a few turns.
- Slacken the screws of the fixation points of the E.H.T. cable to the C.R.T.
- Disconnect the analog plot out cable on unit A1.
- Pull the rear panel out of the oscilloscope and lay it down, thereby shifting through the E.H.T. cable and the analog plot out cable.

In this situation the oscilloscope can operate and measurements can be done.
Because connector X4604 of unit A20 is disconnected, the high voltage is not present, so nothing can be seen on the screen.
Also the power supply is not fully loaded, because the management unit A25 is not connected.
To test the power supply under full load, the extension board for the plug in units can be used as shown in figure 10.2.
It is also possible to use a dummy load, which is specified in section 13.2.

WARNING: If the osciloscope is operating, parts of POWER 1 unit A19 are at mains potential.

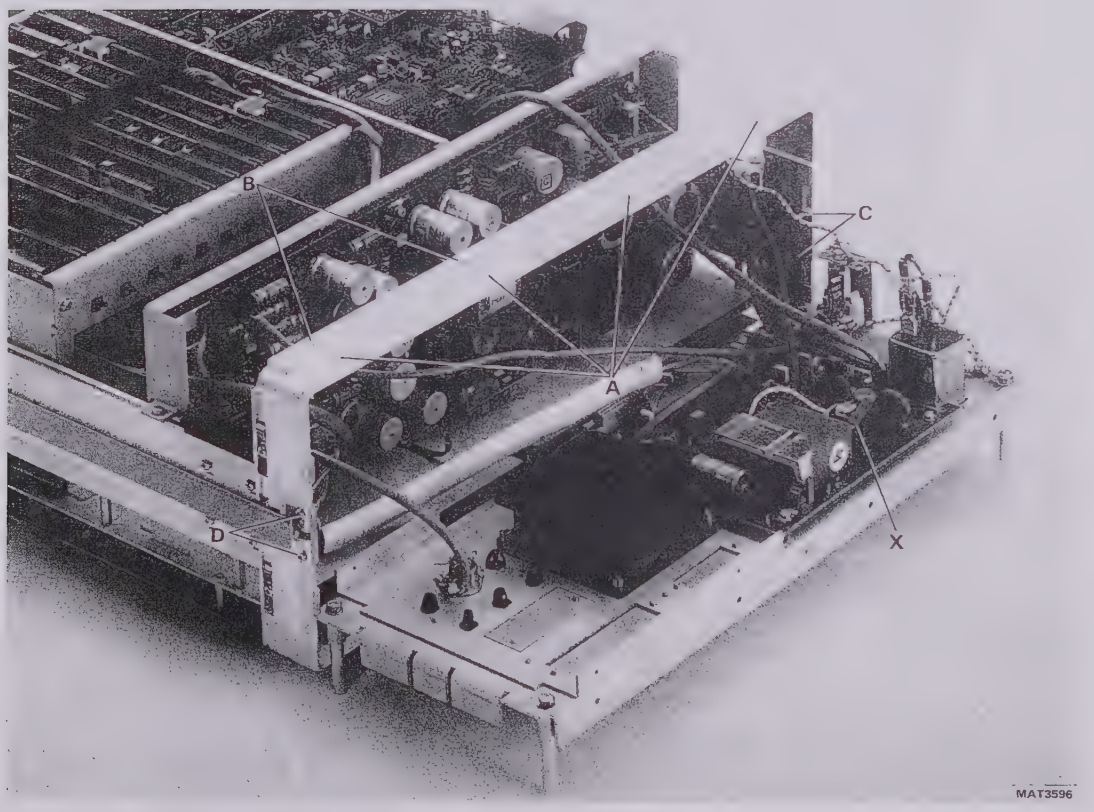


Figure 10.1 Removing the rear panel.

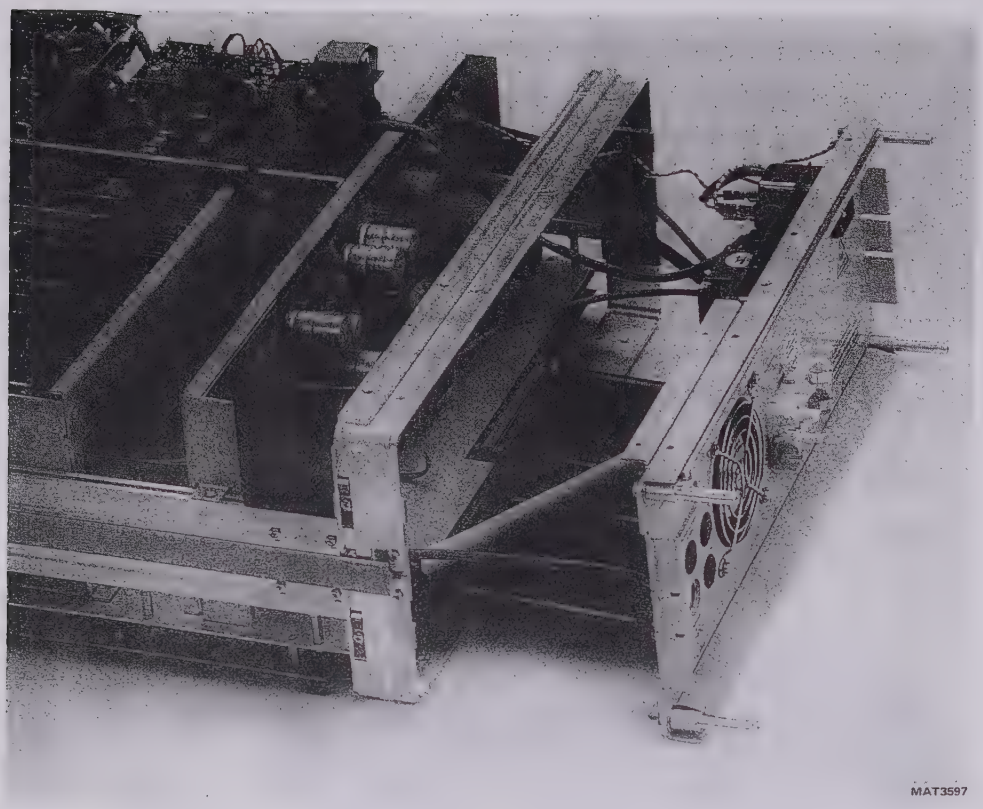


Figure 10.2 Use of the extension board for the rear panel.

To reinstall the rear panel the above mentioned steps have to be done in reverse order.

Special attention is asked for:

- The cable from the mains switch to connector X4401 on unit A19 has to be positioned as much as possible between capacitors C4416 + C4417 and the side of the oscilloscope, to pick up as less interference as possible from transformer T4401.
- The high voltage cable from the E.H.T. transformer should not touch transistor V4612.

10.5 ACCESS TO THE MANAGEMENT UNIT AND THE CCD LOGIC UNIT

To get access to the management unit A25 and the CCD logic unit A26 the P^2CCD unit A33 and the vertical signal unit A32 can be turned up as shown in figure 10.3.

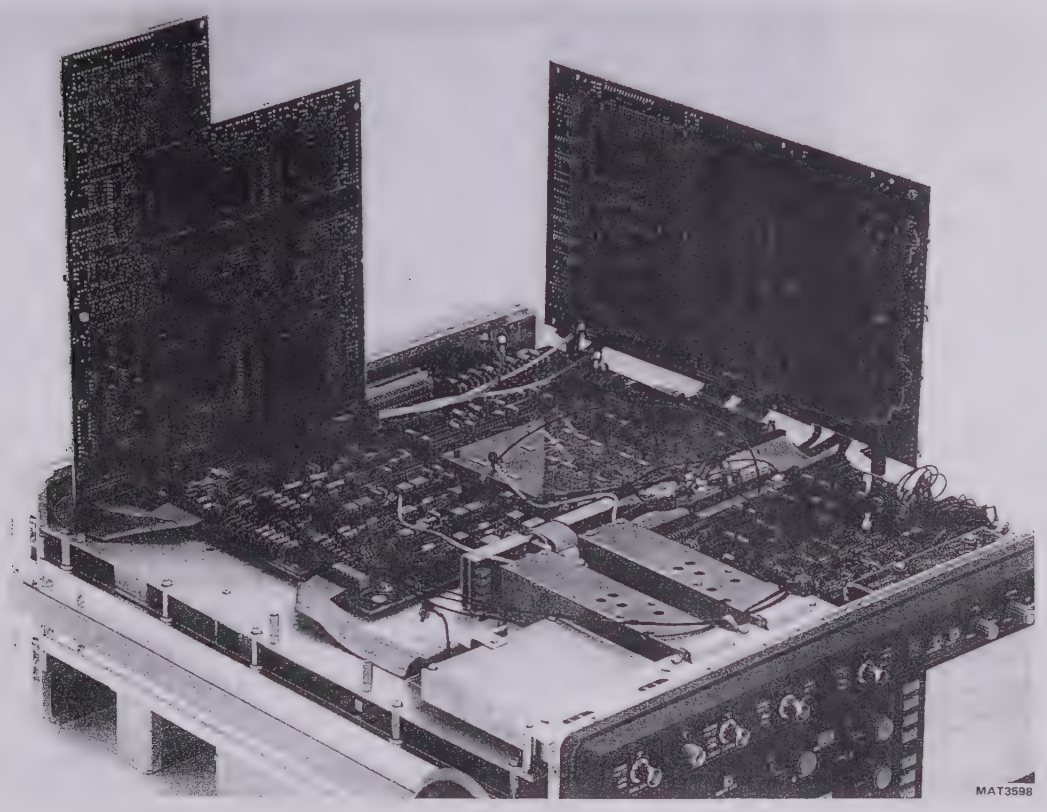


Figure 10.3 Access to the management unit and the CCD logic unit.

The vertical signal unit can be turned up as follows (see figure 10.4):

- Disconnect all coaxial wiring.
- Remove 2 screws marked with A and remove the profile.
- Remove 2 distance pieces that were below the profile.
- Remove 5 remaining screws.
- Turn the unit up and place it on the two supports as shown in figure 10.3.

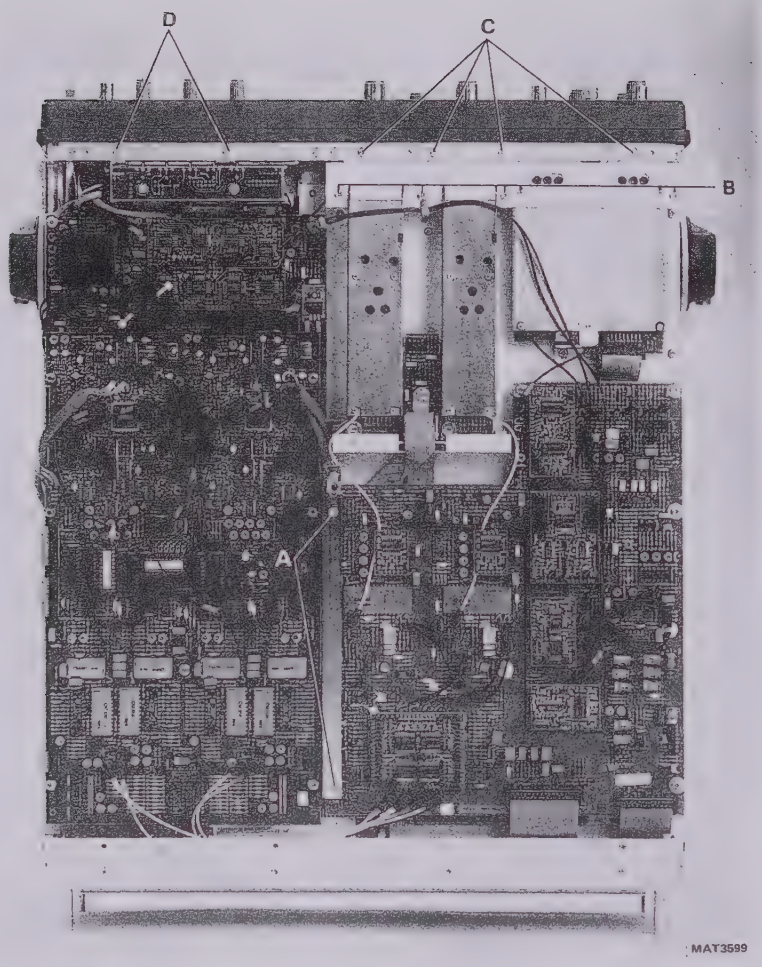


Figure 10.4 Bottom side of the oscilloscope.

The P^2CCD unit can be turned up as follows (see figure 10.4):

- Disconnect all coaxial cables
- Remove 9 screws.
- Turn the unit up and place it on the two supports as shown in figure 10.3.

Now the shielding plate over the management unit, which is fixed with 3 spacers, can be removed.

In this position the oscilloscope can operate, but will not function properly. Nevertheless certain measurements can be done on the units A25 and A26. If longer coaxial cables are used (see section 15.3.2) the instrument can operate completely.
To reinstall the boards the steps have to be done in reverse order. Care should be taken of the reconnection of the coax cables at the right points. The cables should also be repositioned as much as possible to their original positions.
Note that the screw on the corner of the p.c.b. near IC N7913 is equipped with an isolating washer.

NOTE: If one of the coax cables should be replaced care should be taken that the length difference between this cable and cables with similar signals (e.g. balanced signals) is less than 1 cm, to avoid delay time differences.
Coax cables between the driver unit A24 and the P^2CCD unit A33 can only be replaced as a complete set.

10.6 REMOVING THE ADAPTION UNIT, THE OFFSET ADAPTATION UNIT, THE VERTICAL ATTENUATORS AND THE EXTERNAL TRIGGER UNIT

10.6.1 Removing the adaption unit (unit A35) and the offset adaptation unit (unit A50)

- Remove 2 screws marked with A in figure 10.4 and remove the profile.
- Remove the screw and the nylon clamp between the vertical attenuators that locks the flatcable to the offset adaption unit.
- Disconnect the flatcable to the offset adaptation unit.
- Remove the distance piece, that fixes the offset adaption unit and remove the offset adaptation unit.
- Slacken the distance piece between the vertical attenuators that fixes the adaption unit.
- The unit can now be slided backwards and removed from the mounting plate.

10.6.2 Removing the vertical attenuator units

- Remove the offset adaptation unit and the adaption unit (see section 10.6.1).
- Disconnect the coax cables to the vertical signal unit A32.
- Remove 6 screws marked with B in figure 10.4.
- Slacken 4 screws marked with C in figure 10.4.
- The attenuators can be slided backwards and removed.

10.6.3 Disassembling of a vertical attenuator unit.

- Remove the two small screws that fix the shielding case and slide the case from the unit in the direction of the BNC input connector.

NOTES:
- The unit can be measured under operating conditions if it is reconnected to the adaption unit and if all wiring is connected.
- It is strongly recommended to take notice of this chapter and belonging figure 10.5 before starting the job.

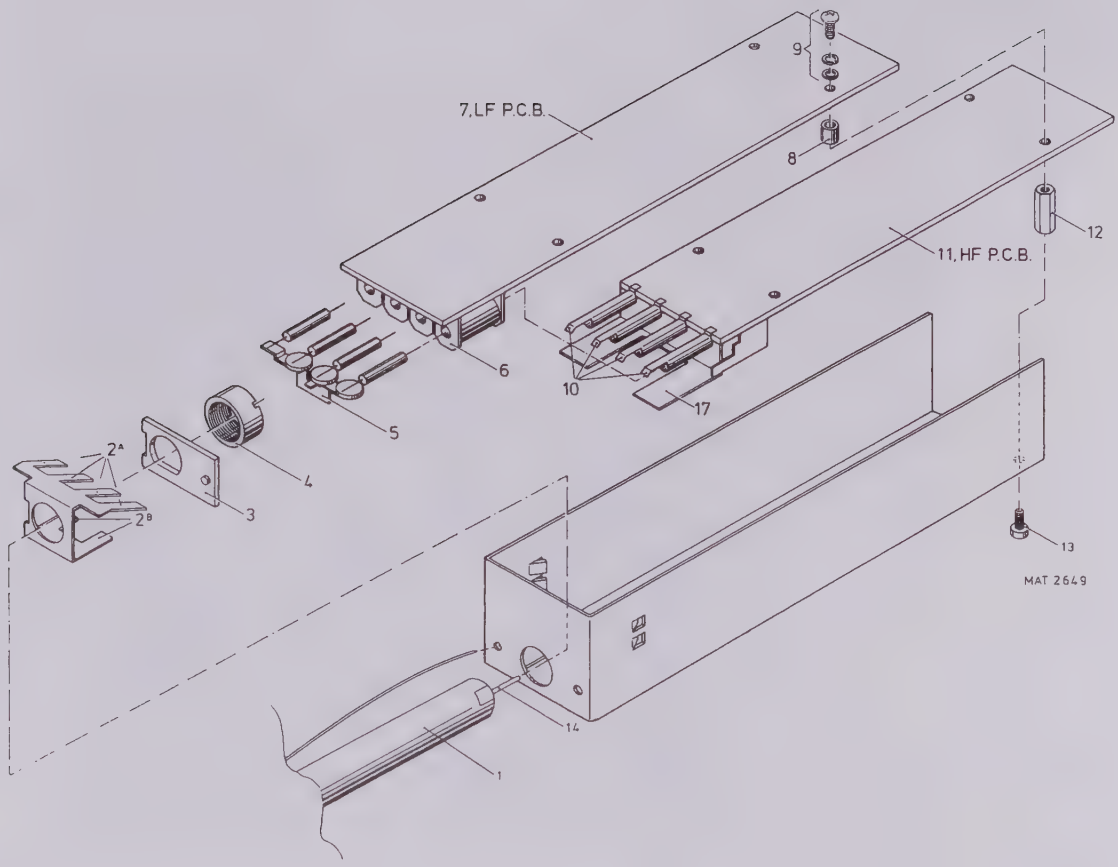


Figure 10.5 Exploded view of attenuator.

- Put the unit on your bench with the LF-p.c.b. upwards.
- Unsolder the wire of the probe detection contact from the soldering tag on the LF-p.c.b.
- Remove the capacitor between the shielding case and the soldering tag on the LF-p.c.b.
- Unsolder the four shielding cans (10) from the tags of the earth bracket (2A).
- Put the unit on your bench with the HF-p.c.b. upwards.
- Unsolder the two tags (2B) of the input earth bracket from earth bracket (17).
- Remove two screws (13) that attach the p.c.b.´s to their mounting bracket.
- Put the unit on your bench with the HF-.p.c.b. upwards and unsolder the signal tag (14) from the bracket with the input capacitors (5). This must be done very quickly in order to avoid that the input capacitors are overheated.
- The subassembly consisting of the LF and HF p.c.b. can be slided out of the mounting bracket.

NOTE: After the above actions, the 50 Ohm termination resistor array on the HF-p.c.b. can be interchanged.

- The BNC-socket can be separated together with the tube and the probe detection contact from the bracket with a special tool that fits on the slotted nut (4) of the tube. More information about this tool is given in section 13.3.1. Together with the removal of the tube the separate parts 2,3 and 4 can be taken apart.

- If you want to separate the HF (11) and LF (7) p.c.b.´s, it is necessary to remove the glass reed switches from their coils. For this purpose the bracket with the input capacitors (5) must be unsoldered from the reed relays. After this the other side of the reed relay can be unsoldered from the HF-p.c.b. and it can be slided out of the coil. Also the resistor between the bracket and the LF-p.c.b. must be unsoldered at the LF-p.c.b. Now the hardware (4x) that fixes the HF and LF p.c.b. together (9,8,12) can be removed and the HF-p.c.b. (11) with its four shielding cans (10) can be slided out of the reed relay coils (6) on the LF-p.c.b. (7).

10.6.4 Removing the external trigger unit

- Remove the electrical wiring to the unit.
- Remove the support next to the flatcable connector.
- Remove 6 screws marked with B in figure 10.4.
- Slacken 4 screws marked with C in figure 10.4.
- The unit can be slided backwards and removed.
- To disassemble the unit, remove the three remaining small screws, remove the bracket and slide the shielding case from the unit.

10.7 REMOVING THE FRONT UNIT

10.7.1 Removing the complete front unit

- Remove 3 screws marked with A (see figure 10.6).
- Slacken 3 screws marked with B.
- Slacken 2 screws marked with C.
- Carefully press the front unit via the front side out of the instrument.
- Disconnect the two flatcable connectors from the front unit.
- Now the front unit itself can be disassembled easily.

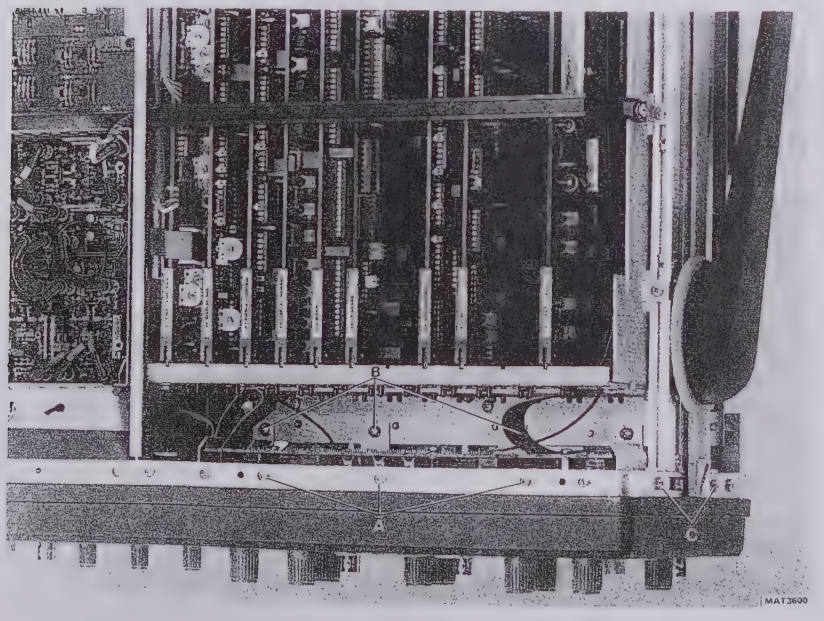


Figure 10.6 Removing the front unit.

10.7.2 Removing the knobs of the rotary controls

- Remove the knob cover.
- Slacken the internal nut.
- Pull off the knob.

10.7.3 Removing the textplate

- Remove the complete front unit as described in section 10.7.1.
- Remove all the knobs of the rotary controls (see section 10.7.2).
- Remove 5 slotted nuts which fix the textplate and the aluminium housing to the unit. This can be done with a special tool for slotted nuts as described under section 13.3.1.
- Remove the textplate.

NOTE: For a repair of a defective rotary control the textplate has not to be removed. Only the p.c.b. with the leds and the fototransistors (unit A14) has to be removed then.

10.8 REMOVING THE C.R.T. CONTROL UNIT (A16 + A18)

- Turn unit A33 up as described in section 10.5.
- Remove the fixation screws of unit A26 and shift the unit a little backwards.
- Remove the three C.R.T. control knobs as follows:
  - Remove the knob covers.
  - Slacken the internal screws.
  - Pull the knobs off.
- Remove the electrical wiring.
- Remove 2 screws on the front profile marked with D (see figure 10.4) and pull the unit backwards.

NOTE: When reinstalling the unit take care of the correct position of the marks on the caps of the knobs.

10.9 REMOVING THE SOFTKEY UNIT (A17)

- Remove the front unit as described in section 10.7.1 until the unit is from the instrument and remove the bezel with the contrast filter.
- Remove the caps from the softkeys (8x).
- Remove 3 fixation screws of the support of the softkey unit inside the frontpanel hole.
- Remove the support with the softkey unit through the frontpanel hole.
- Remove the softkey unit from the support and disconnect the flatcable.

NOTE: When the unit is re-installed, the middle screw of the support is turned in a small metal bezel support, which might get lost.

TROUBLE SHOOTING AND SERVICE DIAGNOSTICS 11

TROUBLE SHOOTING

CONTENTS

11.0 Trouble shooting..... 11-1
11.1 Introduction..... 11-1
11.2 Trouble shooting techniques..... 11-1
11.3 Trouble shooting hints..... 11-2
11.4 Description of the diagnostic software..... 11-3
11.5 Recalibration after repair..... 11-19

- Connect a signal of 100 Hz 500 mVpp to the disconnected coaxial cable connector. This signal is applied to the ADC unit A11 via the coaxial cable.
- Check that the signal is visible on the C.R.T. with some distortion. The signal is not stable triggered, but changes of frequency, amplitude or waveform should become visible.
- If no traces are visible then check:
    - Trace intensity control
    - Z-control
    - Units A3, A4, A5, A8, A9, A11

- If the traces become visible in the way as described, the fault is in the acquisition section. This is unit A33 or one of the units between the signal inputs and A33 (A27 to A32) or in the units, which control these units (A25, A5, A26, A49, A34, A48).

- If the DPU operates properly, the signal IL$\emptyset$2--LT gives regularly negative pulses.

- If the acquisition operates properly, HDOF--LT on unit A26 gives regularly positive pulses. The rising edge of the pulse is the start of a new acquisition.

- If certain time base settings do not operate properly, the mode overview in section 8.33.3 may give an indication of where the fault is.

11.4 DESCRIPTION OF THE DIAGNOSTIC SOFTWARE

11.4.1 Introduction

The diagnostic software consists of three parts:

- the power up routine
- softkey selectable diagnostic software
- hardware selectable diagnostic software

It is recommended to read the concerning hardware description first (chapter 8), before using the diagnostic software.

Each part will be described in the following subsections.

11.4.2 The power up routine

The power up routine is initiated every time the oscilloscope is turned on or when the microprocessor is restarted by the watchdog circuit (unit A6). It performs the following actions:
- First all leds on the front panel are turned on during 3 seconds.
- The leds REP ONLY and NOT TRIG´D are extinghuished.
  Now the part of the microprocessor RAM (unit A5) which does not contain data that should be retained, is tested. If the test fails, the leds stay off and the address where the failure is, is continuously read and written by the microprocessor. This makes tracing of the failure easier.

- The led REP ONLY is turned on, so only led NOT TRIG´D is off. Now the TEXT MEMORY is tested. The TRACE MEMORY can not be tested, because these data should be retained.
  If the test fails, the led NOT TRIG´D stays off and the address where the failure is, is continuously read and written by the microprocessor, as with the previous test.
- The led NOT TRIG´D is also turned on, so all leds are on.
  Now the part of the microprocessor ram (unit A5) that contains settings, is tested by means of a checksum test.
  If a fault is found in a setting belonging to a stored trace, this setting is cleared.
  If a fault is found in a programmed front setting, the concerning front setting and all front setting which are stored at higher addresses are cleared. Because all settings are stored in time order of entrance, an "arbitrary" part of the settings is cleared.
  Next the actual front setting is checked. If it has a checksum fault an AUTO SET is initiated, else the oscilloscope is set according to the values found in the ram.
  It is this last routine that initiates AUTO SET after power up, if no backup batteries are installed.
- Finally the battery voltage is tested, and if it is too low, a message appears on the CRT screen.
  The battery check is only done in this stage of the power up routine; nowhere else during operation.
  The oscilloscope is now ready for operation.

Resumed:
- If the power up routine hangs up with both leds REP ONLY and NOT TRIG´D off, the microprocessor ram is defective.
- If it hangs up with only led NOT TRIG´D off, the display ram is defective.
- If stored traces or programmed front settings are cleared or an AUTO SET is initiated, while the backup batteries are OK, the contents of the microprocessor ram is destroyed. This may be caused by the oscilloscope being turned off at the moment the microprocessor was writing in the ram, but if it happens every time the oscilloscope is turned on the ram itself is broken.

NOTE: If the power up routine hangs up, the watchdog circuit on unit A6 is triggered regurlarly by the microprocessor, to prevent a new initiation of the power up routine again.

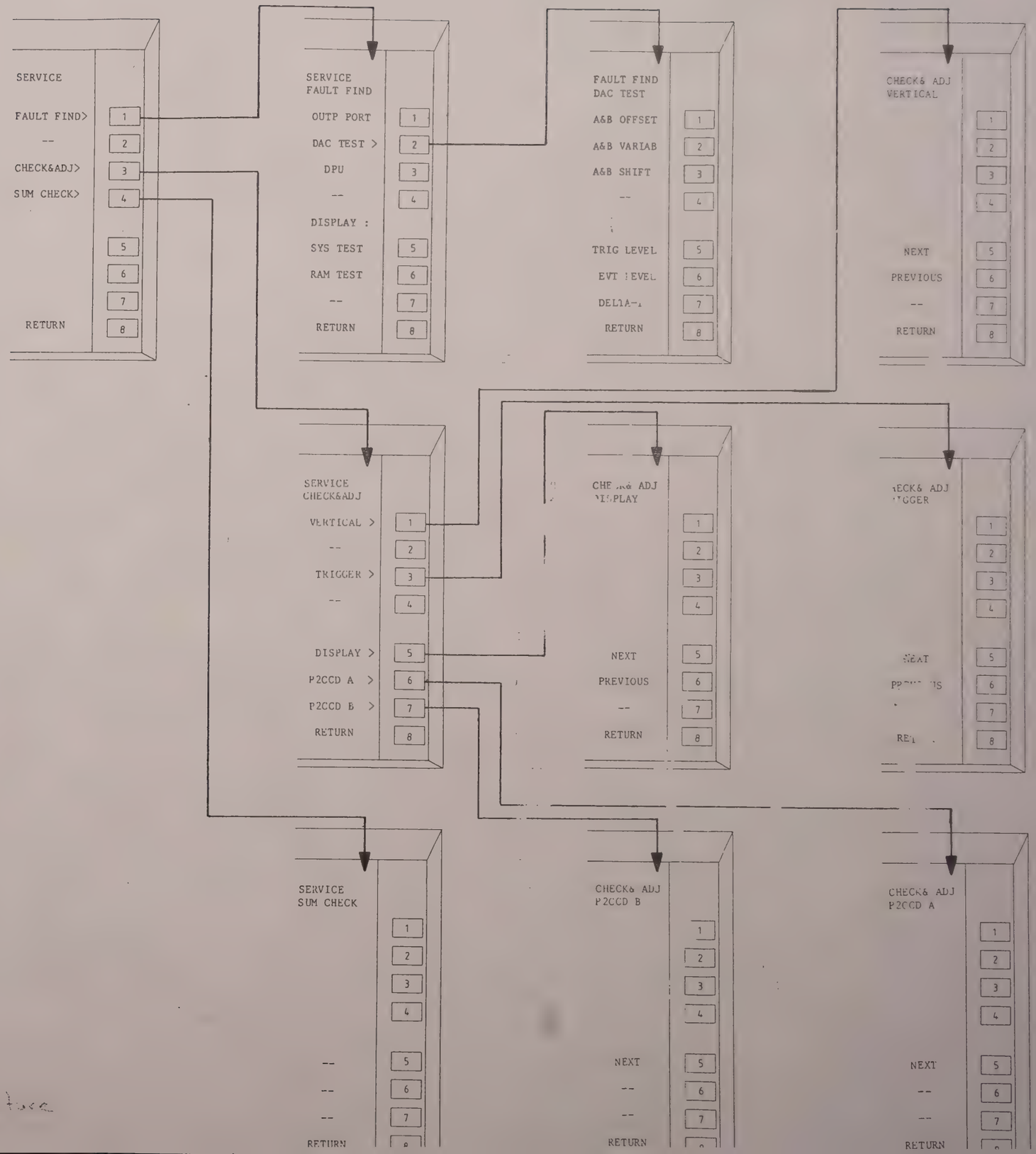


Figure 11.1 Service select menu structure

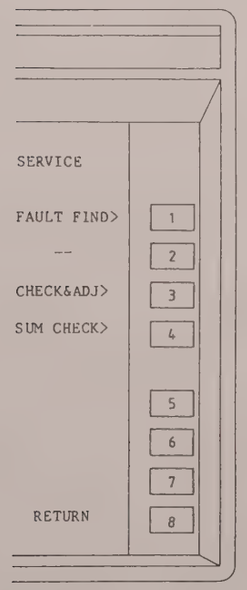
11.4.3 Softkey selectable diagnostic software

If some functions of the oscilloscope do not operate properly, the softkey selectable diagnostic software can be used to detect the defective hardware circuits.
This diagnostic software also contains a number of check and adjust routines (see chapter 9).

The routines destroy the actual front setting. Therefore returning to normal operation via the softkeys generates an AUTO SET.
It is always possible to return to normal operation by pressing the green pushbutton AUTO SET.
When a routine is operative and a setting is done on the front panel, the following message is given:

Instrument in SERVICE mode.
Changes are executed, but not always correct.

This is done because settings can not be executed if the concerning hardware is controlled by the selected diagnostic routine.



After pushing the upper and the lower softkey, the SERVICE menu appears on the screen. This menu allows selection of a range of fault find routines and a range of check & adjust routines (see figure 11.1)

Information about the software release is displayed at the left side of the softkeys 5 to 7.

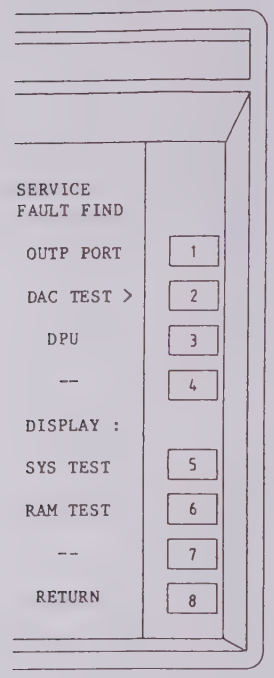
A message

For correct SERVICE handling:
*** switch off any active OPTION ***

may appear.

Options may be installed in the instrument, but they may not be active when the softkey selectable diagnostic software is used.
E.g. an interface should not display TIME and/or DATE.

1 FAULT FIND>



If FAULT FIND is selected the SERVICE FAULT FIND menu is displayed and a number of fault finding routines can be selected.

Each test can be stopped by pressing the same softkey again or by selecting another test.

In this part of the diagnostic software the traces are suppressed.

1 1 OUTP PORT

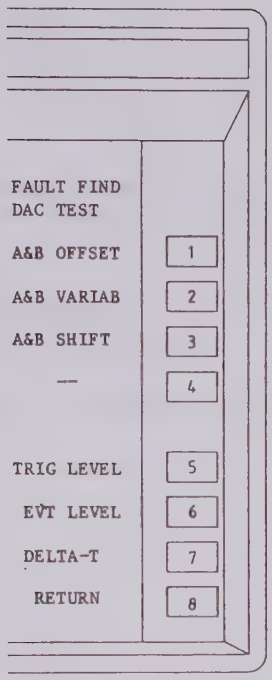
If OUTP PORT is selected an alternating pattern of zeroes and ones with a frequency of 1.6 Hz is generated at the following output ports on the management unit A25:

Name	IC nrs	Signal destination
delta-t control latch	D427	A34
attenuator control latch A	D409 + D411	A28 + A32
attenuator control latch B	D412 + D413	A29 + A32
vertical signal switch latch	D417	A33
trigger latches	D421 + D422	A31 + A32
P^2CCD output control latch	D436	A33

This test can be used to test the proper operation of these latches and their controlling hardware by checking all the outputs with an oscilloscope.

11

1 2 DACTEST>



If DACTEST is selected, the FAULT FIND DAC TEST menu is displayed.
With this menu all DAC´s in the acquisition section of the oscilloscope can be tested, by checking their output voltage with another oscilloscope.

Because the softkeys are only checked after a cycle of a test and the cycle can take some time (up to a few seconds), it may be necessary to keep a softkey pressed down a while to get the desired action.

1 2 1 A&B OFFSET

If A&B OFFSET is selected, a sawtooth signal is generated at the outputs of the OFFSET DACs of channel A and B (N403 and N404 on unit A25). During the slope of the sawtooth the digital values at the inputs of these 14 bit DACs is incremented by 16 every time. So the 4 less significant bits are not tested. The output voltage ranges from -5 to +5 V.
The period is 0,6 s.

Measuring points:

OSA: adaptation unit A35, X7451, pin 13
OSB: adaptation unit A35, X7451, pin 11

1 2 2 A&B VARIAB

If A&B VARIAB is selected, sawtooth signal is generated at the output of the SHIFT-VAR. DAC (N401 on unit A25). The output voltage is sampled and held by the Sample & Hold circuits VAR A and VAR B (N413 and N416 on unit A25).
During the slope of the sawtooth the digital value at the input of the 12 bit DAC is incremented by 4 every time. So the 2 less significant bits are not tested.
The output voltage of the DAC ranges from 0 V to -5 V.
The input and output voltages of the S&H circuits range from -5 V to +5 V.
The period is 2,5 s.

Measuring points:

DAC output voltage: N401 pin 18 on unit A25
S&H input voltages: N413 or N416 pin 3 on unit A25
VGA: vertical signal unit A32, X5206, pin 11.
VGB: vertical signal unit A32, X5206, pin 12

1 2 3 A&B SHIFT

If A&B SHIFT is selected, a sawtooth signal is generated at the output of the SHIFT-VAR. DAC (N401 on unit A25). The output voltage is sampled and held by the Sample & Hold circuits SHIFT A and SHIFT B (N412 and N414 on unit A25).
During the slope of the sawtooth the digital value at the input of the 12 bit DAC is incremented by 4 every time. So the 2 less significant bits are not tested.
The output voltage of the DAC ranges from 0 V to −5 V.
The input and output voltages of the S&H circuits range from −5 V to +5 V.
The period is 2,5 s.

Measuring points:

DAC output voltage: N401 pin 18 on unit A25
S&H input voltages: N412 or N414 pin 3 on unit A25
SHA: vertical signal unit A32, X5206, pin 15.
SHB: vertical signal unit A32, X5206, pin 9.

Note: SHA and SHB should be measured with the flatcable connector X5206 disconnected from A32. The signals can be measured on the flatcable part of the connector. If the connector is fitted, the voltages of SHA and SHB range from −6 V to +2 V.

1 2 4 --

1 2 5 TRIG LEVEL

If TRIG LEVEL is selected, a sawtooth signal is generated at the output of the TRIGGER LEVEL DAC (N407 on unit A25).
During the slope of the sawtooth the digital value at the input of this 14 bit DAC is incremented by 16 every time. So the 4 less significant bits are not tested.
The output voltage range from 0 V to +5 V.
The period is 0,5 s.

Measuring points:

TRDULV: vertical signal unit A32, X7014, pin 11.
TRLV : vertical signal unit A32, X7014, pin 23.

1 2 6 EVT LEVEL

If EVT LEVEL is selected, a sawtooth signal is generated at the output of the TRIGGER EVENT DAC (N406 on unit A25).
During the slope of the sawtooth the digital value at the input of this 14 bit DAC is incremented by 16 every time. So the 4 less significant bits are not tested.
The output voltage range from 0 V to +5 V.
The period is 1 s.

Measuring point:

TREVLV: external trigger unit A31, X4703, pin 2.

1 2 7 DELTA-T

If DELTA-T is selected, a sawtooth signal is generated at the output of the delta-t DAC (N8511 on clock unit A34).
During the slope of the sawtooth the digital value at the input of this 14 bit DAC is incremented by 16 every time. So the 4 less significant bits are not tested.
The output voltage range from 0 V to +11 V.
The top of the sawtooth is slightly clamped.
The period is 160 ms.

Measuring point:

Clock unit A34, IC N8512, pin 6.

1 2 8 RETURN

Return to SERVICE FAULT FIND menu.

1 3 DPU

If DPU is selected, the control memory of the DPU CONTROL unit A8 is loaded with a program that is run afterwards. This brings the DPU in a steady cycle, which enables testing of the system.
On a number of output signals of the DPU CONTROL a pulse is generated (see table below). These are all the output signals to the DPU (unit A9) and the trigger address comparator on unit A4, except TRRY and RSDU--LT.
The signals can be found on connector X1402.
The pulse width is 125 ns; the repetition time is 4,5 us.
All signals are at TTL level.

Signal name	Pinnr.	Signal name	Pinnr.
DUABØØ	C20	RDDURM	C26
DUABØ1	C21	SFSRØØ	C12
DUABØ2	A21	SFSRØ1	C11
DUABØ3	C22	STRLF	C15
DUABØ4	A22	ENOFD	A18
DUABØ5	C23	CKF	C25
DUABØ6	A23	CO	C13
DUABØ7	C24	SLAM	A28
DUABØ8	C16	RSDUR-LT	C19
DUABØ9	A17	OTDIAD	C29
DUAB1Ø	C18	OEDUØØ	A29
DUAB11	C17	OEDUØ1	A31
CSDURM	A27	LEDP	C31
CKDUR1	C3	SLOFAD	C27
CKDUR2-LT	A25	CNCPCN	A15
CKDUR3	A26	FBRY	C32

The state of the signals at the testpoints of unit A8 is:

Signal name	State
TRRY	Ø
EC	Ø
DAVA	Ø
ILØ2--LT	1
CKPL	Symmetrical square wave, cycle time = 125 ns.

1 4 --

1 5 DISPLAY SYS TEST

If DISPLAY SYS TEST is selected, the display system continuously displays the softkey text area, which can be seen as an intensified display. Traces, other text areas and miscellaneous text are not displayed. So the display system (units A1, A2, A3 and A4) is brought in a steady cycle, which enables testing of the system. See section 8.1 to 8.4 for the concerning hardware.

NOTE: if there is a failure in the display system, which causes the softkey text area not to be displayed, this test can not be selected in a visisble way. Nevertheless pushing the softkeys in the right sequence selects this test.

1 6 DISPLAY RAM TEST

If DISPLAY RAM TEST is selected, the display ram on unit A4 is tested. This ram consists of the text memory (D2014 and D2016) and the trace memory (D2008, D2009, D2011 and D2012). In the text memory the softkey text and the miscellaneous text is not tested.
If the test is completed succesfully, a message:

DISPLAY RAM test completed succesfully.

is displayed.
If the test fails, all leds on the front panel start blinking and the address where the failure is, is continuously read and written by the microprocessor.

NOTES: - this test destroys the contents of the trace memory, so after the test all traces are lost.
- as with the DISPLAY SYS TEST (see above), this test can be selected by pushing the softkeys in the right sequence, in case of a display failure.

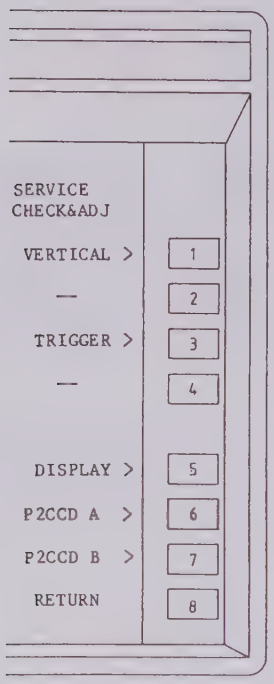
1 7 --

1 8 RETURN

Returns to SERVICE SELECT menu.

2 --

3 CHECK & ADJ>

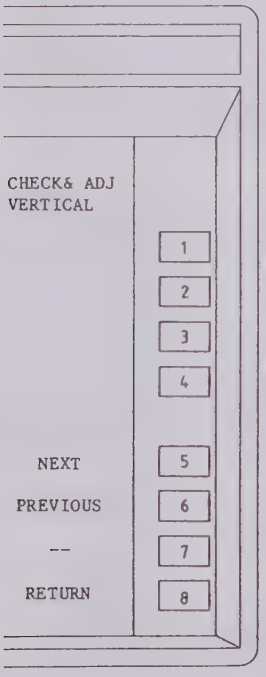


If CHECK & ADJ is selected, the CHECK & ADJ menu is displayed and a number of adjust routines can be selected.

Each routine is only operative if it is displayed.

See section 9.3 for detailed information about the use of the adjust routines.

3 1 VERTICAL>



If VERTICAL is selected, the CHECK & ADJ VERTICAL menu is displayed.
Information about the activated adjust routine for the vertical section of the oscilloscope is given at the left side of the softkeys 1 to 4.
The sequence number of the routine is displayed in the top of the menu behind "VERTICAL".

3 1 5 NEXT

Activates and displays the vertical adjust routine with the next higher sequence number.

3 1 6 PREVIOUS

Activates and displays the vertical adjust routine with the next lower sequence number.

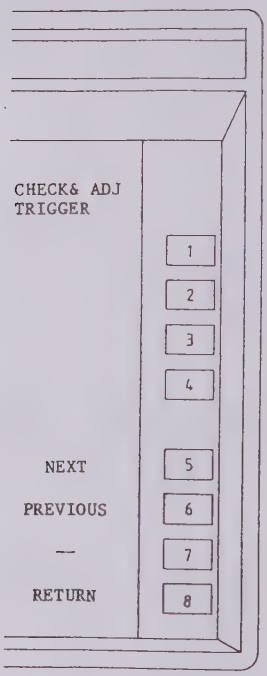
3 1 7 --

3 1 8 RETURN

Return to SERVICE CHECK & ADJ menu.

3 2 --

3 3 TRIGGER>



If TRIGGER is selected, the CHECK & ADJ TRIGGER menu is displayed.
Information about the activated adjust routine for the trigger section of the oscilloscope is given at the left side of the softkeys 1 to 4.
The sequence number of the routine is displayed in the top of the menu behind "TRIGGER".

3 3 5 NEXT

Activates and displays the trigger adjust routine with the next higher sequence number.

3 3 6 PREVIOUS

Activates and displays the trigger adjust routine with the next lower sequence number.

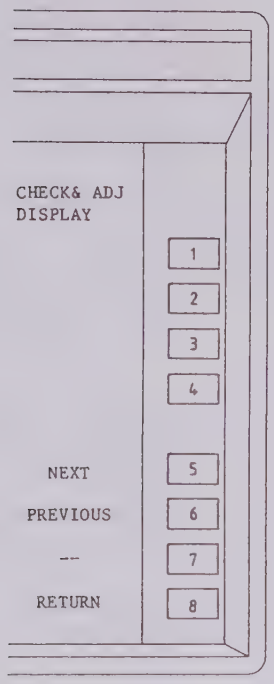
3 3 7 --

3 3 8 RETURN

Return to SERVICE CHECK & ADJ menu.

3 4 --

3 5 DISPLAY>



If DISPLAY is selected, the CHECK & ADJ DISPLAY menu is displayed.
Information about the activated adjust routine for the display section of the oscilloscope is given at the left side of the softkeys 1 to 4.
The sequence number of the routine is displayed in the top of the menu behind "DISPLAY".

Note:

When leaving the DISPLAY Ø menu it may be necessary to keep the key depressed for a short time, before any action takes place.

3 5 5 NEXT

Activates and displays the display adjust routine with the next higher sequence number.

3 5 6 PREVIOUS

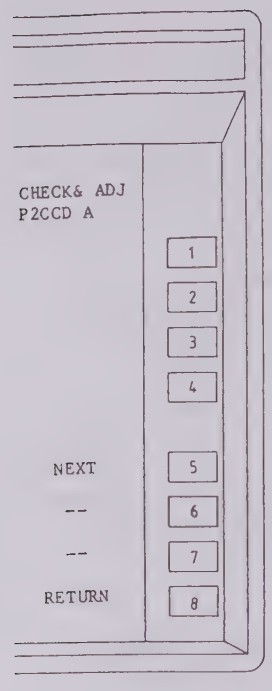
Activates and displays the display adjust routine with the next lower sequence number.

3 5 7 --

3 5 8 RETURN

Return to SERVICE CHECK & ADJ menu.

3 6 P2CCD A>



If P2CCD A is selected, the CHECK & ADJ P2CCD A menu is displayed.
Information about the activated adjust routine for the P^2CCD A section of the oscilloscope is given at the left side of the softkeys 1 to 4.
The sequence number of the routine is displayed in the top of the menu behind "P2CCD A".

3 6 5 NEXT

Activates and displays the P^2CCD A adjust routine with the next higher sequence number.

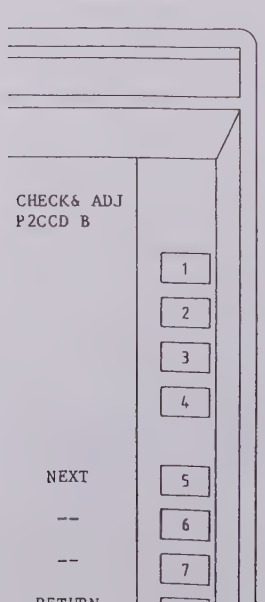
3 6 6 --

3 6 7 --

3 6 8 RETURN

Return to SERVICE CHECK & ADJ menu.

3 7 P2CCD B>



If P2CCD B is selected, the CHECK & ADJ P2CCD B menu is displayed.
Information about the activated adjust routine for the P^2CCD B section of the oscilloscope is given at the left side of the softkeys 1 to 4.
The sequence number of the routine is displayed in the top of the menu behind "P2CCD B".

3 7 5 NEXT

Activates and displays the P^2CCD B adjust routine with the next higher sequence number.

3 7 6 --

3 7 7 --

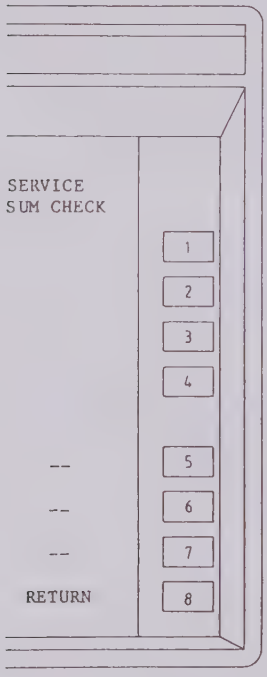
3 7 8 RETURN

Return to SERVICE CHECK & ADJ menu.

3 8 RETURN

Return to SERVICE CHECK & ADJ menu.

4 SUM CHECK>



If SUM CHECK is selected, the SUM CHECK menu is displayed.

At the left side of the softkeys 1 to 4 the sum check data are displayed.

4 5 --

4 6 --

4 7 --

4 8 RETURN

Return to SERVICE menu.

8 RETURN

Return to normal operation.
When a routine is still operative the following message is given:
Changes are executed, but not always correct.
This is done because settings can not be executed if the concerning hardware is controlled by the selected diagnostic.
Therefore this way of returning to normal operation is not recommended.

11.4.4 Hardware selectable diagnostic software

By changing over the service switches on unit A6, a number of service routines can be selected, which are suitable to test the hardware. For some routines not all hardware is needed. So these tests can be used by starting with the minimum required hardware and as long as the routines operate correctly more hardware can be connected until the routines do not operate anymore. The last connected hardware will be broken then.

The table below gives a survey of the tests.

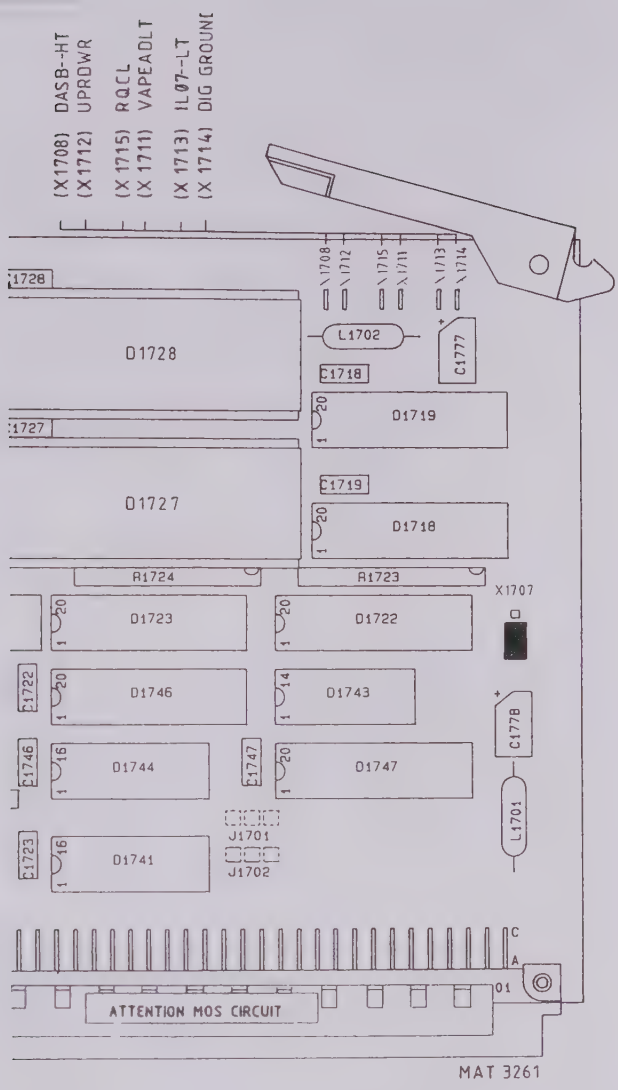
Test	Service switches X1716	X1704	X1706	X1707	Minimum required hardware
Normal operation	fitted	down	down	down	all cards
RAM test	removed	down	up	down	A5 + A6
Front + output ports	removed	up	down	down	A5 + A6 + A8 + frontpanel
Address range	removed	up	up	up	A6

NOTES:
- Figure 11.2 shows the service switches in normal operation position.
- If X1716 is not fitted in normal operation, the oscilloscope may operate normally, but it is possible that it does not start up under certain conditions, because the watchdog circuit is disabled.
- Any options (A7 or A10) should be removed.

The RAM TEST enables testing of the microprocessor ram on unit A5. The test is a cyclic sequence that consists of the following parts:

- All leds on the frontpanel are turned on during 3 seconds.
- All leds are turned off, except the led ALIASED.
- The microprocessor ram is written with a certain pattern in a certain sequence.
- The led REP ONLY is turned on.
- The contents of the microprocessor ram is read back and checked. If the contents is OK, all leds are turned on during 3 seconds, etc. If the contents is wrong, the 3 leds ALIASED, REP ONLY and NOT TRIG´D start blinking with a frequency of about 2 Hz and the address where the failure is, is continuously read and written by the microprocessor.

The FRONTPANEL AND OUTPUT PORTS TEST enables the testing of the frontpanel and the output ports, which can not be tested by the softkey selectable output port test (see section 11.4.3).
When the test is started all leds on the frontpanel start blinking with a frequency of about 2 Hz.
After pushing a pushbutton, the softkeys included, or turning a rotary switch all leds are turned off.
Now the three leds ALIASED, REP ONLY and NOT TRIG´D form the display of a three byte binary counter. The counter counts the opening or closing of every pushbutton switch on the frontpanel as well as the level changes of the outputs of the rotary switches as they are turned. The counter counts always up, independent of the turning direction of the rotary switches.


(X1708) DASB-HT
(X1712) UPROWR
(X 1715) RQCL
(X 1711) VAPEADLT
(X 1713) IL07-LT
(X 1714) DIG GROUNI
\1708
\1712
\1715
\1711
\1713
\1714
1728
D1728
L1702
C1777
C1718
D1719
1727
D1727
C1719
D1718
R1724
R1723
X1707
D1723
D1722
C1722
D1746
D1743
C1778
C1746
D1744
C1747
D1747
L1701
C1723
D1741
J1701
J1702
C
A
01
ATTENTION MOS CIRCUIT
MAT 3261

While the front test is started by pushing a button or turning a rotary switch, the output port test is also started. This test writes an alternating pattern to hardware that is selected by signals with the following names:

Unit	Signal name	IC numbers
A2	WRVEPOLT	D2314 + D2316
A2	WRHOPOLT	D2317 + D2318 + D2332
A3	WRDPSTLT	D2119
A3	WRPSDPLT	D2103 + D2104
A3	WRDPPALT	D2106 + D2107
A3	WRHOVRLT	D2108
A5	--	D1807
A8	SLOT2	D1419
A8	SLOT4	D1421 + D1422

At the outputs of mentioned latches a symmetrical square wave appears with a repetition time of about 270 us.
Furtheron the alternating pattern is written to the following hardware:

Unit	Signal name	IC numbers
A3	Z + Interrupt timer	D2126
A5	Slow time base logic	D1801
A5	Acquisition control logic	D1802
A8	Control memory	D1426 + D1427 + D1428 + D1429

NOTE:
- This test can be done without unit A8 fitted, if a diode link is made between MYSLØ3LT (pin B6) and DATRAKLT (pin C8) on connector X1701. The anode of the diode should be connected to pin C8.

The ADDRESS RANGE TEST writes and reads in sequence the hexadecimal code 5555 to all addresses, followed by the same sequence with hexadecimal code AAAA.
The complete test takes about 74 seconds and is repeated automatically. Each address is read immediately after it is written. The read data are not checked.
During this test all levels of the lines of the microprocessor busses should change regularly.

NOTES:
- Data and address bus lines to other units via the motherboard (unit A12) only change if the address range outside unit A6 is addressed.
- This test can also be run with unit A6 removed from the oscilloscope and supplied by an external 5 Volt power supply.

11.5 RECALIBRATION AFTER REPAIR

After an electrical component has been renewed the calibration of that particular circuit should be checked, as well as the calibration of other closely related circuits.

Since the power supply affects all circuits, calibration of the entire instrument should be checked if work has been done in the power supply or if the transformer has been renewed.

HANDLING OF COMPONENTS AND SOLDERING TECHNIQUES 12

HANDLING OF COMPONENTS AND SOLDERING TECHNIQUES

CONTENTS

12.0 Handling of components and soldering techniques..... 12-1
12.1 Handling of components..... 12-1
12.1.1 Standard parts..... 12-1
12.1.2 Special parts..... 12-1
12.1.3 Transistors and integrated circuits..... 12-1
12.1.4 Static sensitive components..... 12-2
12.2 Handling of MOS devices..... 12-2
12.2.1 Storage and transport..... 12-2
12.2.2 Testing or handling..... 12-2
12.2.3 Mounting..... 12-2
12.2.4 Soldering..... 12-2
12.2.5 Static charges..... 12-3
12.2.6 Transient voltages..... 12-3
12.2.7 Voltage surges..... 12-3
12.3 Soldering techniques..... 12-3
12.3.1 Soldering and desoldering of surface mounted devices..... 12-4

12.0 HANDLING OF COMPONENTS AND SOLDERING TECHNIQUES

12.1 HANDLING OF COMPONENTS

12.1.1 Standard parts

Electrical and mechanical parts replacements can be obtained through your local PHILIPS organisation or representative. However, many of the standard electronic components can be obtained from other local suppliers. Before purchasing or ordering replacement parts, check chapter 15 "PARTS LISTS" for value, tolerance, rating and description.

NOTE: Physical size and shape of a component may affect instruments performance, particularly at high frequencies.
Always use direct replacement components, unless it is known that a substitute will not degrade the instruments performance.

12.1.2 Special parts

In addition to the standard electronic components, some special components are used:

- Components, manufactured or selected by PHILIPS to meet specific performance requirements.
- Components which are important for the safety of the instrument.

ATTENTION: Both type of components may only be replaced by components obtained through your local PHILIPS organisation or representative.

12.1.3 Transistors and integrated circuits

- Return transistors and I.C.'s to their original positions, if removed during routine maintenance.

- Do not renew or switch semi-conductor devices unnecessary, as it may affect the calibration of the instrument.

- Any replacement component should be of the original type or a direct replacement. Bend the leads to fit in the socket or pcb-holes and cut the leads to the same length as on the component being renewed.

- When a device has been renewed, check the operation of the part of the instrument, that may be affected.

- When re-installing power-supply transistors, use silicon grease to increase the heat-transfer capabilities.

WARNING: Handle silicon grease with care. Avoid contact with the eyes. Wash hands thoroughly after use.

12.1.4 Static sensitive components

This instrument contains electrical components (like for example the P^2CCD) that are suspectible to damage from static discharge. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

12.2 HANDLING OF MOS DEVICES

Though all our MOS integrated circuit incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

CAUTION: Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

12.2.1 Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or a special IC carrier that either short-circuits all leads or insulates them from external contact.

12.2.2 Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord to a chain. Connect all testing and handling equipment to the same surface. Signals should not be applied to the input while the device power supply is off. All unused input leads should be connected either to the supply voltage or to ground.

12.2.3 Mounting

Mount MOS integrated circuits on printed circuit boards after all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board, the person mounting the circuit should touch the board before bringing the MOS circuits into contact with it.

12.2.4 Soldering

Soldering iron tips, including those of low voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

12.2.5 Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted, the proper handling precautions should still be observed.
Until the sub-assemblies are inserted into the complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape is put on the circuit board terminals.

12.2.6 Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed circuit boards with MOS devices, from test sockets or systems with power on.

12.2.7 Voltage surges

Beware of voltage surges due to switching electrical equipment ON or OFF, relays and d.c. lines.

12.3 SOLDERING TECHNIQUES

Working method:

- Carefully unsolder one after the other the soldering tags of the semi-conductor.
- Remove all superfluous soldering material. Use a sucking iron or sucking litze wire.
- Check that the tags of the replacement part are clean and pre-tinned on the soldering places.
- Locate the replacement semi-conductor exactly on its place, and solder each tag to the relevant printed conductor on the circuit board.

NOTE: Bear in mind that the maximum permissible soldering time is 10 seconds during which the temperature of the tags must not exceed 250°C. The use of solder with a low melting point is therefore recommended.
Take care not to damage the plastic encapsulation of the semi-conductor (softening point of the plastic is 150°C).

ATTENTION: When you are soldering inside the instrument it is essential to use a low-voltage soldering iron, the tip of which must be earthed to the mass of the oscilloscope.

Suitable soldering irons are:

- ORYX micro-miniature soldering instrument, type 6 A, voltage 6 V, in combination with PLATO pin-point tip type 0-569.
- ERSA miniature soldering iron, type minor 040 B, voltage 6 V.
- Low voltage mini soldering iron, type 800/12 W-6 V, power 12 W, voltage 6 V, order no. 4822 395 10004, in combination with 1 mm pin-point tip, order no. 4822 395 10012.

Ordinary 60/40 solder with core and 35- to 40 W pencil type soldering iron can be used to accomplish the majority of the soldering. If a higher wattage-rating soldering iron is used on the etched circuit boards, excessive heat can cause the etched circuit wiring to separate from the board base material.

12.3.1. Soldering and desoldering of surface mounted devices

Introduction

This description gives you a method for replacing surface mounted devices (S.M.D.'s) and incorporates subjects such as:

- required tools and materials.
- how to arrange the S.M.D.-workshop. (see figure 12.1).
- general hints for S.M.D.-handling.
- interchanging S.M.D.'s with two or three connections.
- interchanging S.M.D.'s with four or more connections.

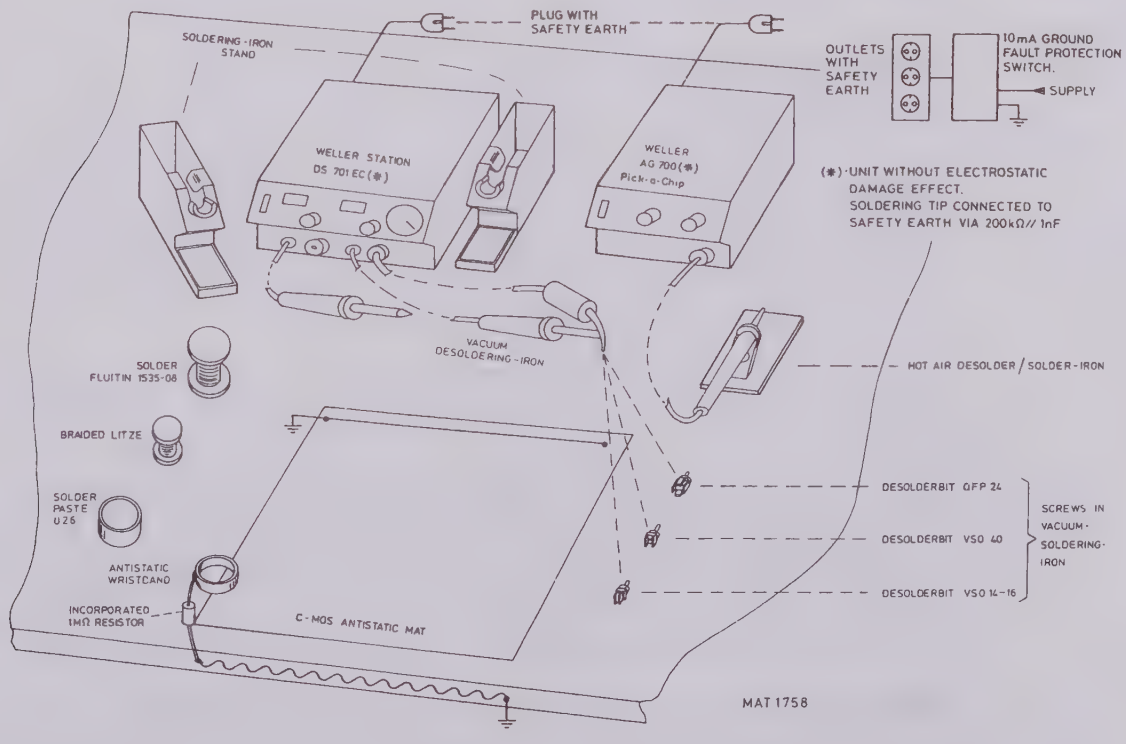


Figure 12.1 Arrangement of working area for S.M.D. exchange.

Required tools and materials

The following tools are necessary:

- A hot-air soldering/desoldering station for components with two or three leads: Weller AG 700 pick-a-chip.
- A vacuum, temperature controlled, soldering/desoldering station for components with four or more connections: Weller DS 701 EC.

- Desoldering accessories that can be attached to the Weller DS 701 EC-equipment: for dual-in-line S.M.D.'s VSO 14 and VSO 16 (with 14 and 16 connections such as used on the HF-attenuator p.c.b.) the types with Weller ordering code 587 13 701 and 587 13 702. For dual-in-line S.M.D.'s VSO 40 (with 40 connections such as used on the LCD-unit) the type with Weller ordering code 587 13 703. For QFP 24 S.M.D.'s (such as used on the time base chip unit) the type with Weller ordering code 587 13 704.
- A working area that has been secured against electro static discharge (E.S.D.).
- A pair of tweezers.

NOTE: The Weller equipment can be ordered via your local Weller-dealer.

The following material is necessary:

- "Fluittin" solder diameter of 0,8 mm, 15/35, Sn Pb 60.
- Solder paste 026.
- Components. Since not all the components are marked, they must be kept in their original packing in order to avoid interchanging them.
- Desoldering braided wire.

General hints for S.M.D.-mounting.

- Protection against E.S.D.: since the working area must be suitable for repair of MOS-devices, some precautions must be taken (see figure 12.1)
  All repairs must be done earthened which means that the repair surface, the soldering iron and the technician must be connected to the earth potential. This is achieved by using a C-MOS antistatic mat that must be connected to earth. The service-technician is connected to earth by wearing an antistatic wristband.
- Components: desoldered components cannot be used again since desoldering is done at a temperature of 350 degrees Celcius while they can only whitstand 240 degrees Celcius for max. 10 sec.
  Keep the new components as long as possible in their original packing in order to avoid damage and mixing up new and old S.M.D.'s.
- For an optimal supply of heat a working area must be used that does not lead away the heat: the antistatic mat in figure 12.1 meets this requirement.

Interchanging S.M.D.'s with two or three connections.

IMPORTANT: Before removing the component, observe very carefully its position in order to aviod that the new component is installed upside-down. This is especially important for capacitors where the metallisation at both ends is longer at the p.c.b. side than at the top side.

Use the equipment Weller AG 700 pick-a-chip and proceed as follows:

- Heat the component up equably with hot air of 350 degrees Celcius.
- Remove the component with a pair of tweezers.
- Clean the p.c.b. tracks, on which the new component has to be soldered, with braided wire or with the use of the vacuum desoldering equipment DS 701 EC.
- Put solder paste on the connections of the new component and position it on the p.c.b..
- Solder the component on to the p.c.b. with the solder described in the materials list. Soldering temperature must be 240 degrees Celsius, soldering time must not exceed 3 sec. per connection. The tip of your soldering iron must not touch the component, but must touch the p.c.b. track close to the component.

Interchanging S.M.D. s with four or more connections.

Use the equipment Weller DS 701 EC and attach a suitable desoldering piece (VSO 14, VSO 16, VSO 40 or OFP 24). Then proceed as follows:

- Adjust the desoldering temperature to 350 degrees Celcius and place the desoldering piece on the IC that has to be removed. Take care that all connections of the IC are equally heated up).
- Switch the vacuum on and lift the component from the p.c.b.
- Clean the p.c.b. tracks, on which the new component has to be soldered, with braided wire or with the use of the vacuum desoldering equipment DS 701 EC.
- Put solder paste on the connections of the new component and position it on the p.c.b.
- Position the component by soldering first the outside connections in a crosswise manner. Soldering temperature must be 240 degrees Celcius. Keep the soldering time as short as possible.
- Solder now the other connections.
- If necessary you must remove superfluous rests of solder with the use of braided wire.

SERVICE TOOLS 13

CONTENTS

13.0 Service tools..... 13-1
13.1 Recommended test and calibration equipment..... 13-1
13.2 Dummy load for power supply..... 13-3
13.3 Special tools..... 13-5
13.3.1 Special tool for removing small rotary knobs 13-5
13.3.2 Special tool for removing the S.M.D. modules from the p.c.b.'s 13-5
13.3.3 Extension board for the units A1 ... A11 and A20..... 13-5
13.3.4 Special tool for renewing integrated circuits (DIL package)... 13-5

13.0 SERVICE TOOLS

13.1 RECOMMENDED TEST AND CALIBRATION EQUIPMENT

Type of instrument	Specification	Used for	Example of required instruments
1. Constant amplitude sine-wave generator.	Freq. 50 kHz.. >300 MHz Voltage 10 mV.. 5 V	Bandwidth check of vertical channels and triggering	Tektronix SG503 + SG504
2. Time marker generator	Repetition rate 5 s ... 5 ns	Checking and adjusting of time base sweep rates including MAGN X10.	Tektronix TG501.
3. Square-wave calibration generator	Rise-time faster then 1 ns Voltage 10 mV up to (for prerefe-rence) 30 V Duty cycle 50%	Checking and adjusting of square-wave response of vertical channels and triggering	Generator with additional attenuators partly PG506.
4. LF sine-wave /sq.-wave generator	Sine-wave Freq.: 1 Hz... 1 MHz Voltage: 0... 30 V	Checking the LF trigger sensitivity	Philips PM5131
	Square-wave Freq.: 1 Hz... 1 MHz Voltage: 0... 30 V Rise time: faster then 100 ns	Checking and adjusting sq.-wave response of for instance attenuator unit	
5. Cables, T-piece, terminations and 10:1 attenuator	BNC-type		
6. Dummy probe 2:1	1 MOhm ±0,1%//14 pF	Check of input capacitance	

Type of instrument	Specification	Used for	Example of required instruments
7. Trimming tool kit	--	Adjustments	Philips SBC317 (ord. number 4822 310 50095)
8. Variable mains transformer.	Well-insulated Output voltage 90...264 VAC	Checking influence of mains voltage variations and adjustment of power supply.	Philips ord. number 2422 529 00005
9. Oscilloscope	The bandwidth must be the same or higher than the bandwidth of the instrument under test.	Checking and adjusting the instrument under test	Philips PM3295
10. Digital multimeter	Wide voltage, current and resistance ranges. Required accuracy 0,1%	Checking and adjusting the instrument under test	Philips PM2718
11. BNC probe tip adapter	--	Checking bandwidth of the oscilloscope via probe.	Philips 5322 263 50022
12. BNC banana adapter	--	Checking the variable gain balance.	Philips PM 9051
13. Stabilized power supply	0-12 V d.c./ 1 mA	Checking the penlift signal of the plot output.	Philips PE 1535
14. Plot out cable DIN/ 6x banana	--	Checking and adjusting of the plot output.	Philips 5322 321 20908
15. Constant sine-wave generator	245...1050 MHz	Checking the trigger sensitivity at 300 MHz.	Tektronix SG 504

13.2 DUMMY LOAD FOR POWER SUPPLY (unit A20)

Information for an easy access to the power supply and for safe working conditions can be found in chapter 10 "DISASSEMBLING AND ASSEMBLING". This chapter also explains how to measure the power supplies in working condition.
The position of the rear side panel of the oscilloscope under test is also indicated in chapter 10.

In order to be able to determine whether a certain fault condition is initiated by the power supply itself or by the connected oscilloscope circuits, a dummy load is listed in the table below. The table gives also an example of the resistor types that can be used to compose the dummy load: the resistors can be ordered at Concern Service.

The dummy load resistors must be mounted on a p.c.b. and connected via a (flat)cable to X4604 on unit A20 (mounted on rear side panel).
The connector pins are also given in the diagram of chapter 8.20.
Electrolytic capacitors in the dummy load are not necessary because of the capacitive values present on the power supply unit itself.

Supply Voltage	Connector pin(s) X4604 (A20)	Output Current	Power dissi-pation	Dummy load
+5 V (+5 D)	30A-30C-31A-31C-32A-32C	5 A	25W	10 resistors of 10 Ohm, 4 W in parallel: 4822 112 21054
-5 V (-5 D)	13A-13C-14A-14C-15A-15C	2,2 A	11 W	4 resistors of 10 Ohm, 4 W: 4822 112 21054 and 1 resistor of 39 Ohm, 4 W: 4822 112 21069 in parallel
+7 V	16A-16C	550 mA	3,9 W	2 resistors of 27 Ohm, 4 W: 4822 112 21065 in parallel
-7 V	17A-17C	1,2A	8,4 W	2 resistors of 12 Ohm, 7 W: 4822 112 41056 in parallel
+14 V	20A-20C-21A-21C	1,2A	16,8 W	2 resistors of 27 Ohm, 11 W: 4822 112 31065 and 1 resistor of 100 Ohm 4 W: 4822 112 21081 in parallel
-14 V	18A-18C-19A-19C	1A	14 W	2 resistors of 8,2 Ohm, 4 W: 4822 112 21052 in parallel, with 1 resistor of 10 Ohm 11 W: 4822 112 31054 in series
+19 V	23A-23C	150 mA	2,9 W	1 resistor of 100 Ohm, 4 W: 4822 112 21081 in series with 27 Ohm , 4 W: 4822 112 21065
-19 V	22A-22C	250 mA	4,8 W	2 resistors of 150 Ohm, 4 W: 4822 112 21085 in parallel
+40 V	24A-24C	120 mA	4,8 W	1 resistor of 330 Ohm, 7 W: 4822 112 41094
+100 V	12 A	20 mA	2 W	1 resistor of 4,7 kOhm, 4 W: 4822 112 21125
ϟ 6,3 V a.c filament C.R.T.	X4602 pins 3 and 1	250 mA	1,6 W	lamp 6,3 V 250 mA: 4822 134 40007

13.3 SPECIAL TOOLS

13.3.1 Special tool for the slotted nuts on the front panel.

A special tool is available for the slotted nuts on the front panel, code number 5322 395 54024.
For those who want to make such a tool, a sketch is given below with the dimensions in mm.
The material is silversteel NO94, tempered 40-45RC.

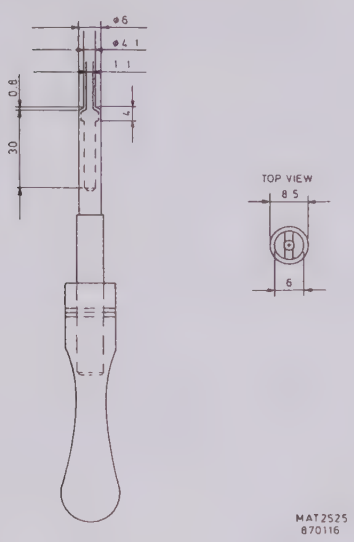


Figure 13.1 Dimensional drawing of tool for slotted nut.

13.3.2 Special tool for removing the S.M.D. modules from the p.c.b.´s

To remove the S.M.D. modules from the vertical signal unit A32, CCD logic A26 and from the clock unit A34, a special cutnipper must be used for instance:

Lindström - Eskilstuna - Sweden type 3511 or
Erem - Geneve - type 504AE/110 (oblique cutnipper).
Service ordering number: 5322 395 90564

13.3.3 Extension board for the units A1 ... A11 and A20

For test and repair purposes the unit A1 ... A11 or A20 can be plugged in their connectors via an extension board available under codenumber 5322 216 51153
The position of the rear side panel with unit A20 connected to the management unit A25 via the above mentioned extension card is indicated in chapter 10.

13.3.4 Special tool for removing integrated circuits (DIL package)

For cutting the connection pins of integrated circuits a special cutnipper is available under ordering number 5322 395 71004

SAFETY INSPECTION AND TESTS AFTER REPAIR AND MAINTENANCE 14

SAFETY INSPECTION AND TESTS AFTER REPAIR AND MAINTENANCE

CONTENTS

14.0 Safety inspection and tests after repair and maintenance in the primary circuit..... 14-1
14.1 Safety inspection and tests..... 14-1
14.1.1 General directives..... 14-1
14.1.2 Safety components..... 14-1
14.1.3 Checking the protective earth connection..... 14-1
14.1.4 Checking the insulation resistance..... 14-1
14.1.5 Checking the leakage current..... 14-1
14.1.6 Voltage test..... 14-2
14.2 Instrument replacing..... 14-2

14.0 SAFETY INSPECTION AND TESTS AFTER REPAIR AND MAINTENANCE IN THE PRIMARY CIRCUIT

14.1 SAFETY INSPECTION AND TESTS

14.1.1 General directives

- Take care that the creepage distances and clearances have not been reduced.
- Before soldering, the wires should be bent through the holes of solder tags, or wrapped around the tag in the form of an open U, or, wiring ridigity shall be maintained by cable clamps or cable lacing.
- Replace all insulating guards and -plates.

14.1.2 Safety components

Components in the primary circuit may only be renewed by components selected by PHILIPS, see also clause 12.1.2.

14.1.3 Checking the protective earth connection

The correct connection and condition is checked by visual control and by measuring the resistance between the protective lead connection at the plug and the cabinet/frame. The resistance shall not be more than 0,1 Ohm. During measurement the mains cable should be removed from the mains. Resistance variations indicate a defect.

14.1.4 Checking the insulation resistance

Measure the insulation resistance at U = 500V dc between the mains connections and the protective lead connections. For this purpose set the mains switch to ON. The insulation resistance shall not be less than 2 MOhm.

NOTE: 2 MOhm is a minimum requirement at 40°C and 95% Relative Humidity. Under normal conditions the insulation resistance should be much higher (10 ... 20 MOhm).

14.1.5 Checking the leakage current

The leakage current shall be measured between each pole of the mains supply in turn, and all accessible conductive parts connected together (including the measuring earth terminal).
The leakage current is not excessive if the measured currents from the mentioned parts does not exceed 0,5 mA rms.

14.1.6 Voltage test

The instrument shall withstand, without electrical breakdown, the application of a test voltage between the supply circuit and accessible conductive parts that are likely to become energized. The test potential shall be 1500 V rms at supply-circuit frequency, applied for one second.
The test shall be conducted when the instrument is fully assembled, and with the primary switch in the ON position.
During the test, both sides of the primary circuit of the instrument are connected together and to one terminal of the voltage test equipment; the other voltage test equipment terminal is to be connected to the accessible conductive parts.

14.2 INSTRUMENT REPACKING

If the instrument is to be shipped to a Service Centre for service or repair, attach a tag showing the full addres and the name of the individual at the users firm that can be contacted. The Service Centre needs the complete instrument, its serial number and a fault description. If the original packing is not available, repack the instrument in such a way that no damage occurs during transport.

PARTS LISTS

CONTENTS

15.0 Parts lists..... 15-1
15.1 Mechanical parts..... 15-1
15.1.1 Mechanical + electrical parts front side..... 15-1
15.1.2 Mechanical + electrical parts rear side..... 15-4
15.1.3 Carrying handle and housing..... 15-6
15.1.4 Internal mechanical parts for front unit..... 15-8
15.1.5 C.R.T. fixing materials..... 15-9
15.1.6 Miscellaneous parts..... 15-10
15.2 Electrical units..... 15-11
15.3 Cables and connectors..... 15-13
15.3.1 Flat cables and connectors..... 15-13
15.3.2 Coax cables..... 15-13
15.3.3 Miscellaneous cables and connectors..... 15-14
15.3.4 Coax connector socket..... 15-14
15.4 Mains cords..... 15-14
15.5 Tools..... 15-14
15.6 Electrical parts..... 15-15

15.0 PARTS LISTS

SUBJECT TO ALTERATION WITHOUT NOTICE

In this chapter the mechanical and electrical parts are listed.

The item numbers of the parts are indicated in the figures of this chapter.

The opening of parts, or removal of covers, is likely to expose live conductors. The instrument should therefore be disconnected from all voltage sources before any opening of parts or removal of covers is started.
During and after dismantling, bear in mind that capacitors in the instrument may still be charged even if the instrument has been separated from all voltage sources.

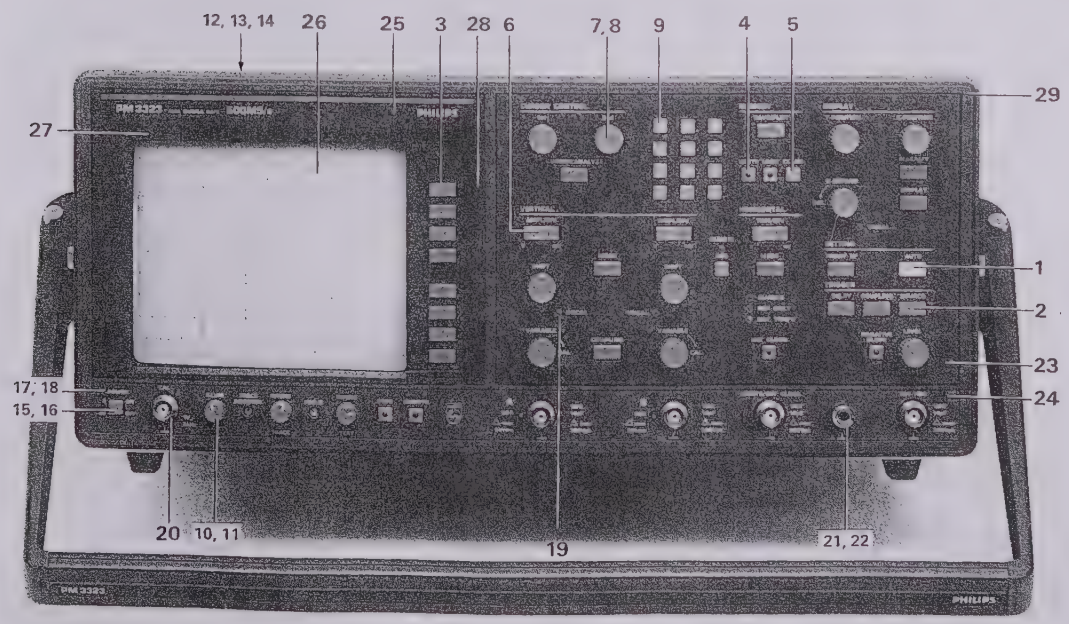
15.1 MECHANICAL PARTS

15.1.1 Mechanical + electrical parts front side (figure 15.1)

Item	Qty/. instr.	Description	Ordering number
1	1	Green pushbutton cover for: S4229 AUTO SET	5322 414 20186
2	11	Brown pushbutton cover (12,5 x 6,5) for: S4224 CURSOR/ANALYZE S4221 VERTICAL MODE S4219 VERTICAL COUPLING S4217 SAVE/PLOT S4222 HORIZONTAL MODE S4216 MAGNIFY S4218 DISPLAY S4226 FRONT NO S4228 TRIGGER DELAY S4223 TRIGGER COUPLING S4227 TRIGGER SOURCE	5322 414 60037
3	8	Brown pushbutton cover (12,5 x 6,5) for: S4 SOFTKEY 1 S5 SOFTKEY 2 S6 SOFTKEY 3 S7 SOFTKEY 4 S8 SOFTKEY 5 S9 SOFTKEY 6 S10 SOFTKEY 7 S11 SOFTKEY 8	5322 414 20185

Item	Qty/. instr.	Description	Ordering number
4	4	Brown pushbutton cover assembly (6,5 x 6,5) with led window for: S4233 WRITE S4234 LOCK S4231 EXT CLOCK S4237 NEG SLOPE S2 DOTS S3 SMOOTH	5322 414 60038
5	2	Brown pushbutton cover and switch (6,5 x 6,5) for: S4236 CLEAR S4232 URQ	5322 276 11856
6	3	Brown UP/DOWN-control cover (18 x 6,5) and switch for: S4238 A AMP/DIV S4239 B AMP/DIV S4241 TIME/DIV	5322 277 10878
7	10	Brown knob dia 14 mm for rotary controls: CURSOR 1st CURSOR 2nd SHIFT A SHIFT B VARIABLE A VARIABLE B Y-POSITION X-POSITION X-EXPAND LEVEL	5322 414 30062
8	10	Brown cover for 14 mm knob for rotary controls:	5322 414 70015
9	1	Key unit (12 keys with numbered covers)	5322 218 41032
10	3	Brown knob dia 10 mm for: R1 ILLUM R3 INTENS TRACE R5 INTENS TEXT	5322 414 30044
11	3	Brown cover with white marking line: R1 - R3 and R5	5322 414 70016
12	2	Illumination lamp E1 and E2 (28 V - 80 mA)	5322 134 40534
13	1	Illumination lampholder	5322 255 24015
14	1	Light cover for illumination lampholders	5322 380 10021
15	1	POWER ON knob	5322 414 60142
16	1	Spring for POWER ON knob	5322 492 41354
17	1	POWER ON ledholder	5322 255 40231
18	1	POWER ON led CQW54-VI H1	5322 130 32704

19	7	Led TLHR 4613 for: UNCAL A H4204 UNCAL B H4206 REMOTE H4207 ALIASED H4201 REP ONLY H4202 NOT TRIG´D H4203 UNCAL X-EXPAND H4208	4822 130 31128
20	5	BNC socket for: X1 CAL X2 A X3 B X4 EVENTS/EXT CLOCK X6 EXT TRIG	5322 267 10191
21	1	Knurled nut for earth connector X5	5322 505 14178
22	1	Thread end for earth connector X5	5322 535 84446
23	1	Front text plate (with adhesive backside)	5322 455 11009
24	1	Textplate under C.R.T. (with adhesive backside)	5322 455 11008
25	1	Textstrip above C.R.T. (with adhesive backside)	5322 455 81087
26	1	Blue contrast filter	5322 381 10963
27	1	Bezel (window for contrast filter)	5322 450 60977
28	2	Spring for bezel	5322 492 70273
29	1	Plastic front frame	5322 447 91377
-	1	Front cover (without inner plate)	5322 447 91378
-	1	Inner plate of front cover	5322 447 91376



15.1.2 Mechanical + electrical parts rear side (figure 15.2 and 15.3)

Item	Qty/. instr.	Description	Ordering number
1	4	Distance piece for rear foot	5322 462 50385
2	2	Rear foot (without rubber feet)	5322 462 41135
3	4	Rubber foot for rear foot	5322 462 40765
4	4	Screw for rear foot	5322 502 12882
5	4	Distance peace for rear foot	5322 532 24591
6	4	Washer	5322 532 14593
7	4	Spring washer	4822 530 80163
8	1	Cover for battery holder	5322 462 40766
9	2	Battery holder	5322 256 64014
10	1	Rear plate	5322 447 91698
11	1	PLOT output socket X17	4822 267 40039
12	1	Power inlet X19 (Fuse holder + mains input socket)	5322 219 81131
13	1	Fuse 2,5 A TZ F1	4822 253 30026
14	1	Fan M1	5322 361 10453
15	1	Fan protection grid	5322 466 30269
16	2	Rear profile (without strip and grounding spiral)	5322 466 61845
17	70cm	HF grounding spiral for rear profile	5322 492 70274

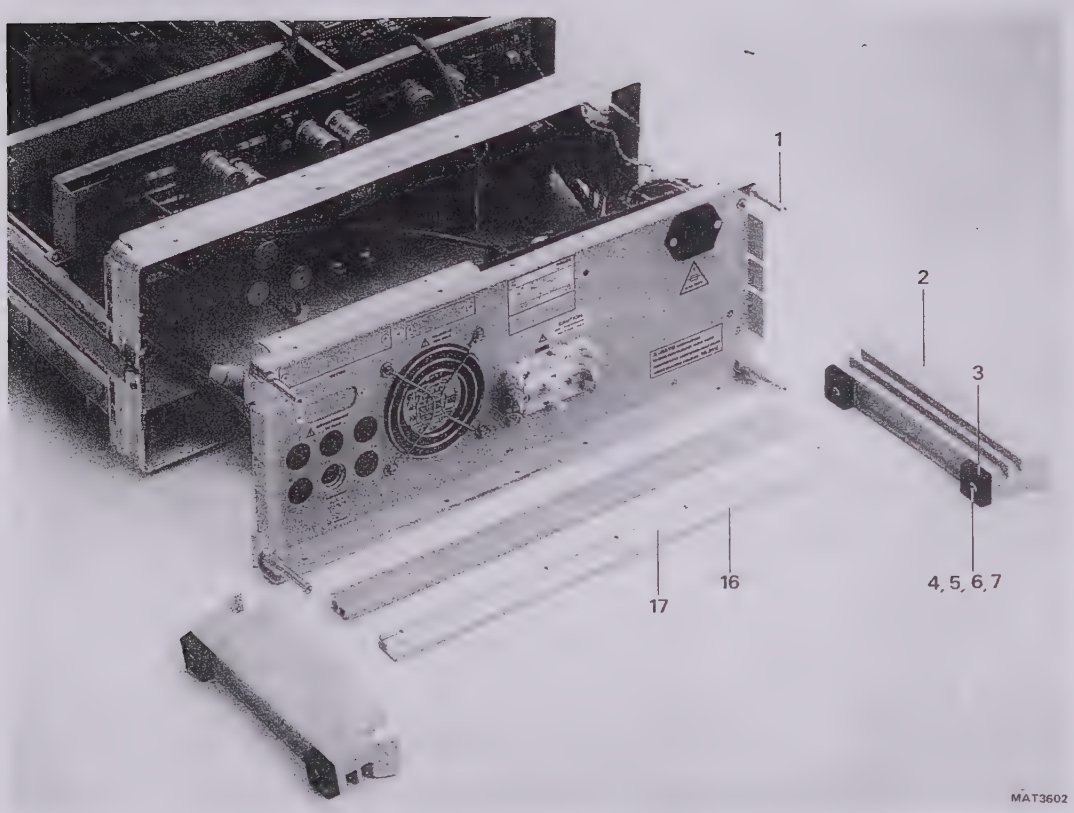
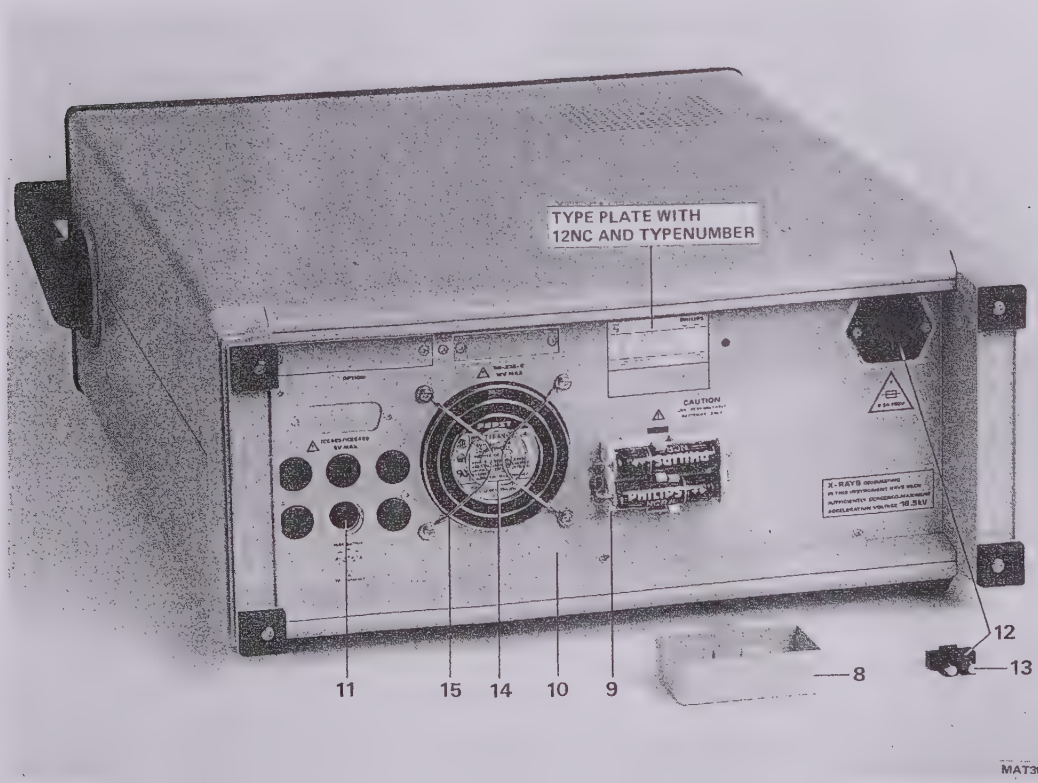


Figure 15.2 Mechanical parts rear side.



15.1.3 Carrying handle and housing (figure 15.4 and 15.5)

Carrying handle

Item	Qty/. instr.	Description	Ordering number
1	2	Locking pin	5322 535 74401
2	2	Spring	5322 492 54155
3	1	Handle arm left	5322 498 50225
4	1	Handle arm right	5322 498 50226
5	1	Metal carrying profile	5322 466 61554
6	1	Plastic carrying profile cover	5322 466 61555
7	1	Textstrip	5322 455 81088
8	4	Screw	4822 502 10064

Housing

Item	Qty/. instr.	Description	Ordering number
9	2	Beige side profile (left or right)	5322 466 61553
10	2	Beige handle ring	5322 498 50242
11	1	Top cover	5322 447 91697
12	4	Cap for pouch holes	5322 462 71476
13	1	Bottom cover	5322 447 91375
14	4	Foot (bottom side)	5322 462 50325

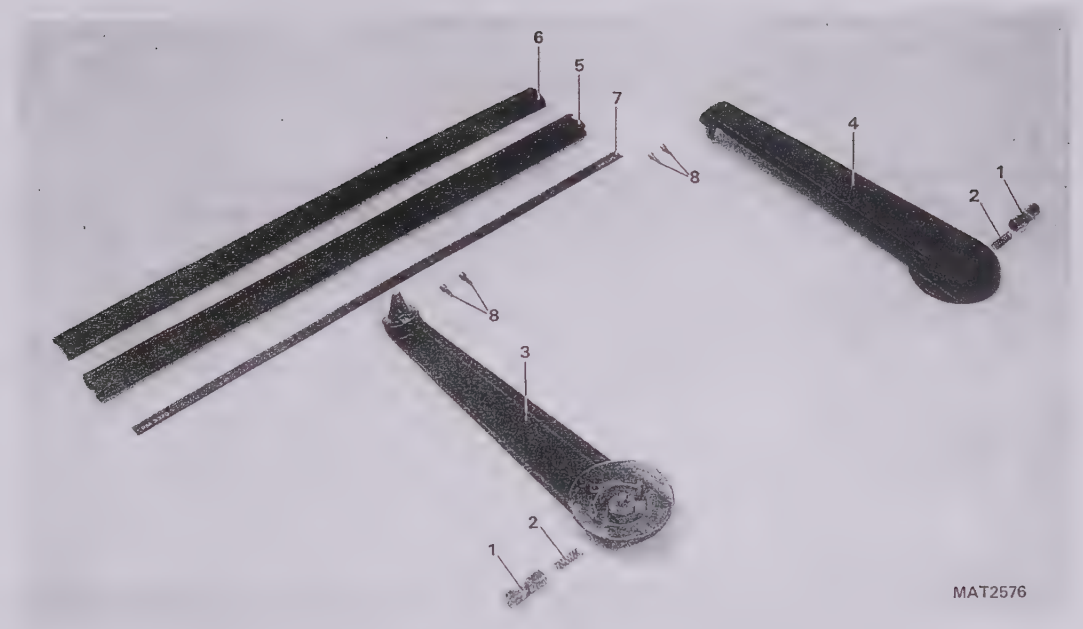


Figure 15.4 Carrying handle.

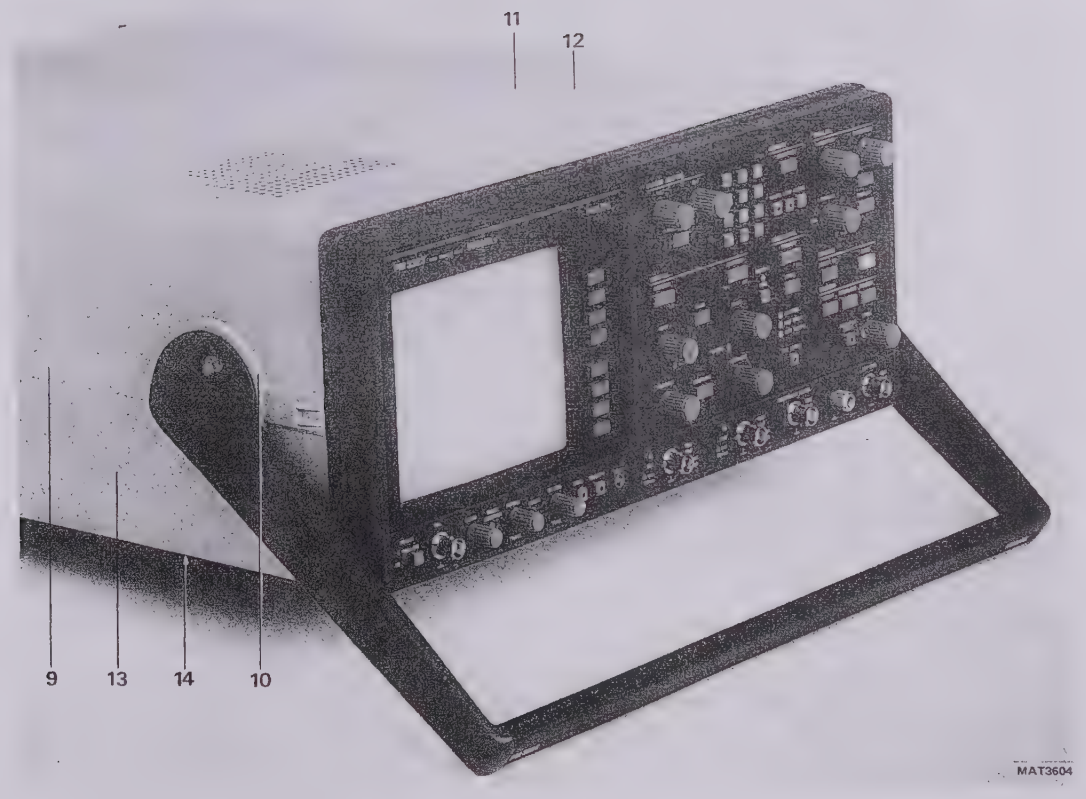


Figure 15.5 Housing.

15.1.4 Internal mechanical parts for front unit (figure 15.6)

Item	Qty/. instr.	Description	Ordering number
1	10	Prism for rotary shaft encoder	5322 256 91198
2	10	Lock for rotary shaft encoder	5322 532 51869
3	10	Rotary shaft encoder	5322 535 91823
4	10	Fixture for leds and fototransistors	5322 256 91199
5	5	Slotted nut for textplate	5322 505 14186
6	4	Spacer	5322 535 92926
7	6	Distance piece M3 x 20	5322 535 91905

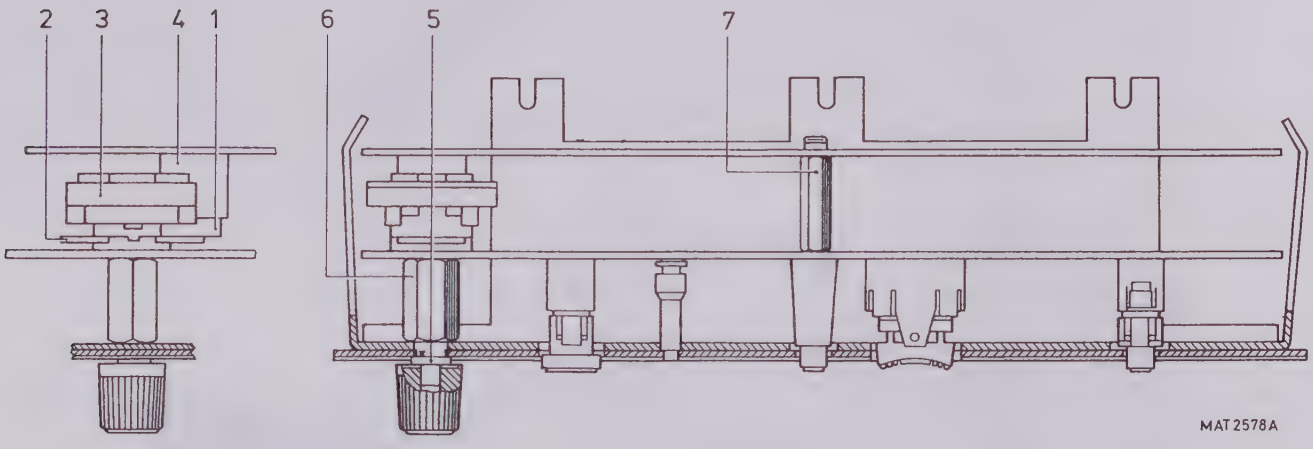


Figure 15.6 Mechanical parts front unit.

15.1.5 C.R.T. fixing materials (figure 15.7)

Item	Qty/. instr.	Description	Ordering number
1	1	C.R.T. socket X1504	5322 255 40502
2	1	Earthing spring for C.R.T. shielding	5322 492 63718
3	6	Gummi parts in C.R.T. shielding	5322 466 61556
4	1	Plastic/rubber pressure support for C.R.T.	5322 462 41136
5	3	Gummi parts around C.R.T. front	5322 532 11588
6	1	Plastic clamping fork for front side of C.R.T.	5322 401 11112
7	1	Metal wedge for front side of C.R.T.	5322 535 20072
8	1	Metal clamping piece for front side of C.R.T.	5322 535 20071

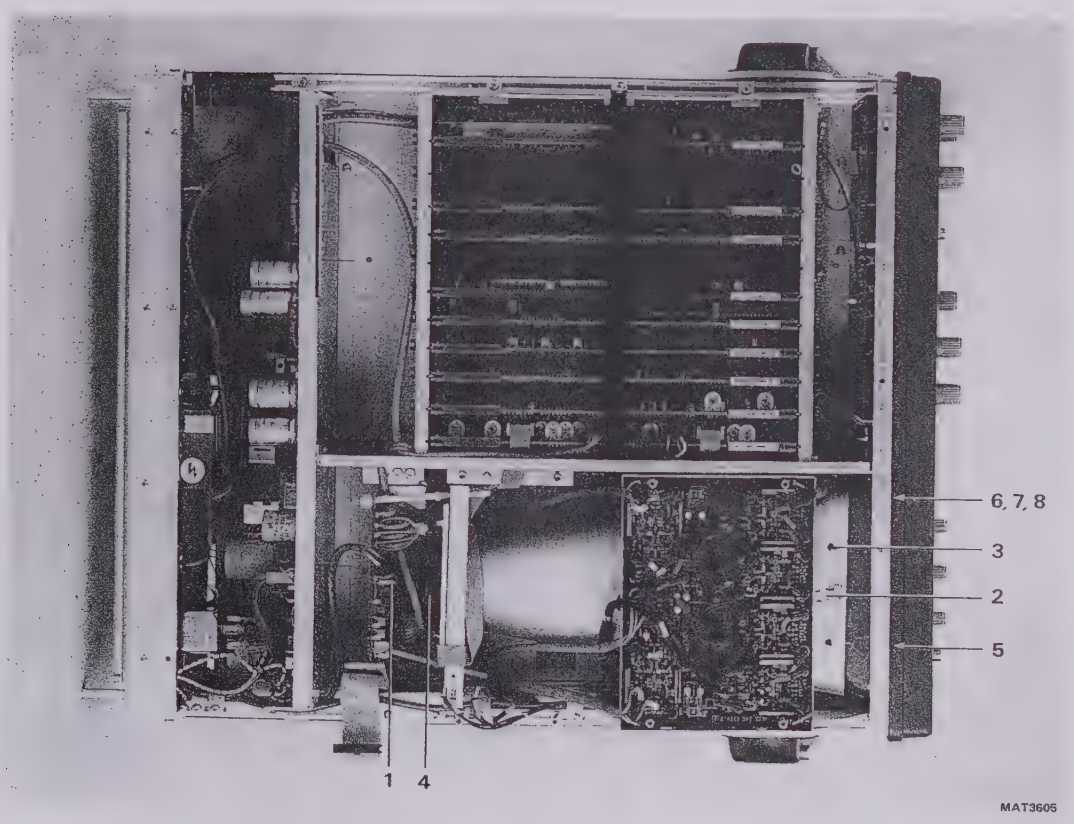


Figure 15.7 C.R.T. fixing materials.

15.1.6 Miscellaneous parts (figure 15.8)

Item	Qty/. instr.	Description	Ordering number
1	1	C.R.T. D18-190GH/129 V1	5322 131 20205
2	22	Plastic conductor for units A1..A11	5322 401 11109
3	18	Red p.c.b. handle	5322 401 11108
4	18	Pin for red p.c.b. handle	5322 402 10036
5	1	Bracket over plug-in units	5322 401 11113
6	3	Ball cord for unit A15	5322 401 11114
7	5	Spring for heatsink on unit A19 for transistors: V4447 - V4448 - V4429 - V4424 - V4426	5322 492 63721
8	1	Bracket for high voltage unit D4601	5322 401 11111
9	1	Power on switch S1	5322 276 11859
-	110	Coding pin for DIN connectors	5322 268 10254

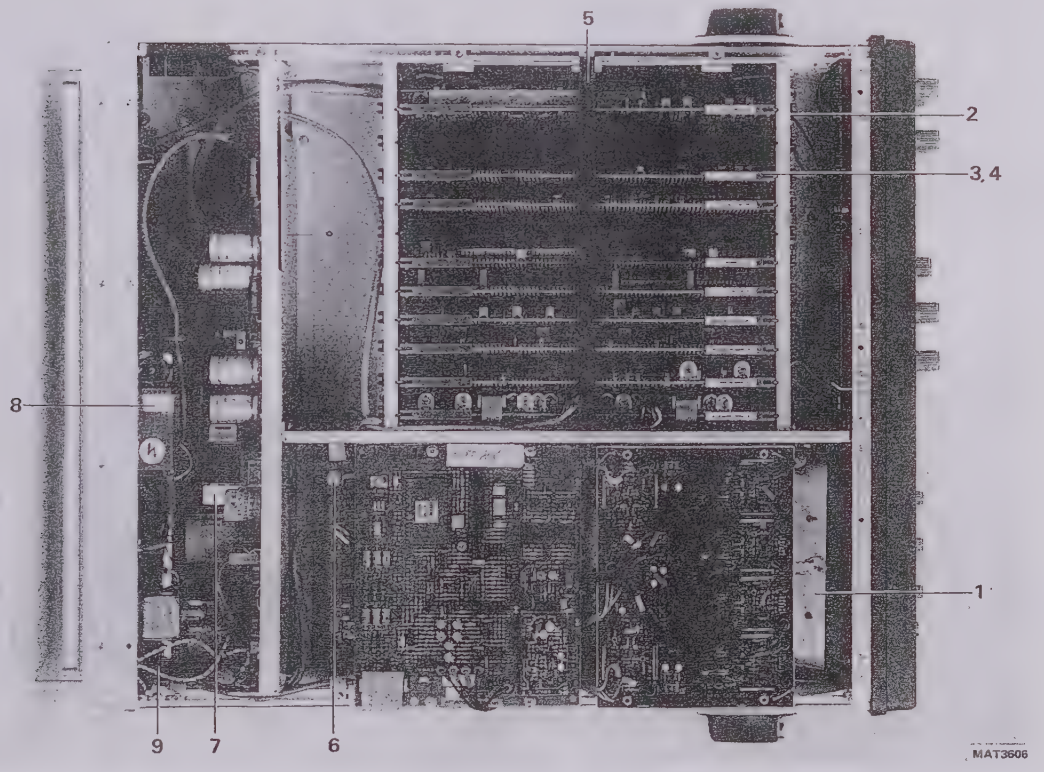


Figure 15.8 Miscellaneous parts.

15.2 ELECTRICAL UNITS (Figures 15.9 and 15.10)

Item	Description	Ordering number
A1	Final amplifier unit	5322 216 51154
A2	Display dac unit	5322 216 51155
A3	Display control unit	5322 216 51156
A4	Display memory unit	5322 216 51157
A5	MRAM unit	5322 214 90188
A6	UPROC unit	5322 214 90187
A8	DPU control unit	5322 216 51161
A9	DPU unit	5322 216 51162
A11	ADC + T&H unit	5322 216 51163
A13	FRONT 1 unit	5322 216 51176
A14	FRONT 2 unit	5322 216 51178
A15	Z-amplifier unit	5322 216 51164
A16	C.R.T. control unit (inclusive unit A18 SMOOTH + DOTS unit)	5322 216 51179
A17	Softkey unit	5322 218 41031
A19	POWER 1 unit	5322 216 51182
A20	POWER 2 unit	5322 216 51183
A24	DRIVER unit	5322 216 51234
A26	CCD logic unit	5322 216 51235
A27	HF attenuator unit	5322 216 51081
A28	LF attenuator unit	5322 216 51184
A29	HF attenuator unit	5322 216 51081
A30	LF attenuator unit	5322 216 51184
A31	External trigger unit	5322 216 51185
A33	P^2CCD unit	5322 216 51236
A34	Clock unit	5322 216 51237
A38	Mini trigger select unit	5322 216 51166
A39	Mini trigger select unit	5322 216 51166
A40	Mini trigger filter unit	5322 216 51167
A41	Mini trigger amplifier unit	5322 216 51168
A42	Mini trigger logic unit	5322 216 51169
A43	Mini events/amplifier unit	5322 216 51171
A44	Mini vertical amplifier proc.	5322 216 51172
A48	Mini frequency doubler	5322 216 51238
A49	Mini CCD logic unit	5322 216 51175
A51	Attenuator relais unit	5322 216 51187
A65	Attenuator unit complete	5322 693 11073
-	Extension board	5322 216 51153
-	EHT unit	5322 216 51177
-	Set of software	5322 310 10309

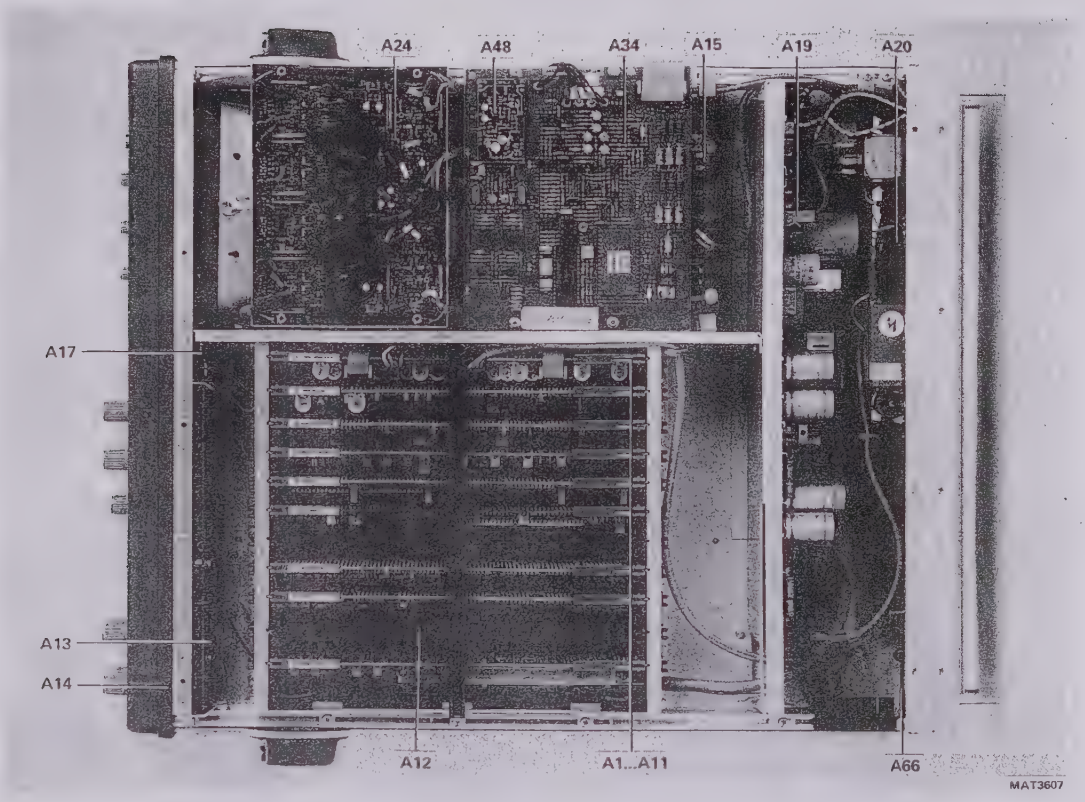
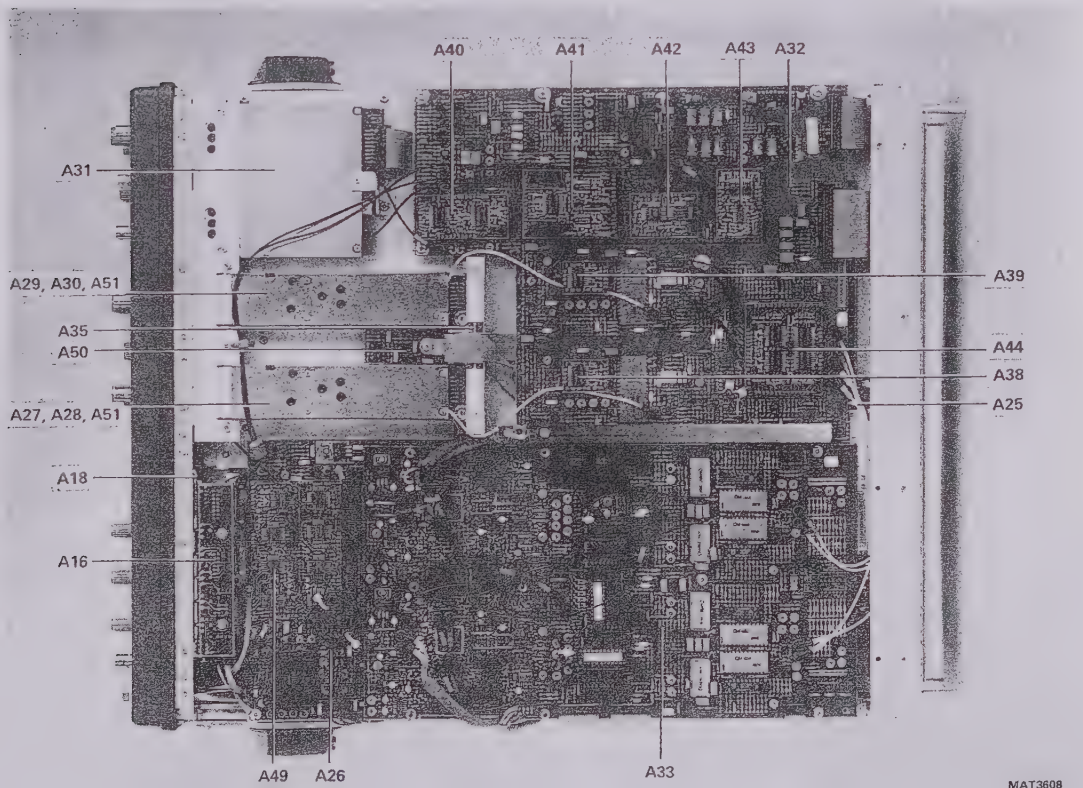


Figure 15.9 Position of electrical units.



15.3 CABLES AND CONNECTORS

15.3.1 Flatcables and connectors

The following flatcables are available:	Ordering number
50 Pole flatcable from X4403 on unit A19 to X4606 on unit A20	5322 321 23424
64 Pole flatcable from X501 on unit A12 to X2502 on unit A25	5322 321 23427

The remaining flatcables used in this oscilloscope must be made by yourself with the following parts:

- Universal flatcable, 40 wires, length 60 cm	5322 323 50112

To get the required number of wires the flat cable must be split by means of a pair of scissors or a knife.
The cable must be cut on the required length.

- Flatcable connectors

The connectors can be mounted on the flatcable by means of a pair of pliers or in a bench-vice.

Attention: check the position of the flatcable in the connector before pressing the connector together.

The following connectors are available:	Ordering number
10 pole cable connector	5322 265 51117
20 pole cable connector	5322 265 54059
24 pole cable connector	5322 265 51114
26 pole cable connector	5322 267 60164
34 pole cable connector	5322 267 70163
40 pole cable connector	5322 267 70162
Nylon clamps to lock connectors (36 per instr.)	5322 401 11156

15.3.2 Coax cables

The following coax cable sets are available:	Ordering number
Cable set 75 ohm (2 cables per set) between unit A24 and A33	5322 321 23429
Cable set 50 ohm (4 cables per set) between unit A24 and A33	5322 321 23428

The remaining 50 ohm coax cables are standardized, so some cables are a little bit too long. The tules around the cable ends can have a different colour, but if necessary it can be replaced by the original one.

Cable length	Ordering number
20 cm	5322 321 21291
26 cm	5322 321 21293
31 cm	5322 321 21292

15.3.3 Miscellaneous cables and connectors	Ordering number
High voltage cable from X4602 on unit A20 to X1503 on unit A15	5322 321 23426
High current cable from X4404 on unit A19 to X528 on unit A12	5322 321 23425
Connector (5 pole) for X4401 on unit A19	5322 267 50452
Kontakt bush	5322 268 24128
Connector (3 pole) for X3001 on unit A16	5322 268 40233
Kontakt bush	5322 268 20165
Connector (3 pole) for X4402 on unit A19 X4601 on unit A20 X4603 on unit A20 X3304 on unit A33	5322 268 40233
Kontakt bush	5322 268 20165
Connector (4 pole) for X3002 on unit A16 for X1502 on unit A15	5322 268 40269
Connector (5 pole) for X104 on unit A1	5322 268 40279
Kontakt bush	5322 268 20152
Connector (4 pole) for X103 on unit A1	5322 268 40269
Kontakt bush	5322 268 20176

15.3.4 Coax connector socket (70 connectors per instrument)	
Outer part (bush)	5322 268 24116
Inner part (pin)	5322 268 14141

15.4 MAINS CORDS:

	Last digit 12nc of oscilloscope (on packing)	
European version	1	5322 321 21616
U.S.A. version	3	5322 321 10446
U.K. version	4	5322 321 21617
Swiss version	5	5322 321 21618
Australian version	8	5322 321 21781

15.5 TOOLS:

Oblique cutnipper	5322 395 90564
Cutnipper	5322 395 71004
Extension board	5322 216 51153

15.6 ELECTRICAL PARTS

The opening of parts, or removal of covers, is likely to expose live conductors. The instrument should therefore be disconnected from all voltage sources before any opening of parts or removal of covers is started.
During and after dismantling, bear in mind that capacitors in the instrument may still be charged even if the instrument has been separated from all voltage sources.

CAPACITORS

POSNR	DESCRIPTION	ORDERING CODE
	PGA SOCKET 68-P	5322 255 40815
	PGA SOCKET 68-P	5322 255 40815
C 0401	63V 10% 100NF	5322 121 42492
C 0402	63V 10% 100NF	5322 121 42492
C 0403	63V 10% 100NF	5322 121 42492
C 0404	63V 10% 100NF	5322 121 42492
C 0406	63V 10% 100NF	5322 121 42492
C 0407	63V 10% 100NF	5322 121 42492
C 0408	63V 10% 100NF	5322 121 42492
C 0409	63V 10% 100NF	5322 121 42492
C 0411	63V 10% 100NF	5322 121 42492
C 0412	63V 10% 100NF	5322 121 42492
C 0413	63V 10% 100NF	5322 121 42492
C 0414	63V 10% 100NF	5322 121 42492
C 0416	63V 10% 100NF	5322 121 42492
C 0417	63V 10% 100NF	5322 121 42492
C 0418	2% 27PF	4822 122 30045
C 0419	63V 10% 100NF	5322 121 42492
C 0421	63V 10% 100NF	5322 121 42492
C 0422	63V 10% 100NF	5322 121 42492
C 0424	63V 10% 100NF	5322 121 42492
C 0426	63V 10% 100NF	5322 121 42492
C 0427	63V 10% 100NF	5322 121 42492
C 0428	63V 10% 100NF	5322 121 42492
C 0429	63V 10% 100NF	5322 121 42492
C 0430	100V 10% 10NF	4822 121 41857
C 0431	63V 10% 100NF	5322 121 42492
C 0432	63V 10% 100NF	5322 121 42492
C 0433	10% 680PF	4822 122 30053
C 0434	100V 10% 10NF	4822 121 41857
C 0436	100V 10% 10NF	4822 121 41857
C 0437	100V 10% 10NF	4822 121 41857
C 0438	100V 10% 10NF	4822 121 41857
C 0439	-10+50% 68UF	4822 124 20689
C 0440	2% 100PF	4822 122 31316
C 0441	-10+50% 150UF	4822 124 20672
C 0442	-10+50% 150UF	4822 124 20672
C 0443	-10+50% 100UF	4822 124 20679
C 0444	-10+50% 100UF	4822 124 20679
C 0445	2% 100PF	4822 122 31316
C 0446	-10+50% 68UF	4822 124 20689
C 0447	-10+50% 68UF	4822 124 20689
C 0448	-10+50% 100UF	4822 124 20679
C 0449	-10+50% 100UF	4822 124 20679
C 0450	2% 100PF	4822 122 31316
C 0451	-10+50% 68UF	4822 124 20689
C 0452	-10+50% 68UF	4822 124 20689
C 0453	-10+50% 47UF	4822 124 20699
C 0454	-10+50% 150UF	4822 124 20672
C 0455	2% 100PF	4822 122 31316
C 0456	-10+50% 150UF	4822 124 20672
C 0457	-10+50% 100UF	4822 124 20679
C 0458	-10+50% 68UF	4822 124 20689
C 0459	-10+50% 68UF	4822 124 20689
C 0460	2% 100PF	4822 122 31316
C 0461	-10+50% 150UF	4822 124 20672
C 0462	-10+50% 15UF	4822 124 20729
C 0463	-10+50% 100UF	4822 124 20679
C 0464	-10+50% 100UF	4822 124 20679
C 0465	2% 100PF	4822 122 31316
C 0466	-10+50% 68UF	4822 124 20689
C 0467	-10+50% 68UF	4822 124 20689
C 0468	-10+50% 47UF	4822 124 20699
C 0469	63V 10% 100NF	5322 121 42492
C 0471	63V 10% 100NF	5322 121 42492
C 0472	-10+50% 100UF	4822 124 20679
C 0473	-10+50% 68UF	4822 124 20689
C 0474	63V 10% 100NF	5322 121 42492
C 0476	63V 10% 100NF	5322 121 42492
C 0477	63V 10% 100NF	5322 121 42492
C 0478	63V 10% 100NF	5322 121 42492
C 0479	-10+50% 68UF	4822 124 20689
C 0481	63V 10% 100NF	5322 121 42492
C 0482	63V 10% 100NF	5322 121 42492
C 0483	63V 10% 100NF	5322 121 42492
C 0484	63V 10% 100NF	5322 121 42492
C 0486	-10+50% 47UF	4822 124 20699
C 0487	-10+50% 150UF	4822 124 20672
C 0488	-10+50% 150UF	4822 124 20672
C 0489	-10+50% 150UF	4822 124 20672
C 0491	-10+50% 150UF	4822 124 20672
C 0492	100V 10% 10NF	4822 121 41857
C 0493	100V 10% 10NF	4822 121 41857
C 0494	63V 10% 100NF	5322 121 42492
C 0496	63V 10% 100NF	5322 121 42492
C 0497	63V 1% 10NF	5322 121 54154
C 0498	63V 1% 10NF	5322 121 54154
C 0499	63V 1% 10NF	5322 121 54154
C 0501	63V 1% 10NF	5322 121 54154
C 0502	63V 10% 100NF	5322 121 42492
C 0503	63V 10% 100NF	5322 121 42492
C 0504	63V 10% 100NF	5322 121 42492
C 0506	63V 10% 100NF	5322 121 42492
C 0507	63V 10% 100NF	5322 121 42492
C 0508	630V 1% 100PF	4822 121 50562
C 0509	63V 10% 100NF	5322 121 42492
C 0511	63V 10% 100NF	5322 121 42492
C 0512	63V 10% 100NF	5322 121 42492
C 0513	63V 10% 100NF	5322 121 42492
C 0514	63V 10% 100NF	5322 121 42492
C 0516	63V 10% 100NF	5322 121 42492
C 0517	63V 10% 100NF	5322 121 42492
C 0518	100V 10% 10NF	4822 121 41857
C 0519	10% 1NF	4822 122 30027
C 0521	10% 680PF	4822 122 30053
C 0522	100V 10% 10NF	4822 121 41857
C 0523	100V 10% 10NF	4822 121 41857
C 0524	100V 10% 10NF	4822 121 41857
C 0526	100V 10% 10NF	4822 121 41857
C 0527	63V 10% 100NF	5322 121 42492
C 0528	63V 10% 100NF	5322 121 42492
C 0529	63V 10% 100NF	5322 121 42492
C 0531	63V 10% 100NF	5322 121 42492
C 0532	63V 10% 100NF	5322 121 42492
C 0533	63V 10% 100NF	5322 121 42492
C 0534	63V 10% 100NF	5322 121 42492
C 0536	63V 10% 100NF	5322 121 42492
C 0537	63V 10% 100NF	5322 121 42492
C 0538	100V 10% 10NF	4822 121 41857
C 0539	10% 1NF	4822 122 30027
C 0541	10% 680PF	4822 122 30053
C 0542	100V 10% 10NF	4822 121 41857
C 0543	100V 10% 10NF	4822 121 41857
C 0544	100V 10% 10NF	4822 121 41857
C 0546	100V 10% 10NF	4822 121 41857
C 0547	63V 10% 100NF	5322 121 42492
C 0548	63V 10% 100NF	5322 121 42492
C 0549	63V 10% 100NF	5322 121 42492
C 0551	63V 10% 100NF	5322 121 42492
C 0552	63V 10% 100NF	5322 121 42492
C 0553	63V 10% 100NF	5322 121 42492
C 0554	63V 10% 100NF	5322 121 42492
C 0556	63V 10% 100NF	5322 121 42492
C 0557	63V 10% 100NF	5322 121 42492
C 0558	100V 10% 10NF	4822 121 41857
C 0559	10% 1NF	4822 122 30027

POSNR	DESCRIPTION	ORDERING CODE
C 0560	100V 10% 10NF	4822 121 41857
C 0561	10% 680PF	4822 122 30053
C 0562	100V 10% 10NF	4822 121 41857
C 0563	100V 10% 10NF	4822 121 41857
C 0564	100V 10% 10NF	4822 121 41857
C 0565	100V 10% 10NF	4822 121 41857
C 0566	100V 10% 10NF	4822 121 41857
C 0567	63V 10% 100NF	5322 121 42492
C 0568	63V 10% 100NF	5322 121 42492
C 0569	63V 10% 100NF	5322 121 42492
C 0571	63V 10% 100NF	5322 121 42492
C 0572	63V 10% 100NF	5322 121 42492
C 0573	63V 10% 100NF	5322 121 42492
C 0574	63V 10% 100NF	5322 121 42492
C 0576	63V 10% 100NF	5322 121 42492
C 0577	63V 10% 100NF	5322 121 42492
C 0578	100V 10% 10NF	4822 121 41857
C 0579	10% 1NF	4822 122 30027
C 0601	-10+50% 47UF	4822 124 20699
C 0602	-20+50% 10NF	4822 122 31414
C 0603	-20+50% 10NF	4822 122 31414
C 0604	2% 10PF	4822 122 32185
C 0606	-20+50% 10NF	4822 122 31414
C 0609	-10+50% 47UF	4822 124 20699
C 0611	-20+50% 10NF	4822 122 31414
C 0612	-10+50% 47UF	4822 124 20699
C 0613	-20+50% 10NF	4822 122 31414
C 0614	-20+50% 10NF	4822 122 31414
C 0616	-20+50% 10NF	4822 122 31414
C 0617	-20+50% 10NF	4822 122 31414
C 0618	-10+50% 47UF	4822 124 20699
C 0619	-20+50% 10NF	4822 122 31414
C 0621	-20+50% 10NF	4822 122 31414
C 0622	-10+50% 47UF	4822 124 20699
C 0623	-20+50% 10NF	4822 122 31414
C 0624	-10+50% 100UF	4822 124 20701
C 0626	-20+50% 10NF	4822 122 31414
C 0627	-10+50% 100UF	4822 124 20701
C 0628	-20+50% 10NF	4822 122 31414
C 0629	-10+50% 100UF	4822 124 20701
C 0631	-20+50% 10NF	4822 122 31414
C 0632	-10+50% 6.8UF	4822 124 20741
C 0633	-20+50% 10NF	4822 122 31414
C 0634	-10+50% 6.8UF	4822 124 20741
C 0636	-20+50% 10NF	4822 122 31414
C 0637	-10+50% 100UF	4822 124 20701
C 0638	-20+50% 10NF	4822 122 31414
C 0639	-20+50% 10NF	4822 122 31414
C 0641	-20+50% 10NF	4822 122 31414
C 0642	-20+50% 10NF	4822 122 31414
C 0643	-20+50% 10NF	4822 122 31414
C 0644	-20+50% 10NF	4822 122 31414
C 0646	-20+50% 10NF	4822 122 31414
C 0647	-20+50% 10NF	4822 122 31414
C 0648	-20+50% 10NF	4822 122 31414
C 0649	-20+50% 10NF	4822 122 31414
C 0651	-10+50% 47UF	4822 124 20699
C 0652	-20+50% 10NF	4822 122 31414
C 0654	-20+50% 10NF	4822 122 31414
C 0658	-10+50% 47UF	4822 124 20699
C 0659	-10+50% 47UF	4822 124 20699
C 0661	-10+50% 6.8UF	4822 124 20741
C 0662	-10+50% 6.8UF	4822 124 20741
C 0663	-10+50% 6.8UF	4822 124 20741
C 0664	-10+50% 330UF	4822 124 20705
C 0667	-20+50% 10NF	4822 122 31414
C 0701	-20+50% 10NF	4822 122 31414
C 0702	-10+50% 100UF	4822 124 20701
C 1201	-20+50% 10NF	4822 122 31414
C 1203	-20+50% 10NF	4822 122 31414
C 1204	-20+50% 10NF	4822 122 31414
C 1206	-20+50% 10NF	4822 122 31414
C 1207	-20+50% 10NF	4822 122 31414
C 1208	-20+50% 10NF	4822 122 31414
C 1216	-20+50% 10NF	4822 122 31414
C 1217	-20+50% 10NF	4822 122 31414
C 1219	-20+50% 10NF	4822 122 31414
C 1223	-20+50% 10NF	4822 122 31414
C 1224	-20+50% 10NF	4822 122 31414
C 1229	-20+50% 10NF	4822 122 31414
C 1234	-20+50% 10NF	4822 122 31414
C 1236	-20+50% 10NF	4822 122 31414
C 1237	-20+50% 10NF	4822 122 31414
C 1238	-20+50% 10NF	4822 122 31414
C 1239	-20+50% 10NF	4822 122 31414
C 1241	-20+50% 10NF	4822 122 31414
C 1242	-20+50% 10NF	4822 122 31414
C 1243	-20+50% 10NF	4822 122 31414
C 1244	-20+50% 10NF	4822 122 31414
C 1248	-20+50% 10NF	4822 122 31414
C 1249	-20+20% 10UF	5322 124 21956

POSNR	DESCRIPTION	ORDERING CODE
C 1251	-20+20% 33UF	5322 124 21957
C 1252	-20+50% 10NF	4822 122 31414
C 1253	-20+50% 10NF	4822 122 31414
C 1254	2% 56PF	4822 122 32027
C 1256	2% 68PF	4822 122 31349
C 1257	2% 56PF	4822 122 32027
C 1258	2% 56PF	4822 122 32027
C 1259	2% 56PF	4822 122 32027
C 1402	-20+20% 33UF	5322 124 21957
C 1403	-20+50% 10NF	4822 122 31414
C 1404	-20+50% 10NF	4822 122 31414
C 1406	-20+50% 10NF	4822 122 31414
C 1407	-20+50% 10NF	4822 122 31414
C 1408	-20+50% 10NF	4822 122 31414
C 1409	-20+50% 10NF	4822 122 31414
C 1411	-20+50% 10NF	4822 122 31414
C 1412	-20+50% 10NF	4822 122 31414
C 1413	-20+50% 10NF	4822 122 31414
C 1414	2% 12PF	4822 122 31056
C 1416	2% 100PF	4822 122 31316
C 1701	-20+50% 10NF	4822 122 31414
C 1702	-20+50% 10NF	4822 122 31414
C 1704	-20+50% 10NF	4822 122 31414
C 1717	-20+50% 10NF	4822 122 31414
C 1718	-20+50% 10NF	4822 122 31414
C 1719	-20+50% 10NF	4822 122 31414
C 1721	-20+50% 10NF	4822 122 31414
C 1722	-20+50% 10NF	4822 122 31414
C 1723	-20+50% 10NF	4822 122 31414
C 1724	-20+50% 10NF	4822 122 31414
C 1726	-20+50% 10NF	4822 122 31414
C 1727	-20+50% 10NF	4822 122 31414
C 1728	-20+50% 10NF	4822 122 31414
C 1731	-20+50% 10NF	4822 122 31414
C 1746	-20+50% 10NF	4822 122 31414
C 1747	-20+50% 10NF	4822 122 31414
C 1751	-20+20% 33UF	5322 124 21957
C 1752	-20+20% 33UF	5322 124 21957
C 1753	-20+20% 33UF	5322 124 21957
C 1754	0.25PF 0.56PF	5322 122 32107
C 1756	2% 150PF	4822 122 31413
C 1757	2% 33PF	5322 122 32072
C 1758	2% 100PF	4822 122 31316
C 1759	2% 150PF	4822 122 31413
C 1761	2% 100PF	4822 122 31316
C 1762	0.25PF 6.8PF	4822 122 31049
C 1772	-20+20% 33UF	5322 124 21957
C 1773	-20+20% 33UF	5322 124 21957
C 1776	-20+20% 33UF	5322 124 21957
C 1777	-20+20% 33UF	5322 124 21957
C 1778	-20+20% 33UF	5322 124 21957
C 1791	2% 100PF	4822 122 31316
C 1792	2% 330PF	4822 122 31353
C 1801	-20+50% 10NF	4822 122 31414
C 1802	-20+50% 10NF	4822 122 31414
C 1803	-20+50% 10NF	4822 122 31414
C 1804	-20+50% 10NF	4822 122 31414
C 1806	-20+50% 10NF	4822 122 31414
C 1807	-20+50% 10NF	4822 122 31414
C 1808	-20+50% 10NF	4822 122 31414
C 1809	-20+50% 10NF	4822 122 31414
C 1811	-20+50% 10NF	4822 122 31414
C 1812	-20+50% 10NF	4822 122 31414
C 1813	-20+50% 10NF	4822 122 31414
C 1814	-20+50% 10NF	4822 122 31414
C 1816	-20+50% 10NF	4822 122 31414
C 1817	-20+50% 10NF	4822 122 31414
C 1818	-20+50% 10NF	4822 122 31414
C 1819	-20+50% 10NF	4822 122 31414
C 1821	-20+50% 10NF	4822 122 31414
C 1822	-20+50% 10NF	4822 122 31414
C 1823	-20+50% 10NF	4822 122 31414
C 1824	-20+50% 10NF	4822 122 31414
C 1826	-20+50% 10NF	4822 122 31414
C 1827	-20+50% 10NF	4822 122 31414
C 1828	-20+50% 10NF	4822 122 31414
C 1829	-20+50% 10NF	4822 122 31414
C 1831	-20+50% 10NF	4822 122 31414
C 1832	-20+50% 10NF	4822 122 31414
C 1833	-20+50% 10NF	4822 122 31414
C 1834	-20+50% 10NF	4822 122 31414
C 1836	-20+50% 10NF	4822 122 31414
C 1837	-20+50% 10NF	4822 122 31414
C 1838	-20+50% 10NF	4822 122 31414
C 1839	-20+20% 10UF	5322 124 21956
C 1841	-20+20% 10UF	5322 124 21956
C 1842	-20+20% 10UF	5322 124 21956
C 1843	-20+20% 10UF	5322 124 21956
C 2112	-20+50% 10NF	4822 122 31414
C 2113	-20+50% 10NF	4822 122 31414
C 2121	-20+50% 10NF	4822 122 31414

POSNR	DESCRIPTION		ORDERING CODE
C 1844	-20+20%	10UF	5322 124 21956
C 1846	-20+20%	10UF	5322 124 21956
C 1847	-20+20%	10UF	5322 124 21956
C 1851	2%	56PF	4822 122 32027
C 1852	2%	330PF	4822 122 31353
C 1853	2%	56PF	4822 122 32027
C 2002	-20+50%	10NF	4822 122 31414
C 2006	-20+50%	10NF	4822 122 31414
C 2008	-20+50%	10NF	4822 122 31414
C 2009	-20+50%	10NF	4822 122 31414
C 2011	-20+50%	10NF	4822 122 31414
C 2012	-20+50%	10NF	4822 122 31414
C 2013	-20+50%	10NF	4822 122 31414
C 2014	-20+50%	10NF	4822 122 31414
C 2016	-20+50%	10NF	4822 122 31414
C 2017	-20+50%	10NF	4822 122 31414
C 2018	-20+50%	10NF	4822 122 31414
C 2022	-20+50%	10NF	4822 122 31414
C 2023	-20+50%	10NF	4822 122 31414
C 2024	-20+50%	10NF	4822 122 31414
C 2027	-20+50%	10NF	4822 122 31414
C 2028	-20+50%	10NF	4822 122 31414
C 2029	-20+50%	10NF	4822 122 31414
C 2031	-20+50%	10NF	4822 122 31414
C 2034	-20+50%	10NF	4822 122 31414
C 2038	-20+50%	10NF	4822 122 31414
C 2039	-20+50%	10NF	4822 122 31414
C 2041	-20+20%	6.8UF	5322 124 21763
C 2043	-20+20%	6.8UF	5322 124 21763
C 2044	-20+20%	6.8UF	5322 124 21763
C 2046	-20+20%	6.8UF	5322 124 21763
C 2047	2%	68PF	4822 122 31349
C 2048	0.25PF	5.6PF	5322 122 32163
C 2101	-20+50%	10NF	4822 122 31414
C 2102	-20+50%	10NF	4822 122 31414
C 2103	-20+50%	10NF	4822 122 31414
C 2104	-20+50%	10NF	4822 122 31414
C 2106	-20+50%	10NF	4822 122 31414
C 2107	-20+50%	10NF	4822 122 31414
C 2108	-20+50%	10NF	4822 122 31414
C 2122	-20+50%	10NF	4822 122 31414
C 2123	-20+50%	10NF	4822 122 31414
C 2124	-20+50%	10NF	4822 122 31414
C 2126	-20+50%	10NF	4822 122 31414
C 2128	-20+50%	10NF	4822 122 31414
C 2129	-20+50%	10NF	4822 122 31414
C 2134	-20+50%	10NF	4822 122 31414
C 2136	-20+50%	10NF	4822 122 31414
C 2137	-20+50%	10NF	4822 122 31414
C 2139	-20+50%	10NF	4822 122 31414
C 2141	-20+50%	10NF	4822 122 31414
C 2142	-20+50%	10NF	4822 122 31414
C 2146	-20+50%	10NF	4822 122 31414
C 2148	-20+50%	10NF	4822 122 31414
C 2149	-20+50%	10NF	4822 122 31414
C 2151	-20+50%	10NF	4822 122 31414
C 2154	-20+50%	10NF	4822 122 31414
C 2156	-20+50%	10NF	4822 122 31414
C 2157	-20+20%	6.8UF	5322 124 21763
C 2158	-20+50%	10NF	4822 122 31414
C 2159	-20+20%	6.8UF	5322 124 21763
C 2161	10%	2.2NF	4822 122 30114
C 2162	-20+50%	4.7NF	4822 122 30128
C 2164	-20+50%	10NF	4822 122 31414
C 2166	-20+50%	6.8NF	4822 122 31429
C 2167	10%	680PF	4822 122 30053
C 2168	-20+20%	6.8UF	5322 124 21763
C 2169	-10+50%	33UF	4822 124 20712
C 2171	-20+20%	6.8UF	5322 124 21763
C 2172	2%	10PF	4822 122 32185
C 2173	2%	68PF	4822 122 31349
C 2301	-20+20%	6.8UF	5322 124 21763
C 2302	-20+50%	10NF	4822 122 31414
C 2306	-20+50%	10NF	4822 122 31414
C 2319	-20+50%	10NF	4822 122 31414
C 2321	-20+50%	10NF	4822 122 31414
C 2322	-20+50%	10NF	4822 122 31414
C 2323	-20+50%	10NF	4822 122 31414
C 2327	-20+50%	10NF	4822 122 31414
C 2334	-20+20%	6.8UF	5322 124 21763
C 2336	-20+50%	10NF	4822 122 31414
C 2339	63V 10%	100NF	5322 121 42492
C 2341	-20+20%	6.8UF	5322 124 21763
C 2343	-20+20%	6.8UF	5322 124 21763
C 2348	2%	100PF	4822 122 31316
C 2349	2%	100PF	4822 122 31316
C 2351	2%	220PF	4822 122 30094
C 2352	2%	220PF	4822 122 30094
C 2353	63V 10%	100NF	5322 121 42492
C 2354	-20+50%	10NF	4822 122 31414

POSNR	DESCRIPTION		ORDERING CODE
C 2356	-20+20%	6.8UF	5322 124 21763
C 2357	63V 10%	100NF	5322 121 42492
C 2358	-20+50%	10NF	4822 122 31414
C 2359	-20+20%	6.8UF	5322 124 21763
C 2361	-20+50%	10NF	4822 122 31414
C 2363	63V 10%	100NF	5322 121 42492
C 2364	-20+50%	10NF	4822 122 31414
C 2366	630V 1%	316PF	4822 121 50531
C 2367	630V 1%	316PF	4822 121 50531
C 2369	2%	330PF	4822 122 31353
C 2373	2%	39PF	4822 122 31069
C 2374	63V 10%	100NF	5322 121 42492
C 2376	-20+50%	10NF	4822 122 31414
C 2377	-20+50%	10NF	4822 122 31414
C 2378	-20+50%	10NF	4822 122 31414
C 2379	630V 1%	316PF	4822 121 50531
C 2381	630V 1%	316PF	4822 121 50531
C 2382	-20+50%	10NF	4822 122 31414
C 2383	2%	330PF	4822 122 31353
C 2384	2%	39PF	4822 122 31069
C 2389	-20+50%	10NF	4822 122 31414
C 2391	-20+50%	10NF	4822 122 31414
C 2392	-20+50%	10NF	4822 122 31414
C 2393	-20+20%	6.8UF	5322 124 21961
C 2394	63V 10%	100NF	5322 121 42492
C 2397	-20+50%	10NF	4822 122 31414
C 2398	-20+20%	6.8UF	5322 124 21763
C 2399	-20+50%	10NF	4822 122 31414
C 2401	-20+20%	6.8UF	5322 124 21763
C 2402	63V 10%	100NF	5322 121 42492
C 2403	-20+50%	10NF	4822 122 31414
C 2404	-20+50%	10NF	4822 122 31414
C 2406	-20+50%	10NF	4822 122 31414
C 2407	-20+50%	10NF	4822 122 31414
C 2408	-20+50%	10NF	4822 122 31414
C 2409	-20+50%	10NF	4822 122 31414
C 2411	2%	56PF	4822 122 32027
C 2412	2%	56PF	4822 122 32027
C 2501	-10+50%	22UF	4822 124 20731
C 2502	-20+50%	10NF	4822 122 31414
C 2503	-20+50%	10NF	4822 122 31414
C 2504	-10+50%	22UF	4822 124 20731
C 2513	400V 10%	100NF	5322 121 44198
C 2514	2%	100PF	5322 122 32655
C 2522	-10+50%	47UF	4822 124 20699
C 2523	-20+50%	10NF	4822 122 31414
C 2524	-20+50%	10NF	4822 122 31414
C 2526	-20+50%	10NF	4822 122 31414
C 2527	-20+50%	10NF	4822 122 31414
C 2528	-20+50%	10NF	4822 122 31414
C 2534	-10+50%	47UF	4822 124 20699
C 2536	-20+50%	10NF	4822 122 31414
C 2537	-20+50%	10NF	4822 122 31414
C 2547	-10+50%	100UF	4822 124 20679
C 2551	-20+50%	10NF	4822 122 31414
C 2552	-20+50%	10NF	4822 122 31414
C 2553	-20+50%	10NF	4822 122 31414
C 2559	-10+50%	100UF	4822 124 20679
C 2561	-20+50%	10NF	4822 122 31414
C 2562	-20+50%	10NF	4822 122 31414
C 2563	-20+50%	10NF	4822 122 31414
C 2564	-20+50%	10NF	4822 122 31414
C 2566	-20+50%	10NF	4822 122 31414
C 2572	-10+50%	100UF	4822 124 20679
C 2573	-20+50%	10NF	4822 122 31414
C 2574	-20+50%	10NF	4822 122 31414
C 2583	-20+50%	10NF	4822 122 31414
C 2584	-20+50%	10NF	4822 122 31414
C 2587	-20+50%	10NF	4822 122 31414
C 2591	2%	100PF	4822 122 31316
C 2592	2%	100PF	4822 122 31316
C 2594	63V 10%	100NF	5322 121 42492
C 2595	63V 10%	100NF	5322 121 42492
C 2596	-20+50%	10NF	4822 122 31414
C 2597	-20+50%	10NF	4822 122 31414
C 2613	0.25PF	0.56PF	5322 122 32107
C 2616	2%	39PF	4822 122 31069
C 2617	2%	39PF	4822 122 31069
C 2621	10%	470PF	4822 122 30034
C 2626	100V 10%	47NF	5322 121 42491
C 2627	2%	220PF	4822 122 30094
C 2632	-20+50%	10NF	4822 122 31414
C 2633	-20+50%	10NF	4822 122 31414
C 2642	-20+50%	10NF	4822 122 31414
C 2643	-20+50%	10NF	4822 122 31414
C 2646	-20+50%	10NF	4822 122 31414
C 2651	-20+50%	10NF	4822 122 31414
C 2652	-20+20%	6.8UF	5322 124 21763
C 2653	2%	100PF	4822 122 31316
C 2661	-20+50%	10NF	4822 122 31414
C 2662	-20+50%	10NF	4822 122 31414

POSNR	DESCRIPTION	ORDERING CODE
C 2663	-20+50% 10NF	4822 122 31414
C 2664	-20+50% 10NF	4822 122 31414
C 2666	2% 47PF	4822 122 31072
C 2801	400V 10% 100NF	5322 121 44198
C 2802	-20+50% 10NF	4822 122 31414
C 2803	20% 470PF	5322 122 50086
C 2804	2% 100PF	4822 122 31316
C 2805	-20+50% 10NF	5322 122 50091
C 2806	20% 1NF	5322 122 50077
C 2807	400V 10% 100NF	5322 121 44198
C 2808	-20+50% 10NF	5322 122 50091
C 2810	-20+50% 10NF	5322 122 50091
C 2811	-20+50% 10NF	4822 122 31414
C 2812	-20+50% 10NF	4822 122 31414
C 2813	-20+50% 10NF	4822 122 31414
C 2814	-20+50% 10NF	4822 122 31414
C 4001	2% 100PF	4822 122 31316
C 4002	2% 100PF	4822 122 31316
C 4003	2% 100PF	4822 122 31316
C 4004	2% 100PF	4822 122 31316
C 4006	2% 100PF	4822 122 31316
C 4007	2% 100PF	4822 122 31316
C 4008	2% 100PF	4822 122 31316
C 4009	2% 100PF	4822 122 31316
C 4011	2% 100PF	4822 122 31316
C 4012	2% 100PF	4822 122 31316
C 4013	2% 100PF	4822 122 31316
C 4014	2% 100PF	4822 122 31316
C 4016	2% 100PF	4822 122 31316
C 4017	2% 100PF	4822 122 31316
C 4018	2% 100PF	4822 122 31316
C 4019	2% 100PF	4822 122 31316
C 4021	2% 100PF	4822 122 31316
C 4022	2% 100PF	4822 122 31316
C 4023	2% 100PF	4822 122 31316
C 4024	2% 100PF	4822 122 31316
C 4026	2% 100PF	4822 122 31316
C 4027	2% 100PF	4822 122 31316
C 4028	-20+50% 10NF	4822 122 31414
C 4029	-20+50% 10NF	4822 122 31414
C 4031	-20+50% 10NF	4822 122 31414
C 4032	-10+50% 150UF	4822 124 20672
C 4033	-10+50% 150UF	4822 124 20672
C 4034	-10+50% 150UF	4822 124 20672
C 4036	-20+50% 10NF	4822 122 31414
C 4037	-20+50% 10NF	4822 122 31414
C 4038	-20+50% 10NF	4822 122 31414
C 4039	-20+50% 10NF	4822 122 31414
C 4041	-20+50% 10NF	4822 122 31414
C 4042	-20+50% 10NF	4822 122 31414
C 4043	-20+50% 10NF	4822 122 31414
C 4044	-20+50% 10NF	4822 122 31414
C 4046	-20+50% 10NF	4822 122 31414
C 4047	-20+50% 10NF	4822 122 31414
C 4048	-20+50% 10NF	4822 122 31414
C 4206	-10+50% 150UF	4822 124 20672
C 4207	-10+50% 150UF	4822 124 20672
C 4208	-20+50% 10NF	4822 122 31414
C 4209	-20+50% 10NF	4822 122 31414
C 4211	-20+50% 10NF	4822 122 31414
C 4212	-20+50% 10NF	4822 122 31414
C 4213	-20+50% 10NF	4822 122 31414
C 4214	-20+50% 10NF	4822 122 31414
C 4216	-20+50% 10NF	4822 122 31414
C 4217	-20+50% 10NF	4822 122 31414
C 4401	250V 10% 220NF	5322 121 44142
C 4402	ME275 20% 2.2NF	5322 121 42978
C 4403	-20+50% 10NF	4822 122 31414
C 4404	-20+50% 10NF	4822 122 31414
C 4405	100V 10% 47NF	5322 121 42491
C 4406	-20+50% 10NF	4822 122 31414
C 4407	ME275 20% 2.2NF	5322 121 42978
C 4408	63V 10% 470NF	5322 121 42979
C 4409	-20+50% 10NF	4822 122 31414
C 4411	63V 10% 100NF	5322 121 42492
C 4412	-20+50% 10NF	4822 122 31414
C 4413	-20+50% 10NF	4822 122 31414
C 4414	63V 10% 100NF	5322 121 42492
C 4416	-20+20% 330UF	5322 124 21472
C 4417	-20+20% 330UF	5322 124 21472
C 4418	-20+20% 150UF	4822 124 21695
C 4419	160V 1% 33NF	5322 121 50997
C 4422	2000V 5% 2.2NF	4822 121 41339
C 4423	63V 10% 100NF	5322 121 42492
C 4424	-10+50% 22UF	4822 124 20731
C 4427	2% 220PF	4822 122 30094
C 4428	-20+50% 10NF	4822 122 31414
C 4429	-20+20% 6800UF	4822 124 40692
C 4430	100V 10% 22NF	4822 121 41856
C 4431	-20+20% 6800UF	4822 124 40692
C 4432	-20+20% 6800UF	4822 124 40692

POSNR	DESCRIPTION	ORDERING CODE
C 4433	-20+20% 6800UF	4822 124 40692
C 4434	-10+50% 680UF	4822 124 20685
C 4436	-20+20% 6800UF	4822 124 40692
C 4437	-10+50% 680UF	4822 124 20685
C 4438	-20+20% 6800UF	4822 124 40692
C 4439	-10+50% 680UF	4822 124 20685
C 4442	63V 10% 470NF	5322 121 42979
C 4443	-20+20% 10000UF	5322 124 21343
C 4446	-10+50% 470UF	4822 124 20695
C 4447	-20+20% 10000UF	5322 124 21343
C 4449	-10+50% 470UF	4822 124 20695
C 4451	-10+50% 330UF	4822 124 20705
C 4452	-10+50% 330UF	4822 124 20705
C 4453	-10+50% 330UF	4822 124 20705
C 4454	-10+50% 330UF	4822 124 20705
C 4456	-10+50% 22UF	5322 124 21768
C 4457	-10+50% 100UF	4822 124 20735
C 4458	-10+50% 22UF	4822 124 20731
C 4459	-10+50% 10UF	4822 124 21129
C 4461	-10+50% 100UF	4822 124 20679
C 4462	63V 10% 100NF	5322 121 42492
C 4471	10% 1NF	4822 122 30027
C 4472	63V 10% 680NF	5322 121 42498
C 4473	10% 1NF	4822 122 30027
C 4474	100V 10% 22NF	4822 121 41856
C 4476	2% 100PF	5322 122 32655
C 4477	2% 100PF	5322 122 32655
C 4478	2% 100PF	5322 122 32655
C 4479	-20+50% 1.5NF	5322 122 50092
C 4601	63V 10% 100NF	5322 121 42492
C 4602	-10+50% 68UF	4822 124 20689
C 4603	10% 4.7NF	4822 122 31125
C 4604	-10+10% 33PF	5322 122 33081
C 4606	100V 10% 47NF	5322 121 42491
C 4607	2% 47PF	4822 122 31072
C 4608	63V 10% 100NF	5322 121 42492
C 4609	10% 4.7NF	4822 122 31125
C 4611	10% 1NF	4822 122 30027
C 4613	-10+50% 68UF	4822 124 20734
C 4614	-20+50% 10NF	5322 122 50091
C 4616	-20+50% 2.2NF	5322 122 50093
C 4617	63V 10% 220NF	4822 121 42408
C 4618	-10+50% 10UF	4822 124 20742
C 4619	100V 10% 47NF	5322 121 42491
C 4621	-10+50% 33UF	4822 124 20712
C 4622	63V 10% 680NF	5322 121 42498
C 4623	10% 1NF	4822 122 30027
C 4624	-10+50% 150UF	4822 124 20716
C 4625	10% 3.3NF	4822 122 30099
C 4626	-10+50% 33UF	4822 124 20712
C 4627	-10+50% 33UF	4822 124 20712
C 4628	-10+50% 33UF	4822 124 20712
C 4629	-20+20% 2200UF	4822 124 21324
C 4702	V 5% 15PF	5322 122 32481
C 4703	V 10% 22NF	5322 122 32654
C 4704	V 10% 22NF	5322 122 32654
C 4706	0.25PF 4.7PF	5322 122 33082
C 4708	V 5% 22PF	5322 122 32658
C 4709	V 0.25PF 4.7PF	5322 122 32287
C 4711	V 5% 15PF	5322 122 32481
C 4712	V 10% 22NF	5322 122 32654
C 4713	V 10% 22NF	5322 122 32654
C 4714	V 0.25PF 1PF	5322 122 32447
C 4716	V 10% 22NF	5322 122 32654
C 4717	V 10% 22NF	5322 122 32654
C 4718	V 0.5PF 5.6PF	5322 122 32967
C 4720	V 10% 22NF	5322 122 32654
C 4721	V 10% 22NF	5322 122 32654
C 4722	V 5% 1NF	5322 122 32531
C 4723	V 10% 22NF	5322 122 32654
C 4724	V 10% 22NF	5322 122 32654
C 4726	V 10% 22NF	5322 122 32654
C 4727	V 10% 22NF	5322 122 32654
C 4728	V 10% 22NF	5322 122 32654
C 4729	V 10% 22NF	5322 122 32654
C 4731	V 10% 22NF	5322 122 32654
C 4732	V 10% 22NF	5322 122 32654
C 4733	V 10% 22NF	5322 122 32654
C 4734	V 10% 22NF	5322 122 32654
C 4736	V 10% 22NF	5322 122 32654
C 4737	-10+50% 68UF	4822 124 20689
C 4738	-10+50% 68UF	4822 124 20689
C 4739	-10+50% 68UF	4822 124 20689
C 4741	-10+50% 68UF	4822 124 20689
C 4742	400V 10% 22NF	5322 121 40308
C 4743	63V 10% 100NF	5322 121 42492
C 4744	-20+50% 10NF	4822 122 31414
C 4746	-20+50% 10NF	4822 122 31414
C 4747	-20+50% 10NF	4822 122 31414
C 4748	2% 22PF	5322 122 32143
C 4749	2% 220PF	4822 122 30094

POSNR	DESCRIPTION		ORDERING CODE
C 4751	-20+50%	10NF	4822 122 31414
C 4752	-20+50%	10NF	4822 122 31414
C 4753	2%	220PF	4822 122 30094
C 4754	-20+50%	10NF	4822 122 31414
C 4756	-20+50%	10NF	4822 122 31414
C 4757	-10+50%	68UF	4822 124 20689
C 4758	-10+50%	68UF	4822 124 20689
C 4759	-20+50%	10NF	4822 122 31414
C 4761	V 10%	22NF	5322 122 32654
C 4765	V 5%	1NF	5322 122 32531
C 4766	V 5%	1NF	5322 122 32531
C 4802	V 5%	15PF	5322 122 32481
C 4803	V 10%	22NF	5322 122 32654
C 4804	V 10%	22NF	5322 122 32654
C 4806	0.25PF	4.7PF	5322 122 33082
C 4808	V 5%	22PF	5322 122 32658
C 4809	V 0.25PF	4.7PF	5322 122 32287
C 4811	V 5%	15PF	5322 122 32481
C 4812	V 10%	22NF	5322 122 32654
C 4813	V 10%	22NF	5322 122 32654
C 4814	V 0.25PF	1PF	5322 122 32447
C 4816	V 10%	22NF	5322 122 32654
C 4817	V 10%	22NF	5322 122 32654
C 4818	V 0.5PF	5.6PF	5322 122 32967
C 4820	V 10%	22NF	5322 122 32654
C 4821	V 10%	22NF	5322 122 32654
C 4822	V 5%	1NF	5322 122 32531
C 4823	V 10%	22NF	5322 122 32654
C 4824	V 10%	22NF	5322 122 32654
C 4826	V 10%	22NF	5322 122 32654
C 4827	V 10%	22NF	5322 122 32654
C 4828	V 10%	22NF	5322 122 32654
C 4829	V 10%	22NF	5322 122 32654
C 4831	V 10%	22NF	5322 122 32654
C 4832	V 10%	22NF	5322 122 32654
C 4833	V 10%	22NF	5322 122 32654
C 4834	V 10%	22NF	5322 122 32654
C 4836	V 10%	22NF	5322 122 32654
C 4837	-10+50%	68UF	4822 124 20689
C 4838	-10+50%	68UF	4822 124 20689
C 4839	-10+50%	68UF	4822 124 20689
C 4841	-10+50%	68UF	4822 124 20689
C 4847	-20+50%	10NF	4822 122 31414
C 4848	2%	22PF	5322 122 32143
C 4849	2%	220PF	4822 122 30094
C 4851	-20+50%	10NF	4822 122 31414
C 4854	-20+50%	10NF	4822 122 31414
C 4856	-20+50%	10NF	4822 122 31414
C 4857	-10+50%	68UF	4822 124 20689
C 4858	-10+50%	68UF	4822 124 20689
C 4861	V 10%	22NF	5322 122 32654
C 4865	V 5%	1NF	5322 122 32531
C 4866	V 5%	1NF	5322 122 32531
C 5001	-20+50%	10NF	4822 122 31414
C 5002	-20+50%	10NF	4822 122 31414
C 5003	-20+50%	10NF	4822 122 31414
C 5004	0.25PF	01.8PF	5322 122 32313
C 5005	-20+50%	10NF	4822 122 31414
C 5008	63V 10%	100NF	5322 121 42492
C 5009	63V 10%	100NF	5322 121 42492
C 5011	100V 10%	33NF	5322 121 42489
C 5012	10%	4.7NF	4822 122 31125
C 5013	63V 10%	470NF	5322 121 42979
C 5014	10%	1.5NF	4822 122 31169
C 5015	63V 10%	470NF	5322 121 42979
C 5016	-20+50%	10NF	4822 122 31414
C 5017	2%	10PF	4822 122 32185
C 5018	2%	10PF	4822 122 32185
C 5020	100V 10%	10NF	4822 121 41857
C 5021	-20+50%	10NF	4822 122 31414
C 5022	-20+50%	10NF	4822 122 31414
C 5023	-20+50%	10NF	4822 122 31414
C 5024	-20+50%	10NF	4822 122 31414
C 5025	63V 10%	100NF	5322 121 42492
C 5026	-20+50%	10NF	4822 122 31414
C 5027	-20+50%	10NF	4822 122 31414
C 5101	-20+50%	10NF	4822 122 31414
C 5102	-20+50%	10NF	4822 122 31414
C 5103	-20+50%	10NF	4822 122 31414
C 5104	0.25PF	01.8PF	5322 122 32313
C 5105	-20+50%	10NF	4822 122 31414
C 5108	63V 10%	100NF	5322 121 42492
C 5109	63V 10%	100NF	5322 121 42492
C 5111	100V 10%	33NF	5322 121 42489
C 5112	10%	4.7NF	4822 122 31125
C 5113	63V 10%	470NF	5322 121 42979
C 5114	10%	1.5NF	4822 122 31169
C 5115	63V 10%	470NF	5322 121 42979
C 5116	-20+50%	10NF	4822 122 31414
C 5117	2%	10PF	4822 122 32185

POSNR	DESCRIPTION		ORDERING CODE
C 5120	100V 10%	10NF	4822 121 41857
C 5121	-20+50%	10NF	4822 122 31414
C 5122	-20+50%	10NF	4822 122 31414
C 5123	-20+50%	10NF	4822 122 31414
C 5124	-20+50%	10NF	4822 122 31414
C 5125	63V 10%	100NF	5322 121 42492
C 5126	-20+50%	10NF	4822 122 31414
C 5127	-20+50%	10NF	4822 122 31414
C 5201	-20+20%	6.8UF	5322 124 21961
C 5202	-20+50%	10NF	4822 122 31414
C 5203	-20+50%	10NF	4822 122 31414
C 5204	-20+50%	10NF	4822 122 31414
C 5205	-20+50%	10NF	4822 122 31414
C 5206	63V 10%	470NF	5322 121 42979
C 5207	-20+50%	10NF	4822 122 31414
C 5208	-20+50%	10NF	4822 122 31414
C 5209	-20+50%	10NF	4822 122 31414
C 5210	-20+50%	10NF	4822 122 31414
C 5211	-20+20%	6.8UF	5322 124 21763
C 5212	-20+50%	10NF	4822 122 31414
C 5213	-20+20%	6.8UF	5322 124 21763
C 5214	-20+50%	10NF	4822 122 31414
C 5221	-20+20%	6.8UF	5322 124 21763
C 5222	-20+50%	10NF	4822 122 31414
C 5223	-20+20%	6.8UF	5322 124 21763
C 5231	-20+20%	33UF	5322 124 21957
C 5232	-20+50%	10NF	4822 122 31414
C 5233	-20+50%	10NF	4822 122 31414
C 5241	-20+20%	33UF	5322 124 21957
C 5242	-20+50%	10NF	4822 122 31414
C 5244	-20+50%	10NF	4822 122 31414
C 5251	-20+20%	6.8UF	5322 124 21763
C 5252	-20+20%	6.8UF	5322 124 21763
C 5253	-20+50%	10NF	4822 122 31414
C 5254	-20+50%	10NF	4822 122 31414
C 5256	-20+50%	10NF	4822 122 31414
C 5257	-20+50%	10NF	4822 122 31414
C 5260	-20+50%	10NF	4822 122 31414
C 5261	-20+20%	6.8UF	5322 124 21763
C 5262	-20+20%	6.8UF	5322 124 21763
C 5263	-20+50%	10NF	4822 122 31414
C 5264	-20+50%	10NF	4822 122 31414
C 5266	-20+50%	10NF	4822 122 31414
C 5267	-20+50%	10NF	4822 122 31414
C 5268	-20+50%	10NF	4822 122 31414
C 5269	-20+50%	10NF	4822 122 31414
C 5270	-20+50%	10NF	4822 122 31414
C 5271	-20+50%	10NF	4822 122 31414
C 5272	-20+50%	10NF	4822 122 31414
C 5273	-20+50%	10NF	4822 122 31414
C 5274	-20+50%	10NF	4822 122 31414
C 5276	-20+50%	10NF	4822 122 31414
C 5302	V 10%	22NF	5322 122 32654
C 5303	V 5%	10PF	5322 122 32448
C 5304	V 10%	22NF	5322 122 32654
C 5306	V 10%	22NF	5322 122 32654
C 5307	V 10%	22NF	5322 122 32654
C 5308	V 10%	22NF	5322 122 32654
C 5332	V 10%	22NF	5322 122 32654
C 5333	V 5%	10PF	5322 122 32448
C 5334	V 10%	22NF	5322 122 32654
C 5336	V 10%	22NF	5322 122 32654
C 5337	V 10%	22NF	5322 122 32654
C 5338	V 10%	22NF	5322 122 32654
C 5401	V 10%	22NF	5322 122 32654
C 5403	V 10%	22NF	5322 122 32654
C 5407	V 10%	22NF	5322 122 32654
C 5408	V 10%	22NF	5322 122 32654
C 5409	V 5%	47PF	5322 122 32452
C 5412	V 10%	22NF	5322 122 32654
C 5413	V 10%	22NF	5322 122 32654
C 5414	V 10%	22NF	5322 122 32654
C 5441	V 10%	22NF	5322 122 32654
C 5443	V 10%	22NF	5322 122 32654
C 5447	V 10%	22NF	5322 122 32654
C 5448	V 10%	22NF	5322 122 32654
C 5449	V 5%	47PF	5322 122 32452
C 5452	V 10%	22NF	5322 122 32654
C 5453	V 10%	22NF	5322 122 32654
C 5454	V 10%	22NF	5322 122 32654
C 6001	-10+50%	150UF	4822 124 20672
C 6002	63V 10%	100NF	5322 121 42492
C 6003	63V 10%	100NF	5322 121 42492
C 6004	63V 10%	100NF	5322 121 42492
C 6006	63V 10%	100NF	5322 121 42492
C 6007	63V 10%	100NF	5322 121 42492
C 6008	63V 10%	100NF	5322 121 42492
C 6009	63V 10%	100NF	5322 121 42492
C 6011	-20+50%	10NF	4822 122 31414
C 6012	-10+50%	150UF	4822 124 20672

POSNR	DESCRIPTION	ORDERING CODE
C 6016	63V 10% 100NF	5322 121 42492
C 6017	-10+50% 6.8UF	4822 124 20741
C 6018	63V 10% 100NF	5322 121 42492
C 6019	-10+50% 6.8UF	4822 124 20741
C 6020	63V 10% 100NF	5322 121 42492
C 6021	10% 1NF	4822 122 30027
C 6022	63V 10% 100NF	5322 121 42492
C 6023	-20+50% 10NF	4822 122 31414
C 6024	-20+50% 10NF	4822 122 31414
C 6025	-20+50% 10NF	4822 122 31414
C 6026	-20+50% 10NF	4822 122 31414
C 6027	63V 10% 100NF	5322 121 42492
C 6028	-20+20% 10UF	5322 124 21956
C 6029	-20+50% 10NF	4822 122 31414
C 6030	63V 10% 100NF	5322 121 42492
C 6031	63V 10% 100NF	5322 121 42492
C 6032	63V 10% 100NF	5322 121 42492
C 6033	63V 10% 100NF	5322 121 42492
C 6034	63V 10% 100NF	5322 121 42492
C 6036	63V 10% 100NF	5322 121 42492
C 6037	63V 10% 100NF	5322 121 42492
C 6038	63V 10% 100NF	5322 121 42492
C 6039	63V 10% 100NF	5322 121 42492
C 6040	63V 10% 100NF	5322 121 42492
C 6041	63V 10% 100NF	5322 121 42492
C 6042	63V 10% 100NF	5322 121 42492
C 6043	63V 10% 100NF	5322 121 42492
C 6044	63V 10% 100NF	5322 121 42492
C 6045	63V 10% 100NF	5322 121 42492
C 6046	63V 10% 100NF	5322 121 42492
C 6047	63V 10% 100NF	5322 121 42492
C 6048	63V 10% 100NF	5322 121 42492
C 6049	-20+50% 10NF	4822 122 31414
C 6051	10% 1NF	4822 122 30027
C 6401	V 10% 22NF	5322 122 32654
C 6402	V 10% 22NF	5322 122 32654
C 6406	V 10% 22NF	5322 122 32654
C 6407	V 10% 22NF	5322 122 32654
C 6408	V 10% 22NF	5322 122 32654
C 6409	V 10% 22NF	5322 122 32654
C 6411	V 10% 22NF	5322 122 32654
C 6412	V 10% 22NF	5322 122 32654
C 6413	V 10% 22NF	5322 122 32654
C 6414	V 5% 47PF	5322 122 32452
C 6417	V 10% 39NF	5322 122 31849
C 6418	V 5% 47PF	5322 122 32452
C 6419	V 5% 47PF	5322 122 32452
C 6802	63V 2.5-5PF	5322 125 50305
C 6803	V 5% 33PF	5322 122 32659
C 6804	V 5% 18PF	5322 122 32965
C 6806	V 0.25PF 2.7PF	5322 122 31873
C 6807	V 10% 22NF	5322 122 32654
C 6808	V 10% 22NF	5322 122 32654
C 6812	V 10% 22NF	5322 122 32654
C 6813	V 10% 22NF	5322 122 32654
C 6816	V 5% 22PF	5322 122 32658
C 6817	63V 3.5-10PF	5322 125 50306
C 6818	V 10% 22NF	5322 122 32654
C 6819	V 5% 100PF	5322 122 32531
C 6821	V 10% 22NF	5322 122 32654
C 6822	V 10% 22NF	5322 122 32654
C 6823	V 10% 22NF	5322 122 32654
C 6824	-10+50% 68UF	4822 124 20689
C 6827	V 5% 100PF	5322 122 32531
C 6828	V 10% 1NF	5322 122 34123
C 6829	V 0.25PF 2.7PF	5322 122 31873
C 6833	V 10% 22NF	5322 122 32654
C 6834	-10+50% 68UF	4822 124 20689
C 6837	-10+50% 68UF	4822 124 20689
C 6839	V 10% 22NF	5322 122 32654
C 6841	-10+50% 68UF	4822 124 20689
C 6844	V 10% 100NF	4822 122 33104
C 6846	V 10% 22NF	5322 122 32654
C 6847	V 10% 22NF	5322 122 32654
C 6848	V 10% 22NF	5322 122 32654
C 6849	V 10% 22NF	5322 122 32654
C 6853	-10+50% 68UF	4822 124 20689
C 6901	400V 10% 22NF	5322 121 40308
C 6902	63V 10% 100NF	5322 121 42492
C 6903	63V 10% 100NF	5322 121 42492
C 6904	63V 10% 100NF	5322 121 42492
C 6906	2% 22PF	5322 122 32143
C 6907	2% 220PF	5322 122 32346
C 6908	10% 2.2NF	4822 122 30114
C 6912	63V 10% 100NF	5322 121 42492
C 6913	63V 10% 100NF	5322 121 42492
C 6914	63V 10% 100NF	5322 121 42492
C 6916	63V 10% 100NF	5322 121 42492
C 6917	63V 10% 100NF	5322 121 42492

POSNR	DESCRIPTION	ORDERING CODE
C 6921	63V 10% 100NF	5322 121 42492
C 6922	-10+50% 68UF	4822 124 20689
C 6923	63V 10% 100NF	5322 121 42492
C 6924	63V 10% 100NF	5322 121 42492
C 6926	63V 10% 100NF	5322 121 42492
C 6927	63V 10% 100NF	5322 121 42492
C 6929	10% 1NF	4822 122 30027
C 7001	-20+50% 10NF	4822 122 31414
C 7002	-20+20% 68UF	5322 124 21955
C 7003	-20+20% 68UF	5322 124 21955
C 7004	-20+50% 10NF	4822 122 31414
C 7006	-20+50% 10NF	4822 122 31414
C 7007	-20+50% 10NF	4822 122 31414
C 7008	-20+50% 10NF	4822 122 31414
C 7009	-20+50% 10NF	4822 122 31414
C 7011	63V 10% 100NF	5322 121 42492
C 7012	-20+50% 10NF	4822 122 31414
C 7013	63V 10% 220NF	4822 121 42408
C 7014	63V 10% 220NF	4822 121 42408
C 7015	-20+20% 33UF	5322 124 21957
C 7016	63V 10% 220NF	4822 121 42408
C 7017	63V 10% 220NF	4822 121 42408
C 7019	-20+50% 10NF	4822 122 31414
C 7021	63V 10% 220NF	4822 121 42408
C 7022	2% 150PF	4822 122 31413
C 7023	63V 10% 220NF	4822 121 42408
C 7024	10% 1.5NF	4822 122 31169
C 7026	10% 4.7NF	4822 122 31125
C 7027	10% 1NF	4822 122 30027
C 7028	2% 220PF	4822 122 30094
C 7029	2% 100PF	4822 122 31316
C 7031	-20+50% 10NF	4822 122 31414
C 7032	-20+50% 10NF	4822 122 31414
C 7033	-20+50% 10NF	4822 122 31414
C 7034	-20+50% 10NF	4822 122 31414
C 7036	-20+50% 10NF	4822 122 31414
C 7037	-20+50% 10NF	4822 122 31414
C 7038	-20+50% 10NF	4822 122 31414
C 7039	-20+50% 10NF	4822 122 31414
C 7041	-20+50% 10NF	4822 122 31414
C 7042	-10+50% 150UF	4822 124 20691
C 7043	-20+20% 6.8UF	5322 124 21763
C 7044	-20+50% 10NF	4822 122 31414
C 7046	-20+50% 10NF	4822 122 31414
C 7047	-20+50% 10NF	4822 122 31414
C 7048	-20+50% 10NF	4822 122 31414
C 7049	-20+50% 10NF	4822 122 31414
C 7051	-10+50% 150UF	4822 124 20691
C 7052	-20+50% 10NF	4822 122 31414
C 7053	-10+50% 150UF	4822 124 20691
C 7054	-20+50% 10NF	4822 122 31414
C 7056	-10+50% 220UF	4822 124 20681
C 7057	-20+20% 10UF	5322 124 21956
C 7058	-20+50% 10NF	4822 122 31414
C 7059	-10+50% 220UF	4822 124 20681
C 7061	-20+50% 10NF	4822 122 31414
C 7062	-10+50% 220UF	4822 124 20681
C 7063	-20+50% 10NF	4822 122 31414
C 7064	-10+50% 150UF	4822 124 20691
C 7066	-20+50% 10NF	4822 122 31414
C 7067	-20+50% 10NF	4822 122 31414
C 7068	-20+50% 10NF	4822 122 31414
C 7069	-20+50% 10NF	4822 122 31414
C 7070	-20+50% 10NF	4822 122 31414
C 7071	-10+50% 220UF	4822 124 20681
C 7072	-20+50% 10NF	4822 122 31414
C 7073	-20+20% 10UF	5322 124 21956
C 7074	-20+50% 10NF	4822 122 31414
C 7075	-20+50% 10NF	4822 122 31414
C 7076	-20+50% 10NF	4822 122 31414
C 7077	-20+50% 10NF	4822 122 31414
C 7078	-10+50% 220UF	4822 124 20681
C 7079	-20+50% 10NF	4822 122 31414
C 7081	-20+50% 10NF	4822 122 31414
C 7202	V 0.5PF 5.6PF	5322 122 32967
C 7205	0.25PF 5.6PF	5322 122 32163
C 7206	V 10% 2.7NF	4822 122 33498
C 7207	V 10% 2.7NF	4822 122 33498
C 7208	V 10% 22NF	5322 122 32654
C 7212	V 10% 22NF	5322 122 32654
C 7216	V 10% 22NF	5322 122 32654
C 7217	V 10% 22NF	5322 122 32654
C 7218	V 10% 22NF	5322 122 32654
C 7219	V 10% 22NF	5322 122 32654
C 7221	V 10% 22NF	5322 122 32654
C 7222	V 10% 22NF	5322 122 32654
C 7223	V 10% 22NF	5322 122 32654
C 7224	V 10% 22NF	5322 122 32654
C 7226	V 10% 22NF	5322 122 32654
C 7227	V 10% 22NF	5322 122 32654

POSNR	DESCRIPTION			ORDERING CODE
C 7229	V	10%	22NF	5322 122 32654
C 7231	V	10%	22NF	5322 122 32654
C 7252	V	5%	39PF	5322 122 32966
C 7256	V	10%	22NF	5322 122 32654
C 7257	V	10%	22NF	5322 122 32654
C 7258	V	5%	15PF	5322 122 32481
C 7259	V	10%	22NF	5322 122 32654
C 7261	V	10%	22NF	5322 122 32654
C 7262	V	5%	15PF	5322 122 32481
C 7263	V	10%	22NF	5322 122 32654
C 7264	V	10%	22NF	5322 122 32654
C 7266	V	10%	22NF	5322 122 32654
C 7267	V	10%	22NF	5322 122 32654
C 7268	V	10%	22NF	5322 122 32654
C 7269	V	10%	22NF	5322 122 32654
C 7271	V	10%	22NF	5322 122 32654
C 7272	V	10%	22NF	5322 122 32654
C 7273	V	10%	22NF	5322 122 32654
C 7274	V	10%	22NF	5322 122 32654
C 7276	V	10%	22NF	5322 122 32654
C 7277	V	10%	22NF	5322 122 32654
C 7278	V	10%	22NF	5322 122 32654
C 7279	V	10%	22NF	5322 122 32654
C 7281	V	10%	22NF	5322 122 32654
C 7282	V	10%	22NF	5322 122 32654
C 7283	V	10%	22NF	5322 122 32654
C 7284	V	10%	22NF	5322 122 32654
C 7351	V	10%	22NF	5322 122 32654
C 7352	V	10%	22NF	5322 122 32654
C 7353	V	10%	22NF	5322 122 32654
C 7354	V	10%	22NF	5322 122 32654
C 7355	V	5%	22PF	5322 122 32658
C 7356	V	10%	22NF	5322 122 32654
C 7357	V	10%	22NF	5322 122 32654
C 7358	V	10%	22NF	5322 122 32654
C 7359	V	10%	22NF	5322 122 32654
C 7361	V	10%	22NF	5322 122 32654
C 7362	V	10%	22NF	5322 122 32654
C 7402	V	5%	10PF	5322 122 32448
C 7404	V	10%	22NF	5322 122 32654
C 7406	V	10%	22NF	5322 122 32654
C 7407	V	10%	22NF	5322 122 32654
C 7408	V	5%	47PF	5322 122 32452
C 7409	V	10%	22NF	5322 122 32654
C 7411	V	10%	22NF	5322 122 32654
C 7412	V	10%	22NF	5322 122 32654
C 7413	V	10%	22NF	5322 122 32654
C 7414	V	10%	22NF	5322 122 32654
C 7416	V	10%	22NF	5322 122 32654
C 7417	V	10%	22NF	5322 122 32654
C 7418	V	10%	22NF	5322 122 32654
C 7419	V	10%	22NF	5322 122 32654
C 7421	V	10%	22NF	5322 122 32654
C 7422	V	10%	22NF	5322 122 32654
C 7451	63V	10%	100NF	5322 121 42492
C 7452	63V	10%	100NF	5322 121 42492
C 7453	63V	10%	100NF	5322 121 42492
C 7454	63V	10%	100NF	5322 121 42492
C 7456	-20+50%		10NF	4822 122 31414
C 7461	63V	10%	100NF	5322 121 42492
C 7462	63V	10%	100NF	5322 121 42492
C 7463	63V	10%	100NF	5322 121 42492
C 7464	63V	10%	100NF	5322 121 42492
C 7501	V	0.25PF	2.7PF	5322 122 31873
C 7502	-20+80%		22NF	4822 122 30103
C 7503	-20+80%		22NF	4822 122 30103
C 7505	0.25PF		4.7PF	4822 122 31822
C 7506	-20+80%		22NF	4822 122 30103
C 7507	-20+80%		22NF	4822 122 30103
C 7508	-20+80%		22NF	4822 122 30103
C 7509	-20+80%		22NF	4822 122 30103
C 7510	0.25PF		2.2PF	4822 122 31036
C 7511	-20+80%		22NF	4822 122 30103
C 7512	-20+20%		6.8UF	5322 124 21763
C 7513	-20+20%		6.8UF	5322 124 21763
C 7514	2%		100PF	4822 122 31316
C 7515	-20+80%		22NF	4822 122 30103
C 7516	-20+80%		22NF	4822 122 30103
C 7517	-20+80%		22NF	4822 122 30103
C 7518	-20+20%		6.8UF	5322 124 21763
C 7519	-20+20%		6.8UF	5322 124 21763
C 7521	2%		100PF	4822 122 31316
C 7522	V	10%	22NF	5322 122 32654
C 7701	V	0.25PF	2.7PF	5322 122 31873
C 7702	-20+80%		22NF	4822 122 30103
C 7703	-20+80%		22NF	4822 122 30103
C 7704	-20+80%		22NF	4822 122 30103
C 7705	0.25PF		4.7PF	4822 122 31822
C 7706	-20+80%		22NF	4822 122 30103
C 7708	-20+80%		22NF	4822 122 30103
C 7709	-20+80%		22NF	4822 122 30103

POSNR	DESCRIPTION			ORDERING CODE
C 7710	0.25PF		2.2PF	4822 122 31036
C 7711	-20+80%		22NF	4822 122 30103
C 7712	-20+20%		6.8UF	5322 124 21763
C 7713	-20+20%		6.8UF	5322 124 21763
C 7714	2%		100PF	4822 122 31316
C 7715	-20+80%		22NF	4822 122 30103
C 7716	-20+80%		22NF	4822 122 30103
C 7717	-20+80%		22NF	4822 122 30103
C 7718	-20+20%		6.8UF	5322 124 21763
C 7719	-20+20%		6.8UF	5322 124 21763
C 7721	2%		100PF	4822 122 31316
C 7722	V	10%	22NF	5322 122 32654
C 7801	V	10%	22NF	5322 122 32654
C 7802	V	10%	22NF	5322 122 32654
C 7803	V	10%	22NF	5322 122 32654
C 7804	V	10%	22NF	5322 122 32654
C 7806	V	10%	22NF	5322 122 32654
C 7807	V	10%	22NF	5322 122 32654
C 7808	V	10%	22NF	5322 122 32654
C 7809	V	10%	22NF	5322 122 32654
C 7811	V	10%	22NF	5322 122 32654
C 7812	V	10%	22NF	5322 122 32654
C 7813	V	10%	22NF	5322 122 32654
C 7814	V	10%	22NF	5322 122 32654
C 7816	V	10%	22NF	5322 122 32654
C 7817	V	10%	22NF	5322 122 32654
C 7818	V	10%	22NF	5322 122 32654
C 7819	V	10%	22NF	5322 122 32654
C 7821	V	0.25PF	2.7PF	5322 122 31873
C 7822	V	0.25PF	2.7PF	5322 122 31873
C 7823	V	10%	22NF	5322 122 32654
C 7824	V	10%	22NF	5322 122 32654
C 7826	16V	20%	10UF	5322 124 41622
C 7827	16V	20%	10UF	5322 124 41622
C 7828	V	10%	22NF	5322 122 32654
C 7829	V	10%	22NF	5322 122 32654
C 7831	V	10%	22NF	5322 122 32654
C 7832	V	10%	22NF	5322 122 32654
C 7833	V	10%	22NF	5322 122 32654
C 7834	V	10%	22NF	5322 122 32654
C 7836	V	10%	22NF	5322 122 32654
C 7837	V	10%	22NF	5322 122 32654
C 7838	V	10%	22NF	5322 122 32654
C 7839	V	10%	22NF	5322 122 32654
C 7841	V	10%	22NF	5322 122 32654
C 7842	V	10%	22NF	5322 122 32654
C 7843	16V	20%	10UF	5322 124 41622
C 7844	16V	20%	10UF	5322 124 41622
C 7846	V	0.25PF	2.7PF	5322 122 31873
C 7847	V	0.25PF	2.7PF	5322 122 31873
C 7848	V	10%	22NF	5322 122 32654
C 7849	V	10%	22NF	5322 122 32654
C 7851	-20+80%		22NF	4822 122 30103
C 7852	-20+80%		22NF	4822 122 30103
C 7853	-20+80%		22NF	4822 122 30103
C 7854	-20+80%		22NF	4822 122 30103
C 7856	-20+80%		22NF	4822 122 30103
C 7857	-10+50%		150UF	4822 124 20672
C 7858	-20+80%		22NF	4822 122 30103
C 7860	-20+80%		22NF	4822 122 30103
C 7861	-20+80%		22NF	4822 122 30103
C 7868	-20+20%		6.8UF	5322 124 21763
C 7869	-20+20%		6.8UF	5322 124 21763
C 7873	-20+20%		6.8UF	5322 124 21763
C 7874	-20+20%		6.8UF	5322 124 21763
C 7875	-20+80%		22NF	4822 122 30103
C 7878	-20+80%		22NF	4822 122 30103
C 7879	-20+80%		22NF	4822 122 30103
C 7880	-20+80%		22NF	4822 122 30103
C 7882	-20+80%		22NF	4822 122 30103
C 7884	-20+80%		22NF	4822 122 30103
C 7886	-20+80%		22NF	4822 122 30103
C 7887	-20+80%		22NF	4822 122 30103
C 7888	-20+20%		10UF	5322 124 21956
C 7902	V	10%	22NF	5322 122 32654
C 7903	V	10%	22NF	5322 122 32654
C 7906	V	10%	22NF	5322 122 32654
C 7907	V	10%	22NF	5322 122 32654
C 7922	16V	20%	10UF	5322 124 41622
C 7923	16V	20%	10UF	5322 124 41622
C 7924	V	5%	1NF	4822 122 31746
C 7927	16V	20%	10UF	5322 124 41622
C 7928	V	5%	1NF	4822 122 31746
C 7930	V	5%	1NF	4822 122 31746
C 7931	V	10%	22NF	5322 122 32654
C 7932	V	10%	22NF	5322 122 32654
C 7936	16V	20%	10UF	5322 124 41622
C 7938	16V	20%	10UF	5322 124 41622
C 8001	V	5%	820PF	5322 126 10184
C 8002	V	10%	22NF	5322 122 32654
C 8003	V	5%	820PF	5322 126 10184

POSNR	DESCRIPTION			ORDERING CODE
C 8004	V	10%	22NF	5322 122 32654
C 8005	V	0.5PF	8.2PF	5322 122 33244
C 8006	V	10%	22NF	5322 122 32654
C 8007	V	10%	39NF	5322 122 31849
C 8010	V	5%	100PF	5322 122 32531
C 8011	V	5%	820PF	5322 126 10184
C 8012	V	5%	22PF	5322 122 32658
C 8042	V	10%	22NF	5322 122 32654
C 8043	V	5%	820PF	5322 126 10184
C 8045	V	0.5PF	8.2PF	5322 122 33244
C 8046	V	10%	22NF	5322 122 32654
C 8047	V	10%	39NF	5322 122 31849
C 8048	V	10%	1.5NF	4822 122 33174
C 8049	V	10%	1.5NF	4822 122 33174
C 8050	V	5%	100PF	5322 122 32531
C 8052	V	5%	22PF	5322 122 32658
C 8061	V	10%	22NF	5322 122 32654
C 8062	V	10%	22NF	5322 122 32654
C 8063	V	10%	22NF	5322 122 32654
C 8064	V	10%	22NF	5322 122 32654
C 8066	V	10%	22NF	5322 122 32654
C 8067	V	10%	22NF	5322 122 32654
C 8068	V	10%	22NF	5322 122 32654
C 8069	V	10%	22NF	5322 122 32654
C 8071	V	10%	22NF	5322 122 32654
C 8072	V	10%	22NF	5322 122 32654
C 8073	V	10%	22NF	5322 122 32654
C 8074	V	10%	22NF	5322 122 32654
C 8076	V	10%	22NF	5322 122 32654
C 8077	V	10%	22NF	5322 122 32654
C 8078	V	10%	22NF	5322 122 32654
C 8079	V	10%	22NF	5322 122 32654
C 8081	V	10%	22NF	5322 122 32654
C 8082	V	10%	22NF	5322 122 32654
C 8083	V	10%	22NF	5322 122 32654
C 8084	V	10%	22NF	5322 122 32654
C 8086	V	10%	22NF	5322 122 32654
C 8087	V	10%	22NF	5322 122 32654
C 8088	V	10%	22NF	5322 122 32654
C 8089	V	10%	22NF	5322 122 32654
C 8091	V	10%	22NF	5322 122 32654
C 8092	V	10%	22NF	5322 122 32654
C 8093	V	10%	22NF	5322 122 32654
C 8094	V	10%	22NF	5322 122 32654
C 8096	V	10%	22NF	5322 122 32654
C 8097	V	10%	22NF	5322 122 32654
C 8098	V	10%	22NF	5322 122 32654
C 8099	V	10%	22NF	5322 122 32654
C 8102	V	10%	22NF	5322 122 32654
C 8106	V	10%	22NF	5322 122 32654
C 8122	16V	20%	10UF	5322 124 41622
C 8123	16V	20%	10UF	5322 124 41622
C 8124	V	5%	1NF	4822 122 31746
C 8127	16V	20%	10UF	5322 124 41622
C 8128	V	5%	1NF	4822 122 31746
C 8130	V	5%	1NF	4822 122 31746
C 8131	V	10%	22NF	5322 122 32654
C 8132	V	10%	22NF	5322 122 32654
C 8136	16V	20%	10UF	5322 124 41622
C 8138	16V	20%	10UF	5322 124 41622
C 8141	V	10%	22NF	5322 122 32654
C 8142	V	10%	22NF	5322 122 32654
C 8143	16V	20%	10UF	5322 124 41622
C 8144	16V	20%	10UF	5322 124 41622
C 8146	16V	20%	10UF	5322 124 41622
C 8147	V	0.25PF	3.9PF	5322 126 10185
C 8148	V	0.25PF	3.9PF	5322 126 10185
C 8149	V	0.25PF	3.9PF	5322 126 10185
C 8151	V	0.25PF	3.9PF	5322 126 10185
C 8152	V	10%	22NF	5322 122 32654
C 8153	V	10%	22NF	5322 122 32654
C 8154	V	10%	22NF	5322 122 32654
C 8156	V	10%	22NF	5322 122 32654
C 8157	V	10%	22NF	5322 122 32654
C 8158	V	10%	22NF	5322 122 32654
C 8159	V	10%	22NF	5322 122 32654
C 8161	V	10%	22NF	5322 122 32654
C 8162	V	10%	22NF	5322 122 32654
C 8163	V	10%	22NF	5322 122 32654
C 8164	V	10%	22NF	5322 122 32654
C 8166	V	10%	22NF	5322 122 32654
C 8167	V	10%	22NF	5322 122 32654
C 8168	V	10%	22NF	5322 122 32654
C 8169	V	10%	22NF	5322 122 32654
C 8171	V	10%	22NF	5322 122 32654
C 8172	V	10%	22NF	5322 122 32654
C 8173	V	10%	22NF	5322 122 32654
C 8174	V	10%	22NF	5322 122 32654
C 8176	16V	20%	10UF	5322 124 41622
C 8177	16V	20%	10UF	5322 124 41622
C 8178	16V	20%	10UF	5322 124 41622

POSNR	DESCRIPTION			ORDERING CODE
C 8179	16V	20%	10UF	5322 124 41622
C 8181	16V	20%	10UF	5322 124 41622
C 8182	16V	20%	10UF	5322 124 41622
C 8183	16V	20%	10UF	5322 124 41622
C 8184	16V	20%	10UF	5322 124 41622
C 8186	16V	20%	10UF	5322 124 41622
C 8187	16V	20%	10UF	5322 124 41622
C 8188	16V	20%	10UF	5322 124 41622
C 8201	V	5%	820PF	5322 126 10184
C 8202	V	10%	22NF	5322 122 32654
C 8203	V	5%	820PF	5322 126 10184
C 8204	V	10%	22NF	5322 122 32654
C 8205	V	0.5PF	8.2PF	5322 122 33244
C 8206	V	10%	22NF	5322 122 32654
C 8207	V	10%	39NF	5322 122 31849
C 8210	V	5%	100PF	5322 122 32531
C 8212	V	5%	22PF	5322 122 32658
C 8241	V	5%	820PF	5322 126 10184
C 8242	V	10%	22NF	5322 122 32654
C 8243	V	5%	820PF	5322 126 10184
C 8245	V	0.5PF	8.2PF	5322 122 33244
C 8246	V	10%	22NF	5322 122 32654
C 8247	V	10%	39NF	5322 122 31849
C 8250	V	5%	100PF	5322 122 32531
C 8252	V	5%	22PF	5322 122 32658
C 8261	V	10%	22NF	5322 122 32654
C 8262	V	10%	22NF	5322 122 32654
C 8263	V	10%	22NF	5322 122 32654
C 8264	V	10%	22NF	5322 122 32654
C 8301	V	10%	22NF	5322 122 32654
C 8302	V	5%	470PF	5322 122 32268
C 8303	V	5%	470PF	5322 122 32268
C 8304	V	5%	470PF	5322 122 32268
C 8306	V	5%	470PF	5322 122 32268
C 8307	V	5%	470PF	5322 122 32268
C 8308	V	5%	470PF	5322 122 32268
C 8309	V	10%	22NF	5322 122 32654
C 8311	V	5%	1NF	4822 122 31746
C 8312	16V	20%	10UF	5322 124 41622
C 8313	V	0.25PF	1PF	5322 122 32447
C 8314	V	5%	100PF	5322 122 32531
C 8316	V	5%	100PF	5322 122 32531
C 8317	V	5%	10PF	5322 122 32448
C 8318	V	10%	22NF	5322 122 32654
C 8319	V	10%	22NF	5322 122 32654
C 8331	V	5%	1NF	4822 122 31746
C 8332	16V	20%	10UF	5322 124 41622
C 8333	V	0.25PF	1PF	5322 122 32447
C 8334	V	5%	100PF	5322 122 32531
C 8336	V	5%	100PF	5322 122 32531
C 8337	V	5%	10PF	5322 122 32448
C 8338	V	10%	22NF	5322 122 32654
C 8351	V	5%	1NF	4822 122 31746
C 8352	16V	20%	10UF	5322 124 41622
C 8353	V	0.25PF	1PF	5322 122 32447
C 8354	V	5%	100PF	5322 122 32531
C 8356	V	5%	100PF	5322 122 32531
C 8357	V	5%	10PF	5322 122 32448
C 8358	V	10%	22NF	5322 122 32654
C 8371	V	5%	1NF	4822 122 31746
C 8372	16V	20%	10UF	5322 124 41622
C 8373	V	0.25PF	1PF	5322 122 32447
C 8374	V	5%	100PF	5322 122 32531
C 8376	V	5%	100PF	5322 122 32531
C 8377	V	5%	10PF	5322 122 32448
C 8378	V	10%	22NF	5322 122 32654
C 8401	V	5%	10PF	5322 122 32448
C 8411	V	5%	100PF	5322 122 32531
C 8421		-20+80%	22NF	4822 122 30103
C 8422		-20+80%	22NF	4822 122 30103
C 8423		-20+80%	22NF	4822 122 30103
C 8424		-20+80%	22NF	4822 122 30103
C 8426		-20+80%	22NF	4822 122 30103
C 8427		-20+80%	22NF	4822 122 30103
C 8428		-20+80%	22NF	4822 122 30103
C 8429		-20+80%	22NF	4822 122 30103
C 8431	V	10%	22NF	5322 122 32654
C 8432	V	10%	22NF	5322 122 32654
C 8439	V	10%	22NF	5322 122 32654
C 8501		2%	100PF	4822 122 31316
C 8502		2%	100PF	4822 122 31316
C 8503		-20+50%	10NF	4822 122 31414
C 8504		-20+50%	10NF	4822 122 31414
C 8506		10%	3.3NF	4822 122 30099
C 8507		0.25PF	4.7PF	4822 122 31822
C 8508		10%	3.3NF	4822 122 30099
C 8512		-20+50%	10NF	4822 122 31414
C 8513		-20+50%	10NF	4822 122 31414
C 8514		-20+50%	10NF	4822 122 31414
C 8516		-20+50%	10NF	4822 122 31414
C 8517		-20+50%	10NF	4822 122 31414

POSNR	DESCRIPTION	ORDERING CODE
C 8518	-10+50% 100UF	4822 124 20679
C 8519	-20+50% 10NF	4822 122 31414
C 8521	-20+50% 10NF	4822 122 31414
C 8522	2% 10PF	4822 122 32185
C 8523	-20+50% 10NF	4822 122 31414
C 8524	2% 33PF	5322 122 32072
C 8525	-20+50% 10NF	4822 122 31414
C 8526	-20+50% 10NF	4822 122 31414
C 8527	0.25PF 5.6PF	5322 122 32163
C 8528	0.25PF 0.56PF	5322 122 32107
C 8529	2% 22PF	5322 122 32143
C 8531	-20+50% 10NF	4822 122 31414
C 8532	2% 220PF	4822 122 30094
C 8533	-20+50% 10NF	4822 122 31414
C 8534	-20+50% 10NF	4822 122 31414
C 8537	-20+50% 10NF	4822 122 31414
C 8538	-20+50% 10NF	4822 122 31414
C 8539	-20+50% 10NF	4822 122 31414
C 8541	10% 1NF	4822 122 30027
C 8542	63V 10% 100NF	5322 121 42492
C 8543	63V 10% 100NF	5322 121 42492
C 8544	63V 10% 100NF	5322 121 42492
C 8546	63V 10% 100NF	5322 121 42492
C 8547	63V 10% 100NF	5322 121 42492
C 8548	100V 10% 10NF	4822 121 41857
C 8549	100V 10% 10NF	4822 121 41857
C 8551	100V 10% 10NF	4822 121 41857
C 8552	100V 10% 10NF	4822 121 41857
C 8553	-20+50% 10NF	4822 122 31414
C 8554	10% 680PF	4822 122 30053
C 8556	100V 10% 10NF	4822 121 41857
C 8557	100V 10% 10NF	4822 121 41857
C 8561	-10+50% 47UF	4822 124 20699
C 8562	-10+50% 100UF	4822 124 20679
C 8563	-10+50% 100UF	4822 124 20679
C 8564	-10+50% 100UF	4822 124 20679
C 8566	-10+50% 47UF	4822 124 20699
C 8567	-10+50% 47UF	4822 124 20699
C 8571	-20+50% 10NF	4822 122 31414
C 8572	-20+50% 10NF	4822 122 31414
C 8573	-20+50% 10NF	4822 122 31414
C 8574	-20+50% 10NF	4822 122 31414
C 8576	-20+50% 10NF	4822 122 31414
C 8577	-20+50% 10NF	4822 122 31414
C 8580	-20+50% 10NF	4822 122 31414
C 8701	V 0.25PF 1PF	5322 122 32447
C 8702	63V 2.5-5PF	5322 125 50305
C 8703	63V 3.5-10PF	5322 125 50306
C 8704	V 5% 15PF	5322 122 32481
C 8706	V 5% 100PF	5322 122 32531
C 8707	V 5% 820PF	5322 126 10184
C 8708	V 10% 22NF	5322 122 32654
C 8709	V 10% 22NF	5322 122 32654
C 8711	V 10% 22NF	5322 122 32654
C 8712	V 5% 820PF	5322 126 10184
C 8713	V 10% 22NF	5322 122 32654
C 8714	V 10% 22NF	5322 122 32654
C 8716	V 10% 22NF	5322 122 32654
C 8717	V 10% 22NF	5322 122 32654
C 8718	16V 20% 10UF	5322 124 41622
C 8719	16V 20% 10UF	5322 124 41622
C 8721	V 10% 22NF	5322 122 32654
C 8722	V 10% 22NF	5322 122 32654
C 8723	V 10% 22NF	5322 122 32654
C 8724	V 5% 1NF	4822 122 31746
C 9001	100V 10% 10NF	4822 121 41857
C 9002	100V 10% 10NF	4822 121 41857
C 9003	100V 10% 10NF	4822 121 41857
C 9007	100V 10% 10NF	4822 121 41857
C 9008	100V 10% 10NF	4822 121 41857
C 9009	100V 10% 10NF	4822 121 41857
C 9012	100V 10% 10NF	4822 121 41857
C 9013	100V 10% 10NF	4822 121 41857
C 9014	100V 10% 10NF	4822 121 41857
C 9021	100V 10% 10NF	4822 121 41857
C 9031	63V 10% 100NF	5322 121 42492
C 9032	63V 10% 100NF	5322 121 42492
C 9033	63V 10% 100NF	5322 121 42492
C 9034	63V 10% 100NF	5322 121 42492
C 9036	63V 10% 100NF	5322 121 42492
C 9039	100V 10% 10NF	4822 121 41857
C 9041	100V 10% 10NF	4822 121 41857
C 9042	100V 10% 10NF	4822 121 41857
C 9043	100V 10% 10NF	4822 121 41857
C 9044	100V 10% 10NF	4822 121 41857
C 9046	100V 10% 10NF	4822 121 41857
C 9201	V 10% 22NF	5322 122 32654
C 9202	V 10% 22NF	5322 122 32654
C 9203	V 10% 22NF	5322 122 32654
C 9204	V 10% 22NF	5322 122 32654
C 9206	V 10% 22NF	5322 122 32654

POSNR	DESCRIPTION	ORDERING CODE
C 9251	V 10% 22NF	5322 122 32654
C 9252	V 10% 10NF	5322 122 34098
C 9253	V 10% 10NF	5322 122 34098
C 9254	V 10% 10NF	5322 122 34098
C 9256	V 10% 10NF	5322 122 34098
C 9257	V 5% 68PF	5322 122 32269
C 9258	V 5% 68PF	5322 122 32269
C 9259	V 5% 22PF	5322 122 32658
C 9261	V 10% 22NF	5322 122 32654
C 9262	V 10% 22NF	5322 122 32654
C 9263	V 10% 10NF	5322 122 34098
C 9264	V 10% 10NF	5322 122 34098
C 9266	V 10% 22NF	5322 122 32654
C 9267	V 10% 22NF	5322 122 32654
C 9271	V 10% 22NF	5322 122 32654
C 9272	V 10% 22NF	5322 122 32654
C 9273	16V 20% 10UF	5322 124 41622
C 9274	V 10% 22NF	5322 122 32654
C 9276	16V 20% 10UF	5322 124 41622
C 9277	V 10% 22NF	5322 122 32654
C 9301	V 10% 22NF	5322 122 32654
C 9302	V 10% 10NF	5322 122 34098
C 9303	V 10% 10NF	5322 122 34098
C 9304	V 10% 10NF	5322 122 34098
C 9306	V 10% 10NF	5322 122 34098
C 9307	V 5% 68PF	5322 122 32269
C 9308	V 5% 68PF	5322 122 32269
C 9309	V 5% 22PF	5322 122 32658
C 9311	V 10% 22NF	5322 122 32654
C 9312	V 10% 22NF	5322 122 32654
C 9313	V 10% 10NF	5322 122 34098
C 9314	V 10% 10NF	5322 122 34098
C 9316	V 10% 22NF	5322 122 32654
C 9317	V 10% 22NF	5322 122 32654
C 9321	V 10% 22NF	5322 122 32654
C 9322	V 10% 22NF	5322 122 32654
C 9323	16V 20% 10UF	5322 124 41622
C 9324	V 10% 22NF	5322 122 32654
C 9326	16V 20% 10UF	5322 124 41622
C 9327	V 10% 22NF	5322 122 32654
C 9351	V 10% 22NF	5322 122 32654
C 9352	V 10% 10NF	5322 122 34098
C 9353	V 10% 10NF	5322 122 34098
C 9354	V 10% 10NF	5322 122 34098
C 9356	V 10% 10NF	5322 122 34098
C 9357	V 5% 68PF	5322 122 32269
C 9358	V 5% 68PF	5322 122 32269
C 9359	V 5% 22PF	5322 122 32658
C 9361	V 10% 22NF	5322 122 32654
C 9362	V 10% 22NF	5322 122 32654
C 9363	V 10% 22NF	5322 122 32654
C 9364	V 10% 22NF	5322 122 32654
C 9366	V 10% 22NF	5322 122 32654
C 9367	V 10% 22NF	5322 122 32654
C 9372	V 10% 22NF	5322 122 32654
C 9373	16V 20% 10UF	5322 124 41622
C 9374	V 10% 22NF	5322 122 32654
C 9376	16V 20% 10UF	5322 124 41622
C 9401	V 10% 22NF	5322 122 32654
C 9402	V 10% 22NF	5322 122 32654
C 9403	V 10% 22NF	5322 122 32654
C 9404	V 10% 22NF	5322 122 32654
C 9406	V 10% 22NF	5322 122 32654
C 9451	V 10% 22NF	5322 122 32654
C 9452	V 10% 10NF	5322 122 34098
C 9453	V 10% 10NF	5322 122 34098
C 9454	V 10% 10NF	5322 122 34098
C 9456	V 10% 10NF	5322 122 34098
C 9457	V 5% 68PF	5322 122 32269
C 9458	V 5% 68PF	5322 122 32269
C 9459	V 5% 22PF	5322 122 32658
C 9461	V 10% 22NF	5322 122 32654
C 9462	V 10% 22NF	5322 122 32654
C 9463	V 10% 10NF	5322 122 34098
C 9464	V 10% 10NF	5322 122 34098
C 9466	V 10% 22NF	5322 122 32654
C 9467	V 10% 22NF	5322 122 32654
C 9471	V 10% 22NF	5322 122 32654
C 9472	V 10% 22NF	5322 122 32654
C 9473	16V 20% 10UF	5322 124 41622
C 9474	V 10% 22NF	5322 122 32654
C 9476	16V 20% 10UF	5322 124 41622
C 9477	V 10% 22NF	5322 122 32654
C 9501	V 10% 22NF	5322 122 32654
C 9502	V 10% 10NF	5322 122 34098
C 9503	V 10% 10NF	5322 122 34098
C 9504	V 10% 10NF	5322 122 34098
C 9506	V 10% 10NF	5322 122 34098
C 9507	V 5% 68PF	5322 122 32269
C 9508	V 5% 68PF	5322 122 32269
C 9509	V 5% 22PF	5322 122 32658

POSNR	DESCRIPTION			ORDERING CODE
C 9511	V	10%	22NF	5322 122 32654
C 9512	V	10%	22NF	5322 122 32654
C 9513	V	10%	10NF	5322 122 34098
C 9514	V	10%	10NF	5322 122 34098
C 9516	V	10%	22NF	5322 122 32654
C 9517	V	10%	22NF	5322 122 32654
C 9521	V	10%	22NF	5322 122 32654
C 9522	V	10%	22NF	5322 122 32654
C 9523	16V	20%	10UF	5322 124 41622
C 9524	V	10%	22NF	5322 122 32654
C 9526	16V	20%	10UF	5322 124 41622
C 9527	V	10%	22NF	5322 122 32654
C 9551	V	10%	22NF	5322 122 32654
C 9552	V	10%	10NF	5322 122 34098
C 9553	V	10%	10NF	5322 122 34098
C 9554	V	10%	10NF	5322 122 34098
C 9556	V	10%	10NF	5322 122 34098
C 9557	V	5%	68PF	5322 122 32269
C 9558	V	5%	68PF	5322 122 32269
C 9559	V	5%	22PF	5322 122 32658
C 9561	V	10%	22NF	5322 122 32654
C 9562	V	10%	22NF	5322 122 32654
C 9563	V	10%	10NF	5322 122 34098
C 9564	V	10%	10NF	5322 122 34098
C 9566	V	10%	22NF	5322 122 32654
C 9567	V	10%	22NF	5322 122 32654
C 9572	V	10%	22NF	5322 122 32654
C 9573	16V	20%	10UF	5322 124 41622
C 9574	V	10%	22NF	5322 122 32654
C 9576	16V	20%	10UF	5322 124 41622
C 9601	16V	20%	10UF	5322 124 41622
C 9602	16V	20%	10UF	5322 124 41622
C 9603	V	10%	22NF	5322 122 32654
C 9604	V	10%	22NF	5322 122 32654
C 9606	V	10%	22NF	5322 122 32654
C 9607	V	10%	22NF	5322 122 32654
C 9608	V	10%	22NF	5322 122 32654
C 9609	V	10%	22NF	5322 122 32654

CHOKES

POSNR	DESCRIPTION		ORDERING CODE
I 5101	HEF4066BP	PEL	5322 209 10357
L 0019	KE 2X1.2MH 4A		5322 219 81131
L 0401	82UH		4822 158 10563
L 0402	82UH		4822 158 10563
L 0403	82UH		4822 158 10563
L 0404	82UH		4822 158 10563
L 0406	82UH		4822 158 10563
L 0407	82UH		4822 158 10563
L 0408	82UH		4822 158 10563
L 0409	82UH		4822 158 10563
L 0411	82UH		4822 158 10563
L 0412	82UH		4822 158 10563
L 0413	82UH		4822 158 10563
L 0414	82UH		4822 158 10563
L 0416	82UH		4822 158 10563
L 0417	82UH		4822 158 10563
L 0418	10UH	TDK	5322 157 53016
L 0419	82UH		4822 158 10563
L 0422	82UH		4822 158 10563
L 0423	1500UH	TDK	4822 156 21293
L 0424	1500UH	TDK	4822 156 21293
L 0426	1500UH	TDK	4822 156 21293
L 0427	1500UH	TDK	4822 156 21293
L 0431	1500UH	TDK	4822 156 21293
L 0432	1500UH	TDK	4822 156 21293
L 0436	82UH		4822 158 10563
L 0437	82UH		4822 158 10563
L 0438	82UH		4822 158 10563
L 0439	82UH		4822 158 10563
L 0441	82UH		4822 158 10563
L 0442	82UH		4822 158 10563
L 0443	1500UH	TDK	4822 156 21293
L 1201	2.0UH	TDK	4822 157 51757
L 1401	2.0UH	TDK	4822 157 51757
L 1701	2.0UH	TDK	4822 157 51757
L 1702	2.0UH	TDK	4822 157 51757
L 1703	2.0UH	TDK	4822 157 51757
L 1801	2.0UH	TDK	4822 157 51757
L 1802	2.0UH	TDK	4822 157 51757
L 1803	2.0UH	TDK	4822 157 51757
L 1804	2.0UH	TDK	4822 157 51757
L 1806	2.0UH	TDK	4822 157 51757
L 1807	2.0UH	TDK	4822 157 51757
L 1808	2.0UH	TDK	4822 157 51757

POSNR	DESCRIPTION		ORDERING CODE
L 4401	2X2,5MH 2,5A		5322 157 53346
L 4402	47UH	TDK	4822 152 10106
L 4403	47UH	TDK	4822 152 10106
L 4406	5.6UH		4822 157 52259
L 4408	L		5322 157 53376
L 4411	3.3UH	TDK	5322 157 53017
L 4412	3.3UH	TDK	5322 157 53017
L 4414	10UH	TDK	5322 157 52513
L 4416	22UH	TDK	5322 157 52707
L 4417	22UH	TDK	5322 157 52707
L 4418	22UH	TDK	5322 157 52707
L 4419	22UH	TDK	5322 157 52707
L 4421	10UH	TDK	5322 157 53016
L 4423	10UH	TDK	5322 157 53016
L 4424	82UH		4822 158 10563
L 4426	10UH	TDK	5322 157 53016
L 4601	470UH	TDK	5322 157 52514
L 4602	1500UH	TDK	5322 157 53018
L 4603	82UH		4822 158 10563
L 4604	1500UH	TDK	5322 157 53018
L 6003	2.0UH	TDK	4822 157 51757
L 6004	2.0UH	TDK	4822 157 51757
L 8501	82UH		4822 158 10563
L 8502	82UH		4822 158 10563
L 8503	82UH		4822 158 10563
L 8504	82UH		4822 158 10563
L 8506	82UH		4822 158 10563
L 8507	82UH		4822 158 10563
L 8509	0.15UH 10%	TDK	5322 157 53347
L 8511	0.15UH 10%	TDK	5322 157 53347
L 8512	0.22UH 10%	TDK	5322 157 53284
L 8701	1008CT 40NH		5322 157 60167

RESISTORS

POSNR	DESCRIPTION			ORDERING CODE
R 0001	CPP12	20%	47K	5322 101 20945
R 0002	CPP12	20%	47K	5322 101 20946
R 0003	CPP12	20%	47K	5322 101 20945
R 0004	CPP12	20%	47K	5322 101 20946
R 0005	CPP12	20%	47K	5322 101 20945
R 0401	MRS25	1%	1K	4822 116 53108
R 0402	MRS25	1%	1K	4822 116 53108
R 0403	MRS25	1%	1K	4822 116 53108
R 0404	MRS25	1%	1K	4822 116 53108
R 0406	MRS25	1%	1K	4822 116 53108
R 0407	MRS25	1%	1K	4822 116 53108
R 0408	NFR25	5%	1E	4822 111 30483
R 0409	MRS25	1%	1K	4822 116 53108
R 0411	MRS25	1%	511E	5322 116 53135
R 0412	-105-222		2K2	5322 111 90826
R 0413	MRS25	1%	1K	4822 116 53108
R 0414	MRS25	1%	1K	4822 116 53108
R 0417	MRS25	1%	1K	4822 116 53108
R 0418	MRS25	1%	1K	4822 116 53108
R 0419	MRS25	1%	1K	4822 116 53108
R 0421	MRS25	1%	1K	4822 116 53108
R 0422	MRS25	1%	681E	4822 116 53123
R 0423	MRS25	1%	681E	4822 116 53123
R 0424	MRS25	1%	681E	4822 116 53123
R 0426	MRS25	1%	681E	4822 116 53123
R 0427	MRS25	1%	1K	4822 116 53108
R 0428	MRS25	1%	1K	4822 116 53108
R 0429	MRS25	1%	1K	4822 116 53108
R 0431	-105-102		1K	5322 111 90463
R 0432	-105-102		1K	5322 111 90463
R 0433	-105-102		1K	5322 111 90463
R 0434	MRS25	1%	348E	5322 116 53591
R 0436	MRS25	1%	348E	5322 116 53591
R 0437	-105-332		3K3	5322 111 91353
R 0438	-105-332		3K3	5322 111 91353
R 0439	MRS25	1%	1K	4822 116 53108
R 0441	MRS25	1%	1K	4822 116 53108
R 0442	NFR25	5%	1E	4822 111 30483
R 0443	NFR25	5%	1E	4822 111 30483
R 0444	NFR25	5%	1E	4822 111 30483
R 0446	NFR25	5%	1E	4822 111 30483
R 0447	NFR25	5%	1E	4822 111 30483
R 0448	NFR25	5%	1E	4822 111 30483
R 0449	NFR25	5%	1E	4822 111 30483
R 0451	NFR25	5%	1E	4822 111 30483
R 0452	MRS25	1%	4E64	4822 116 52997
R 0453	MRS25	1%	10E	4822 116 52891
R 0454	MRS25	1%	10E	4822 116 52891
R 0456	MRS25	1%	10E	4822 116 52891
R 0457	MRS25	1%	121E	4822 116 52955

POSNR	DESCRIPTION	ORDERING CODE
R 0458	MRS25 1% 215K	5322 116 53425
R 0459	MRS25 1% 23K7	5322 116 53537
R 0460	MRS25 1% 2K37	5322 116 53536
R 0461	MRS25 1% 1K	4822 116 53108
R 0462	0.3W 25% 1K	5322 105 20041
R 0463	MRS25 1% 4K64	5322 116 53212
R 0464	MRS25 1% 1K	4822 116 53108
R 0468	MRS25 1% 10K	4822 116 53022
R 0469	MRS25 1% 10K	4822 116 53022
R 0471	MRS25 1% 10K	4822 116 53022
R 0472	MRS25 1% 10K	4822 116 53022
R 0473	MRS25 1% 10K	4822 116 53022
R 0476	MRS25 1% 5K11	5322 116 53494
R 0477	MRS25 1% 10K	4822 116 53022
R 0478	MRS25 1% 5K11	5322 116 53494
R 0479	MRS25 1% 10K	4822 116 53022
R 0481	MRS25 1% 110K	4822 116 52844
R 0482	MRS25 1% 121E	4822 116 52955
R 0483	MRS25 1% 121E	4822 116 52955
R 0484	MRS25 1% 121E	4822 116 52955
R 0486	MRS25 1% 121E	4822 116 52955
R 0487	MRS25 1% 121E	4822 116 52955
R 0488	MRS25 1% 3K16	4822 116 53021
R 0489	MRS25 1% 2K37	5322 116 53536
R 0491	MRS25 1% 3K16	4822 116 53021
R 0492	MRS25 1% 2K37	5322 116 53536
R 0493	MRS25 1% 100K	4822 116 52973
R 0494	MRS25 1% 100K	4822 116 52973
R 0496	MRS25 1% 2K61	5322 116 53327
R 0497	MRS25 1% 82E5	5322 116 53538
R 0498	MRS25 1% 619E	5322 116 53337
R 0499	MRS25 1% 121E	4822 116 52955
R 0501	-104 330E/470E	5322 111 90836
R 0502	-104 330E/470E	5322 111 90836
R 0502	MRS25 1% 19K6	5322 116 53258
R 0503	-104 330E/470E	5322 111 90836
R 0503	1/4W .25% 1K28	5322 116 80241
R 0504	-104 330E/470E	5322 111 90836
R 0504	1/4W .25% 10K	5322 116 80232
R 0506	-104 330E/470E	5322 111 90836
R 0506	1/4W .25% 10K	5322 116 80232
R 0507	-104 330E/470E	5322 111 90836
R 0508	-104 330E/470E	5322 111 90836
R 0511	MRS25 1% 422E	5322 116 53592
R 0512	MRS25 1% 2K61	5322 116 53327
R 0514	MRS25 1% 19K6	5322 116 53258
R 0516	1/4W .25% 1K28	5322 116 80241
R 0517	1/4W .25% 10K	5322 116 80232
R 0518	1/4W .25% 10K	5322 116 80232
R 0519	MRS25 1% 82E5	5322 116 53538
R 0521	MRS25 1% 619E	5322 116 53337
R 0527	MRS25 1% 422E	5322 116 53592
R 0528	MRS25 1% 100K	4822 116 52973
R 0529	MRS25 1% 100K	4822 116 52973
R 0531	MRS25 1% 2K61	5322 116 53327
R 0533	MRS25 1% 19K6	5322 116 53258
R 0534	1/4W .25% 1K28	5322 116 80241
R 0536	1/4W .25% 10K	5322 116 80232
R 0537	1/4W .25% 10K	5322 116 80232
R 0538	MRS25 1% 82E5	5322 116 53538
R 0539	MRS25 1% 619E	5322 116 53337
R 0546	MRS25 1% 2K15	5322 116 53239
R 0547	MRS25 1% 2K61	5322 116 53327
R 0551	1/4W .25% 1K28	5322 116 80241
R 0553	MRS25 1% 82E5	5322 116 53538
R 0554	MRS25 1% 619E	5322 116 53337
R 0557	MRS25 1% 100E	5322 116 53126
R 0558	MRS25 1% 10E	4822 116 52891
R 0559	MRS25 1% 1K	4822 116 53108
R 0568	MRS25 1% 51E1	5322 116 53213
R 0569	MRS25 1% 1K	4822 116 53108
R 0571	MRS25 1% 1K	4822 116 53108
R 0572	MRS25 1% 1K	4822 116 53108
R 0577	MRS25 1% 1K	4822 116 53108
R 0602	MRS25 1% 10K	4822 116 53022
R 0603	MRS25 1% 51E1	5322 116 53213
R 0604	MRS25 1% 51E1	5322 116 53213
R 0606	MRS25 1% 51E1	5322 116 53213
R 0607	MRS25 1% 10K	4822 116 53022
R 0608	MRS25 1% 51E1	5322 116 53213
R 0609	MRS25 1% 51E1	5322 116 53213
R 0611	MRS25 1% 100E	5322 116 53126
R 0612	MRS25 1% 100E	5322 116 53126
R 0613	MRS25 1% 51E1	5322 116 53213
R 0614	MRS25 1% 51E1	5322 116 53213
R 0616	MRS25 1% 100E	5322 116 53126
R 0617	MRS25 1% 100E	5322 116 53126
R 0618	MRS25 1% 10E	4822 116 52891
R 0619	MRS25 1% 51E1	5322 116 53213
R 0621	MRS25 1% 5K11	5322 116 53494
R 0622	MRS25 1% 10K	4822 116 53022

POSNR	DESCRIPTION	ORDERING CODE
R 0623	MRS25 1% 10K	4822 116 53022
R 0624	MRS25 1% 1K	4822 116 53108
R 0626	MRS25 1% 2K37	5322 116 53536
R 0627	MRS25 1% 51E1	5322 116 53213
R 0628	MRS25 1% 619E	5322 116 53337
R 0629	MRS25 1% 215E	5322 116 53325
R 0631	MRS25 1% 1K1	5322 116 53473
R 0632	MRS25 1% 51E1	5322 116 53213
R 0633	MRS25 1% 162E	5322 116 53523
R 0634	MRS25 1% 825E	5322 116 53541
R 0635	MRS25 1% 51E1	5322 116 53213
R 0636	MRS25 1% 5K11	5322 116 53494
R 0637	MRS25 1% 7K5	4822 116 53028
R 0638	MRS25 1% 5E11	4822 116 52999
R 0639	MRS25 1% 8K25	5322 116 53267
R 0640	MRS25 1% 51E1	5322 116 53213
R 0641	MRS25 1% 51E1	5322 116 53213
R 0642	MRS25 1% 1K47	5322 116 53185
R 0643	MRS25 1% 51E1	5322 116 53213
R 0644	MRS25 1% 511E	5322 116 53135
R 0646	MRS25 1% 196E	5322 116 53492
R 0647	MRS25 1% 51E1	5322 116 53213
R 0648	MRS25 1% 51E1	5322 116 53213
R 0649	MRS25 1% 619E	5322 116 53337
R 0651	MRS25 1% 619E	5322 116 53337
R 0652	MRS25 1% 100E	5322 116 53126
R 0653	MRS25 1% 100E	5322 116 53126
R 0654	MRS25 1% 100E	5322 116 53126
R 0657	MRS25 1% 10E	4822 116 52891
R 0658	MRS25 1% 121E	4822 116 52955
R 0659	MRS25 1% 100E	5322 116 53126
R 0661	NFR25 5% 1E	4822 111 30483
R 0662	NFR25 5% 1E	4822 111 30483
R 0663	NFR25 5% 1E	4822 111 30483
R 0664	NFR25 5% 1E	4822 111 30483
R 0666	NFR25 5% 1E	4822 111 30483
R 0667	NFR25 5% 1E	4822 111 30483
R 0668	MRS25 1% 10K	4822 116 53022
R 0669	MRS25 1% 10K	4822 116 53022
R 0671	MRS25 1% 10K	4822 116 53022
R 0672	MRS25 1% 10K	4822 116 53022
R 0673	MRS25 1% 10K	4822 116 53022
R 0674	MRS25 1% 1K	4822 116 53108
R 0676	MRS25 1% 1K	4822 116 53108
R 0677	MRS25 1% 5K11	5322 116 53494
R 0681	MRS25 1% 1K62	5322 116 53257
R 0682	MRS25 1% 6K81	5322 116 53252
R 0683	MRS25 1% 750E	5322 116 53265
R 0684	MRS25 1% 7K5	4822 116 53028
R 0686	MRS25 1% 237E	5322 116 53259
R 0687	MRS25 1% 1K47	5322 116 53185
R 0688	MRS25 1% 1K47	5322 116 53185
R 0689	MRS25 1% 261E	5322 116 53549
R 0691	MRS25 1% 14K7	4822 116 53531
R 0692	MRS25 1% 3K48	4822 116 53315
R 0693	MRS25 1% 3K48	4822 116 53315
R 0694	MRS25 1% 14K7	4822 116 53531
R 0696	MRS25 1% 7K5	4822 116 53028
R 0697	MRS25 1% 2K37	5322 116 53536
R 0698	MRS25 1% 1K21	4822 116 52956
R 0699	MRS25 1% 1K21	4822 116 52956
R 0701	MRS25 1% 237E	5322 116 53259
R 0702	MRS25 1% 348E	5322 116 53591
R 0703	MRS25 1% 237E	5322 116 53259
R 0704	MRS25 1% 5E11	4822 116 52999
R 0706	MRS25 1% 4K64	5322 116 53212
R 0707	MRS25 1% 23E7	5322 116 53606
R 0708	MRS25 1% 3K48	4822 116 53315
R 0709	MRS25 1% 750E	5322 116 53265
R 0711	MRS25 1% 237E	5322 116 53259
R 0712	MRS25 1% 2K87	5322 116 53513
R 0713	MRS25 1% 2K87	5322 116 53513
R 0714	MRS25 1% 1K21	4822 116 52956
R 0716	MRS25 1% 1K21	4822 116 52956
R 0717	MRS25 1% 23E7	5322 116 53606
R 0718	MRS25 1% 1K21	4822 116 52956
R 0719	MRS25 1% 1K21	4822 116 52956
R 0721	MTP10 20% 4K7	5322 101 14067
R 0722	MRS25 1% 5E11	4822 116 52999
R 0723	MRS25 1% 5K11	5322 116 53494
R 0724	MRS25 1% 10K	4822 116 53022
R 0726	MRS25 1% 2K15	5322 116 53239
R 0727	MRS25 1% 10K	4822 116 53022
R 0728	MRS25 1% 10K	4822 116 53022
R 0729	MRS25 1% 4K22	5322 116 53246
R 0751	MRS25 1% 46E4	5322 116 53248
R 1201	MRS25 1% 464E	5322 116 53232
R 1202	MRS25 1% 464E	5322 116 53232
R 1203	MRS25 1% 5K11	5322 116 53494
R 1204	MRS25 1% 5K11	5322 116 53494
R 1206	MRS25 1% 5K11	5322 116 53494

POSNR	DESCRIPTION		ORDERING CODE
R 1207	MRS25	1% 464E	5322 116 53232
R 1208	MRS25	1% 464E	5322 116 53232
R 1209	MRS25	1% 5K11	5322 116 53494
R 1211	MRS25	1% 464E	5322 116 53232
R 1212	MRS25	1% 464E	5322 116 53232
R 1213	MRS25	1% 464E	5322 116 53232
R 1214	MRS25	1% 51E1	5322 116 53213
R 1216	MRS25	1% 51E1	5322 116 53213
R 1217	MRS25	1% 51E1	5322 116 53213
R 1218	MRS25	1% 51E1	5322 116 53213
R 1219	MRS25	1% 51E1	5322 116 53213
R 1401	MRS25	1% 10K	4822 116 53022
R 1402	MRS25	1% 5K11	5322 116 53494
R 1403	MRS25	1% 5K11	5322 116 53494
R 1404	MRS25	1% 5K11	5322 116 53494
R 1406	MRS25	1% 464E	5322 116 53232
R 1407	MRS25	1% 464E	5322 116 53232
R 1408	MRS25	1% 464E	5322 116 53232
R 1409	MRS25	1% 464E	5322 116 53232
R 1411	MRS25	1% 1K	4822 116 53108
R 1412	MRS25	1% 10K	4822 116 53022
R 1413	MRS25	1% 1K	4822 116 53108
R 1414	MRS25	1% 1K	4822 116 53108
R 1416	MRS25	1% 75E	5322 116 53339
R 1701	-105-472	4K7	5322 111 90474
R 1702	MRS25	1% 464K	5322 116 53247
R 1703	MRS25	1% 10K	4822 116 53022
R 1704	MRS25	1% 100K	4822 116 52973
R 1706	MRS25	1% 10K	4822 116 53022
R 1707	MRS25	1% 5K11	5322 116 53494
R 1708	MRS25	1% 5K11	5322 116 53494
R 1709	MRS25	1% 511E	5322 116 53135
R 1711	MRS25	1% 10K	4822 116 53022
R 1712	MRS25	1% 2K15	5322 116 53239
R 1713	MRS25	1% 562E	5322 116 53214
R 1714	MRS25	1% 100E	5322 116 53126
R 1716	MRS25	1% 10K	4822 116 53022
R 1717	MRS25	1% 100E	5322 116 53126
R 1718	MRS25	1% 562E	5322 116 53214
R 1719	MRS25	1% 147E	5322 116 53569
R 1722	-105-472	4K7	5322 111 90474
R 1723	-105-472	4K7	5322 111 90474
R 1724	-105-472	4K7	5322 111 90474
R 1726	-105-222	2K2	5322 111 90826
R 1727	MRS25	1% 10K	4822 116 53022
R 1728	MRS25	1% 511E	5322 116 53135
R 1731	MRS25	1% 511E	5322 116 53135
R 1732	MRS25	1% 511E	5322 116 53135
R 1733	MRS25	1% 511E	5322 116 53135
R 1741	MRS25	1% 562E	5322 116 53214
R 1742	MRS25	1% 909E	4822 116 53533
R 1743	MRS25	1% 562E	5322 116 53214
R 1744	MRS25	1% 909E	4822 116 53533
R 1746	MRS25	1% 562E	5322 116 53214
R 1747	MRS25	1% 909E	4822 116 53533
R 1772	NFR25	5% 1E	4822 111 30483
R 1773	NFR25	5% 1E	4822 111 30483
R 1779	MRS25	1% 10K	4822 116 53022
R 1781	MRS25	1% 1K	4822 116 53108
R 1782	MRS25	1% 1K	4822 116 53108
R 1783	MRS25	1% 1K	4822 116 53108
R 1791	MRS25	1% 10K	4822 116 53022
R 1792	MRS25	1% 1K	4822 116 53108
R 1801	MRS25	1% 511E	5322 116 53135
R 1802	MRS25	1% 1K	4822 116 53108
R 1804	MRS25	1% 464E	5322 116 53232
R 1806	MRS25	1% 464E	5322 116 53232
R 1807	MRS25	1% 464E	5322 116 53232
R 1817	MRS25	1% 5K11	5322 116 53494
R 1818	MRS25	1% 5K11	5322 116 53494
R 1819	MRS25	1% 5K11	5322 116 53494
R 1821	MRS25	1% 5K11	5322 116 53494
R 1822	MRS25	1% 5K11	5322 116 53494
R 1823	MRS25	1% 1K	4822 116 53108
R 1824	MRS25	1% 1K	4822 116 53108
R 1826	MRS25	1% 121E	4822 116 52955
R 1827	MRS25	1% 121E	4822 116 52955
R 1828	MRS25	1% 121E	4822 116 52955
R 1829	MRS25	1% 121E	4822 116 52955
R 1831	MRS25	1% 121E	4822 116 52955
R 1832	MRS25	1% 121E	4822 116 52955
R 1833	MRS25	1% 121E	4822 116 52955
R 1834	MRS25	1% 121E	4822 116 52955
R 1836	MRS25	1% 121E	4822 116 52955
R 1837	MRS25	1% 121E	4822 116 52955
R 1838	MRS25	1% 10K	4822 116 53022
R 1839	MRS25	1% 1K	4822 116 53108
R 1841	MRS25	1% 10K	4822 116 53022
R 1842	MRS25	1% 511E	5322 116 53135
R 1843	MRS25	1% 1K96	5322 116 53237
R 1844	MRS25	1% 511E	5322 116 53135

POSNR	DESCRIPTION		ORDERING CODE
R 1845	MRS25	1% 100E	5322 116 53126
R 2001	MRS25	1% 10K	4822 116 53022
R 2002	MRS25	1% 10K	4822 116 53022
R 2003	MRS25	1% 511E	5322 116 53135
R 2004	MRS25	1% 511E	5322 116 53135
R 2006	MRS25	1% 511E	5322 116 53135
R 2007	MRS25	1% 10K	4822 116 53022
R 2008	MRS25	1% 10K	4822 116 53022
R 2009	MRS25	1% 10K	4822 116 53022
R 2011	MRS25	1% 10K	4822 116 53022
R 2012	MRS25	1% 1E	4822 116 52976
R 2013	MRS25	1% 1E	4822 116 52976
R 2014	MRS25	1% 10K	4822 116 53022
R 2016	MRS25	1% 511E	5322 116 53135
R 2017	MRS25	1% 10K	4822 116 53022
R 2018	MRS25	1% 511E	5322 116 53135
R 2019	NFR25	5% 1E	4822 111 30483
R 2021	NFR25	5% 1E	4822 111 30483
R 2022	NFR25	5% 1E	4822 111 30483
R 2023	NFR25	5% 1E	4822 111 30483
R 2024	NFR25	5% 1E	4822 111 30483
R 2026	MRS25	1% 511E	5322 116 53135
R 2027	MRS25	1% 1K	4822 116 53108
R 2028	MRS25	1% 1K	4822 116 53108
R 2029	MRS25	1% 1K	4822 116 53108
R 2031	MRS25	1% 1K	4822 116 53108
R 2032	MRS25	1% 10K	4822 116 53022
R 2033	MRS25	1% 10K	4822 116 53022
R 2034	MRS25	1% 1K	4822 116 53108
R 2036	MRS25	1% 10K	4822 116 53022
R 2037	MRS25	1% 10K	4822 116 53022
R 2038	MRS25	1% 1K	4822 116 53108
R 2101	MRS25	1% 10K	4822 116 53022
R 2102	MRS25	1% 10K	4822 116 53022
R 2103	MRS25	1% 511E	5322 116 53135
R 2104	MRS25	1% 511E	5322 116 53135
R 2106	MRS25	1% 511E	5322 116 53135
R 2107	MRS25	1% 10K	4822 116 53022
R 2108	MRS25	1% 10K	4822 116 53022
R 2109	MRS25	1% 511E	5322 116 53135
R 2111	MRS25	1% 511E	5322 116 53135
R 2112	MRS25	1% 511E	5322 116 53135
R 2113	MRS25	1% 511E	5322 116 53135
R 2114	MRS25	1% 5K11	5322 116 53494
R 2116	MRS25	1% 5K11	5322 116 53494
R 2117	MRS25	1% 21K5	5322 116 53241
R 2118	MRS25	1% 10K	4822 116 53022
R 2119	MRS25	1% 10K	4822 116 53022
R 2120	MRS25	1% 10K	4822 116 53022
R 2121	MRS25	1% 511E	5322 116 53135
R 2123	MRS25	1% 10K	4822 116 53022
R 2124	MRS25	1% 5K11	5322 116 53494
R 2126	MRS25	1% 10K	4822 116 53022
R 2127	MRS25	1% 10K	4822 116 53022
R 2128	MRS25	1% 511E	5322 116 53135
R 2129	MRS25	1% 10K	4822 116 53022
R 2131	MRS25	1% 10K	4822 116 53022
R 2132	MRS25	1% 10K	4822 116 53022
R 2133	MRS25	1% 1K	4822 116 53108
R 2134	NFR25	5% 1E	4822 111 30483
R 2136	NFR25	5% 1E	4822 111 30483
R 2137	NFR25	5% 1E	4822 111 30483
R 2138	NFR25	5% 1E	4822 111 30483
R 2139	NFR25	5% 1E	4822 111 30483
R 2141	NFR25	5% 1E	4822 111 30483
R 2142	MRS25	1% 1K	4822 116 53108
R 2301	MRS25	1% 10K	4822 116 53022
R 2302	MRS25	1% 10K	4822 116 53022
R 2303	MRS25	1% 511E	5322 116 53135
R 2304	MRS25	1% 511E	5322 116 53135
R 2305	MRS25	1% 100E	5322 116 53126
R 2306	MRS25	1% 511E	5322 116 53135
R 2307	MRS25	1% 511E	5322 116 53135
R 2308	MRS25	1% 511E	5322 116 53135
R 2309	MRS25	1% 511E	5322 116 53135
R 2310	MRS25	1% 100E	5322 116 53126
R 2311	MRS25	1% 10K	4822 116 53022
R 2312	MRS25	1% 10K	4822 116 53022
R 2313	MRS25	1% 511E	5322 116 53135
R 2314	MRS25	1% 511E	5322 116 53135
R 2316	MRS25	1% 5K11	5322 116 53494
R 2317	MRS25	1% 2K61	5322 116 53327
R 2318	MRS25	1% 2K37	5322 116 53536
R 2319	MRS25	1% 5K11	5322 116 53494
R 2321	MRS25	1% 2K61	5322 116 53327
R 2322	MRS25	1% 2K37	5322 116 53536
R 2323	MRS25	1% 5K11	5322 116 53494
R 2324	MRS25	1% 2K37	5322 116 53536
R 2326	MRS25	1% 2K61	5322 116 53327
R 2327	NFR25	5% 1E	4822 111 30483
R 2328	MRS25	1% 750E	5322 116 53265

POSNR	DESCRIPTION		ORDERING CODE
R 2329	MRS25	1% 750E	5322 116 53265
R 2331	NFR25	5% 1E	4822 111 30483
R 2332	NFR25	5% 1E	4822 111 30483
R 2333	MRS25	1% 7K5	4822 116 53028
R 2334	MTP10	20% 22K	5322 100 10118
R 2336	MRS25	1% 7K5	4822 116 53028
R 2337	MRS25	1% 100K	4822 116 52973
R 2338	MRS25	1% 562E	5322 116 53214
R 2339	MRS25	1% 1K	4822 116 53108
R 2341	MRS25	1% 1K	4822 116 53108
R 2342	MRS25	1% 562E	5322 116 53214
R 2343	MRS25	1% 562E	5322 116 53214
R 2344	MRS25	1% 562E	5322 116 53214
R 2346	MRS25	1% 215E	5322 116 53325
R 2349	MRS25	1% 215E	5322 116 53325
R 2351	MRS25	1% 2K61	5322 116 53327
R 2352	MRS25	1% 750E	5322 116 53265
R 2353	MRS25	1% 2K61	5322 116 53327
R 2354	MRS25	1% 750E	5322 116 53265
R 2356	MRS25	1% 261E	5322 116 53549
R 2357	MRS25	1% 511E	5322 116 53135
R 2366	MRS25	1% 261E	5322 116 53549
R 2367	MRS25	1% 511E	5322 116 53135
R 2368	MRS25	1% 1K78	5322 116 53208
R 2369	MRS25	1% 6K19	5322 116 53263
R 2374	MRS25	1% 3K48	4822 116 53315
R 2376	MRS25	1% 7K5	4822 116 53028
R 2377	MTP10	20% 22K	5322 100 10118
R 2378	MRS25	1% 7K5	4822 116 53028
R 2379	NFR25	5% 1E	4822 111 30483
R 2381	MRS25	1% 619E	5322 116 53337
R 2382	MRS25	1% 2K61	5322 116 53327
R 2383	MRS25	1% 2K61	5322 116 53327
R 2384	MRS25	1% 619E	5322 116 53337
R 2386	MRS25	1% 619E	5322 116 53337
R 2387	MRS25	1% 619E	5322 116 53337
R 2388	MRS25	1% 249E	5322 116 53573
R 2392	MRS25	1% 249E	5322 116 53573
R 2399	MRS25	1% 2K61	5322 116 53327
R 2401	MRS25	1% 750E	5322 116 53265
R 2402	MRS25	1% 2K61	5322 116 53327
R 2403	MRS25	1% 750E	5322 116 53265
R 2404	MRS25	1% 261E	5322 116 53549
R 2406	MRS25	1% 511E	5322 116 53135
R 2407	MRS25	1% 2K15	5322 116 53239
R 2408	MRS25	1% 464E	5322 116 53232
R 2409	MRS25	1% 110E	4822 116 52906
R 2411	MRS25	1% 2K15	5322 116 53239
R 2412	MRS25	1% 464E	5322 116 53232
R 2413	MRS25	1% 110E	4822 116 52906
R 2414	MRS25	1% 100K	4822 116 52973
R 2416	MRS25	1% 261E	5322 116 53549
R 2417	MRS25	1% 511E	5322 116 53135
R 2421	NFR25	5% 1E	4822 111 30483
R 2422	MRS25	1% 3E83	4822 116 52995
R 2424	NFR25	5% 1E	4822 111 30483
R 2426	MRS25	1% 562E	5322 116 53214
R 2451	NFR25	5% 1E	4822 111 30483
R 2452	NFR25	5% 1E	4822 111 30483
R 2453	NFR25	5% 1E	4822 111 30483
R 2454	NFR25	5% 1E	4822 111 30483
R 2456	NFR25	5% 1E	4822 111 30483
R 2500	MRS25	1% 10K	4822 116 53022
R 2502	MRS25	1% 1K	4822 116 53108
R 2503	MRS25	1% 100E	5322 116 53126
R 2504	MRS25	1% 3K83	4822 116 53079
R 2506	MRS25	1% 3K83	4822 116 53079
R 2507	MRS25	1% 3K83	4822 116 53079
R 2508	MRS25	1% 100E	5322 116 53126
R 2512	MRS25	1% 38K3	4822 116 53526
R 2513	MTP10	20% 47K	5322 101 14293
R 2514	MRS25	1% 38K3	4822 116 53526
R 2516	MTP10	20% 47K	5322 101 14293
R 2517	MRS25	1% 6K19	5322 116 53263
R 2518	MRS25	1% 100E	5322 116 53126
R 2519	MRS25	1% 100E	5322 116 53126
R 2521	MRS25	1% 287K	4822 116 53119
R 2522	MRS25	1% 287K	4822 116 53119
R 2523	MRS25	1% 42K2	5322 116 53431
R 2524	MRS25	1% 10K	4822 116 53022
R 2526	MRS25	1% 511E	5322 116 53135
R 2527	MRS25	1% 511E	5322 116 53135
R 2528	MRS25	1% 511E	5322 116 53135
R 2529	MRS25	1% 750E	5322 116 53265
R 2531	MTP10	20% 1K	5322 101 10294
R 2532	MRS25	1% 31K6	5322 116 53262
R 2533	MTP10	20% 1K	5322 101 10294
R 2534	MRS25	1% 1K62	5322 116 53257
R 2535	MRS25	1% 1K62	5322 116 53257
R 2536	MRS25	1% 1K78	5322 116 53208
R 2537	MRS25	1% 5K62	5322 116 53495

POSNR	DESCRIPTION		ORDERING CODE
R 2538	MRS25	1% 3K48	4822 116 53315
R 2539	MRS25	1% 196E	5322 116 53492
R 2541	MRS25	1% 5K62	5322 116 53495
R 2542	MRS25	1% 3K48	4822 116 53315
R 2543	MRS25	1% 196E	5322 116 53492
R 2544	MRS25	1% 5K62	5322 116 53495
R 2546	MRS25	1% 1M	4822 116 52843
R 2547	MRS25	1% 162K	5322 116 53535
R 2548	MRS25	1% 1M	4822 116 52843
R 2549	MRS25	1% 5K62	5322 116 53495
R 2550	MRS25	1% 422E	5322 116 53592
R 2551	MRS25	1% 422E	5322 116 53592
R 2552	MRS25	1% 100E	5322 116 53126
R 2553	MRS25	1% 100E	5322 116 53126
R 2554	MRS25	1% 5K62	5322 116 53495
R 2555	MRS25	1% 100E	5322 116 53126
R 2556	MRS25	1% 287K	4822 116 53119
R 2557	MRS25	1% 287K	4822 116 53119
R 2558	MRS25	1% 42K2	5322 116 53431
R 2559	MRS25	1% 12K1	4822 116 52957
R 2560	MRS25	1% 100E	5322 116 53126
R 2561	MRS25	1% 383E	5322 116 53332
R 2562	MRS25	1% 215E	5322 116 53325
R 2563	MRS25	1% 215E	5322 116 53325
R 2564	MRS25	1% 511E	5322 116 53135
R 2565	MRS25	1% 31K6	5322 116 53262
R 2566	MTP10	20% 1K	5322 101 10294
R 2567	MRS25	1% 196E	5322 116 53492
R 2568	MRS25	1% 196E	5322 116 53492
R 2569	MRS25	1% 31K6	5322 116 53262
R 2570	MRS25	1% 4K64	5322 116 53212
R 2571	MTP10	20% 4K7	5322 101 14067
R 2572	MRS25	1% 2K61	5322 116 53327
R 2573	MRS25	1% 10K	4822 116 53022
R 2574	MRS25	1% 1K	4822 116 53108
R 2576	MRS25	1% 12K1	4822 116 52957
R 2577	MRS25	1% 681E	4822 116 53123
R 2578	MRS25	1% 1K33	5322 116 53512
R 2579	MRS25	1% 12K1	4822 116 52957
R 2581	MRS25	1% 681E	4822 116 53123
R 2582	MRS25	1% 28K7	4822 116 53215
R 2583	MRS25	1% 1M	4822 116 52843
R 2584	MRS25	1% 64K9	5322 116 50514
R 2586	MRS25	1% 1M	4822 116 52843
R 2587	MRS25	1% 28K7	4822 116 53215
R 2588	MRS25	1% 422E	5322 116 53592
R 2589	MRS25	1% 422E	5322 116 53592
R 2590	MRS25	1% 100E	5322 116 53126
R 2591	MRS25	1% 5E11	4822 116 52999
R 2592	MRS25	1% 1E	4822 116 52976
R 2593	MRS25	1% 5E11	4822 116 52999
R 2594	MRS25	1% 1E	4822 116 52976
R 2595	MRS25	1% 100E	5322 116 53126
R 2596	MRS25	1% 1E	4822 116 52976
R 2597	MRS25	1% 1E	4822 116 52976
R 2598	MRS25	1% 1E	4822 116 52976
R 2599	MRS25	1% 5E11	4822 116 52999
R 2601	MRS25	1% 1M	4822 116 52843
R 2602	MRS25	1% 1M	4822 116 52843
R 2603	MRS25	1% 10K	4822 116 53022
R 2604	MRS25	1% 1M	4822 116 52843
R 2607	MRS25	1% 681K	5322 116 53593
R 2608	MRS25	1% 56K2	5322 116 53222
R 2609	MTP10	20% 10K	5322 101 14066
R 2611	MRS25	1% 4K22	5322 116 53246
R 2612	MRS25	1% 75K	5322 116 53266
R 2613	MRS25	1% 21K5	5322 116 53241
R 2614	MRS25	1% 90K9	5322 116 53582
R 2616	MRS25	1% 3K48	4822 116 53315
R 2617	MRS25	1% 287E	5322 116 53221
R 2621	MRS25	1% 2K15	5322 116 53239
R 2622	MRS25	1% 909E	4822 116 53533
R 2623	MRS25	1% 4K64	5322 116 53212
R 2624	MRS25	1% 2K87	5322 116 53513
R 2626	MRS25	1% 1K	4822 116 53108
R 2627	MRS25	1% 147E	5322 116 53569
R 2628	MRS25	1% 1K	4822 116 53108
R 2636	MRS25	1% 10K	4822 116 53022
R 2637	MTP10	20% 22K	5322 100 10118
R 2638	MRS25	1% 23K7	5322 116 53537
R 2639	MRS25	1% 3K48	4822 116 53315
R 2641	MRS25	1% 23K7	5322 116 53537
R 2642	MRS25	1% 750E	5322 116 53265
R 2643	MRS25	1% 100K	4822 116 52973
R 2644	MRS25	1% 2K15	5322 116 53239
R 2646	MRS25	1% 82E5	5322 116 53538
R 2647	MRS25	1% 1K33	5322 116 53512
R 2648	MRS25	1% 100E	5322 116 53126
R 2651	MRS25	1% 1K	4822 116 53108
R 2654	MRS25	1% 51K1	4822 116 53121
R 2655	MRS25	1% 56K2	5322 116 53222

POSNR	DESCRIPTION	ORDERING CODE
R 2657	MRS25 1% 56K2	5322 116 53222
R 2658	MTP10 20% 22K	5322 100 10118
R 2659	MTP10 20% 22K	5322 100 10118
R 2660	MRS25 1% 38K3	4822 116 53526
R 2661	MRS25 1% 38K3	4822 116 53526
R 2663	MRS25 1% 51K1	4822 116 53121
R 2666	MRS25 1% 1K	4822 116 53108
R 2671	MRS25 1% 1K	4822 116 53108
R 2674	MRS25 1% 147K	5322 116 53256
R 2677	MRS25 1% 196K	5322 116 53661
R 2678	MTP10 20% 47K	5322 101 14293
R 2679	MRS25 1% 90K9	5322 116 53582
R 2681	MRS25 1% 162K	5322 116 53535
R 2682	MTP10 20% 47K	5322 101 14293
R 2683	MRS25 1% 100K	4822 116 52973
R 2686	MRS25 1% 147K	5322 116 53256
R 2688	MRS25 1% 1K	4822 116 53108
R 2701	MRS25 1% 511E	5322 116 53135
R 2702	MRS25 1% 1K	4822 116 53108
R 2703	MTP10 20% 100E	5322 101 14072
R 2704	MRS25 1% 383E	5322 116 53332
R 2705	MRS25 1% 100K	4822 116 52973
R 2706	1/4W 0.1% 50E	5322 116 53165
R 2707	MRS25 1% 750E	5322 116 53265
R 2708	MRS25 1% 100K	4822 116 52973
R 2709	MRS25 1% 10K	4822 116 53022
R 2721	MRS25 1% 1M	4822 116 52843
R 2722	MRS25 1% 1M	4822 116 52843
R 2723	MRS25 1% 287K	4822 116 53119
R 2726	MRS25 1% 17K8	5322 116 53235
R 2727	MRS25 1% 17K8	5322 116 53235
R 2728	MTP10 20% 4K7	5322 101 14067
R 2729	MRS25 1% 13K3	5322 116 53489
R 2731	MRS25 1% 1M	4822 116 52843
R 2732	MRS25 1% 1M	4822 116 52843
R 2733	MRS25 1% 750K	5322 116 53727
R 2736	MRS25 1% 31K6	5322 116 53262
R 2737	MRS25 1% 31K6	5322 116 53262
R 2738	MTP10 20% 1K	5322 101 10294
R 2739	MRS25 1% 4K22	5322 116 53246
R 2741	MRS25 1% 316E	5322 116 53514
R 2742	MRS25 1% 21K5	5322 116 53241
R 2743	MRS25 1% 100K	4822 116 52973
R 2744	MRS25 1% 2K15	5322 116 53239
R 2746	MRS25 1% 1K	4822 116 53108
R 2748	MRS25 1% 10K	4822 116 53022
R 2749	MRS25 1% 10K	4822 116 53022
R 2751	MRS25 1% 2K15	5322 116 53239
R 2752	MRS25 1% 511E	5322 116 53135
R 2753	MRS25 1% 511E	5322 116 53135
R 2754	MRS25 1% 511E	5322 116 53135
R 2756	MRS25 1% 511E	5322 116 53135
R 2758	MRS25 1% 681E	4822 116 53123
R 2759	MRS25 1% 196E	5322 116 53492
R 2760	MRS25 1% 31K6	5322 116 53262
R 2801	MRS25 1% 10E	4822 116 52891
R 2802	MRS25 1% 511K	5322 116 53334
R 2803	MRS25 1% 21K5	5322 116 53241
R 2804	MRS25 1% 68K1	5322 116 53338
R 2806	MRS25 1% 237E	5322 116 53259
R 2807	MRS25 1% 100K	4822 116 52973
R 2808	MRS25 1% 1M	4822 116 52843
R 2809	MRS25 1% 1M	4822 116 52843
R 2811	MRS25 1% 31K6	5322 116 53262
R 2812	VR25 5% 10M	4822 110 72214
R 2813	MRS25 1% 511E	5322 116 53135
R 2814	MRS25 1% 1K	4822 116 53108
R 2816	MRS25 1% 68K1	5322 116 53338
R 2821	VR37 5% 3M3	4822 110 42201
R 2822	VR37 5% 4M7	4822 110 42205
R 2823	VR25 5% 2M2	4822 110 72196
R 2824	VR25 5% 2M2	4822 110 72196
R 2826	VR25 5% 2M2	4822 110 72196
R 2827	VR25 5% 2M2	4822 110 72196
R 2828	MRS25 1% 100E	5322 116 53126
R 2831	MRS25 1% 19K6	5322 116 53258
R 2832	MTP10 20% 10K	5322 101 14066
R 2833	MRS25 1% 100K	4822 116 52973
R 2834	MRS25 1% 100K	4822 116 52973
R 2836	MRS25 1% 1K	4822 116 53108
R 3001	NFR25 5% 1E	4822 111 30483
R 3002	MRS25 1% 383E	5322 116 53332
R 4001	MRS25 1% 110E	4822 116 52906
R 4002	MRS25 1% 110E	4822 116 52906
R 4003	MRS25 1% 110E	4822 116 52906
R 4004	MRS25 1% 110E	4822 116 52906
R 4006	MRS25 1% 110E	4822 116 52906
R 4007	MRS25 1% 110E	4822 116 52906
R 4008	MRS25 1% 110E	4822 116 52906
R 4009	MRS25 1% 110E	4822 116 52906
R 4011	MRS25 1% 110E	4822 116 52906

POSNR	DESCRIPTION	ORDERING CODE
R 4012	MRS25 1% 110E	4822 116 52906
R 4013	MRS25 1% 110E	4822 116 52906
R 4014	MRS25 1% 2K15	5322 116 53239
R 4016	MRS25 1% 2K15	5322 116 53239
R 4017	MRS25 1% 4E64	4822 116 52997
R 4018	MRS25 1% 1E	4822 116 52976
R 4019	MRS25 1% 1E	4822 116 52976
R 4021	-101-333 33K	5322 111 90881
R 4022	-101-333 33K	5322 111 90881
R 4023	-105-103 10K	5322 111 90473
R 4024	-105-103 10K	5322 111 90473
R 4026	-105-103 10K	5322 111 90473
R 4027	-105-103 10K	5322 111 90473
R 4028	-101-333 33K	5322 111 90881
R 4029	-101-333 33K	5322 111 90881
R 4201	MRS25 1% 1K47	5322 116 53185
R 4202	-105-103 10K	5322 111 90473
R 4203	MRS25 1% 1K96	5322 116 53237
R 4204	-105-102 1K	5322 111 90463
R 4206	MRS25 1% 287E	5322 116 53221
R 4207	MRS25 1% 287E	5322 116 53221
R 4208	MRS25 1% 287E	5322 116 53221
R 4209	MRS25 1% 287E	5322 116 53221
R 4211	MRS25 1% 287E	5322 116 53221
R 4212	MRS25 1% 287E	5322 116 53221
R 4213	MRS25 1% 287E	5322 116 53221
R 4214	MRS25 1% 287E	5322 116 53221
R 4216	MRS25 1% 287E	5322 116 53221
R 4217	MRS25 1% 287E	5322 116 53221
R 4218	MRS25 1% 287E	5322 116 53221
R 4219	MRS25 1% 287E	5322 116 53221
R 4221	MRS25 1% 287E	5322 116 53221
R 4222	-105-102 1K	5322 111 90463
R 4223	MRS25 1% 1E	4822 116 52976
R 4224	MRS25 1% 1E	4822 116 52976
R 4401	MRS25 1% 100K	4822 116 52973
R 4402	1.7A 20% 82E	4822 116 30069
R 4403	1.7A 20% 82E	4822 116 30069
R 4404	MRS25 1% 10E	4822 116 52891
R 4406	MRS25 1% 316K	4822 116 53058
R 4407	MRS25 1% 1M	4822 116 52843
R 4408	MRS25 1% 215K	5322 116 53425
R 4409	MRS25 1% 21K5	5322 116 53241
R 4411	MRS25 1% 34K8	5322 116 53429
R 4412	MRS25 1% 38K3	4822 116 53526
R 4413	MRS25 1% 26K1	5322 116 53261
R 4414	MRS25 1% 1M	4822 116 52843
R 4416	MRS25 1% 10K	4822 116 53022
R 4417	MRS25 1% 100K	4822 116 52973
R 4418	MRS25 1% 383K	5322 116 53576
R 4419	MRS25 1% 383K	5322 116 53576
R 4421	MRS25 1% 100K	4822 116 52973
R 4422	MRS25 1% 10K	4822 116 53022
R 4423	MRS25 1% 215K	5322 116 53425
R 4424	MRS25 1% 215K	5322 116 53425
R 4426	MRS25 1% 100E	5322 116 53126
R 4427	MRS25 1% 51K1	4822 116 53121
R 4428	MRS25 1% 51K1	4822 116 53121
R 4429	MRS25 1% 51K1	4822 116 53121
R 4431	MRS25 1% 51K1	4822 116 53121
R 4432	MRS25 1% 2E15	5322 116 53722
R 4434	MRS25 1% 215K	5322 116 53425
R 4436	MRS25 1% 215K	5322 116 53425
R 4437	MRS25 1% 100E	5322 116 53126
R 4438	MRS25 1% 464E	5322 116 53232
R 4439	MRS25 1% 10K	4822 116 53022
R 4440	MRS25 1% 21E5	5322 116 53426
R 4441	MRS25 1% 100E	5322 116 53126
R 4442	MRS25 1% 10K	4822 116 53022
R 4443	MRS25 1% 14K7	4822 116 53531
R 4444	0.5W 10% 1K5	4822 116 30248
R 4446	MRS25 1% 215E	5322 116 53325
R 4447	MRS25 1% 215E	5322 116 53325
R 4448	MRS25 1% 1E1	4822 116 52908
R 4449	MRS25 1% 1E1	4822 116 52908
R 4451	MRS25 1% 1E1	4822 116 52908
R 4452	MRS25 1% 1E1	4822 116 52908
R 4454	MRS25 1% 21K5	5322 116 53241
R 4456	MRS25 1% 1K	4822 116 53108
R 4459	MRS25 1% 10K	4822 116 53022
R 4461	MRS25 1% 100K	4822 116 52973
R 4462	MRS25 1% 1K	4822 116 53108
R 4463	MRS25 1% 4K64	5322 116 53212
R 4464	MRS25 1% 100K	4822 116 52973
R 4466	MRS25 1% 5K11	5322 116 53494
R 4467	MRS25 1% 1K	4822 116 53108
R 4468	MRS25 1% 100E	5322 116 53126
R 4469	70 DEG C	5322 116 40093
R 4471	MRS25 1% 1K	4822 116 53108
R 4472	1/4W .25% 14K	5322 116 53194
R 4473	MRS25 1% 560E	5322 116 53618

POSNR	DESCRIPTION	ORDERING CODE
R 4474	1/4W .25% 10K	5322 116 80232
R 4476	MRS25 1% 348E	5322 116 53591
R 4477	1/4W .25% 10K	5322 116 80232
R 4478	1/4W .25% 14K	5322 116 53194
R 4479	MRS25 1% 100K	4822 116 52973
R 4481	MRS25 1% 100E	5322 116 53126
R 4481	10% 4.7NF	4822 122 31125
R 4482	10% 1NF	4822 122 30027
R 4483	1/4W .25% 10K	5322 116 80232
R 4483	-20+50% 10NF	4822 122 31414
R 4484	1/4W .25% 4K48	5322 116 80237
R 4484	10% 1NF	4822 122 30027
R 4486	MRS25 1% 750E	5322 116 53265
R 4487	1/4W .25% 10K	5322 116 80232
R 4488	1/4W .25% 4K48	5322 116 80237
R 4489	MRS25 1% 750E	5322 116 53265
R 4491	MRS25 1% 8K25	5322 116 53267
R 4492	MRS25 1% 1K	4822 116 53108
R 4493	MRS25 1% 14E7	4822 116 53037
R 4494	MRS25 1% 1K	4822 116 53108
R 4496	MRS25 1% 10E	4822 116 52891
R 4497	MRS25 1% 511E	5322 116 53135
R 4498	MRS25 1% 21E5	5322 116 53426
R 4499	MRS25 1% 21E5	5322 116 53426
R 4601	MRS25 1% 1K47	5322 116 53185
R 4602	MRS25 1% 196K	5322 116 53661
R 4603	MRS25 1% 422E	5322 116 53592
R 4604	MRS25 1% 3K48	4822 116 53315
R 4606	MRS25 1% 26K1	5322 116 53261
R 4607	MTP10 20% 10K	5322 101 14066
R 4608	MRS25 1% 6K81	5322 116 53252
R 4609	1/4W 0.1% 147K	5322 116 80246
R 4611	VR37 1% 31M6	5322 116 64103
R 4612	MRS25 1% 681K	5322 116 53593
R 4613	MRS25 1% 16K2	5322 116 53589
R 4614	MRS25 1% 10K	4822 116 53022
R 4616	MRS25 1% 464E	5322 116 53232
R 4617	MRS25 1% 4K64	5322 116 53212
R 4618	MRS25 1% 46E4	5322 116 53248
R 4619	MRS25 1% 46K4	5322 116 53314
R 4621	MRS25 1% 215E	5322 116 53325
R 4622	MRS25 1% 4K64	5322 116 53212
R 4623	MRS25 1% 1E	4822 116 52976
R 4624	MRS25 1% 100E	5322 116 53126
R 4626	MRS25 1% 100E	5322 116 53126
R 4627	MRS25 1% 10K	4822 116 53022
R 4628	MRS25 1% 19K6	5322 116 53258
R 4629	MRS25 1% 19K6	5322 116 53258
R 4631	MRS25 1% 10K	4822 116 53022
R 4632	MRS25 1% 1M	4822 116 52843
R 4633	MRS25 1% 287K	4822 116 53119
R 4634	MRS25 1% 147K	5322 116 53256
R 4636	MRS25 1% 100K	4822 116 52973
R 4637	MRS25 1% 100E	5322 116 53126
R 4638	MRS25 1% 10K	4822 116 53022
R 4639	MRS25 1% 11K	4822 116 52907
R 4641	MRS25 1% 16K2	5322 116 53589
R 4643	MRS25 1% 2K87	5322 116 53513
R 4644	MRS25 1% 100K	4822 116 52973
R 4646	MRS25 1% 3K48	4822 116 53315
R 4647	MRS25 1% 28K7	4822 116 53215
R 4648	MRS25 1% 10K	4822 116 53022
R 4649	MRS25 1% 10K	4822 116 53022
R 4651	MRS25 1% 1K	4822 116 53108
R 4652	MRS25 1% 1K	4822 116 53108
R 4653	MRS25 1% 3K16	4822 116 53021
R 4654	MRS25 1% 750E	5322 116 53265
R 4656	0.5W 10% 3K3	5322 116 30234
R 4657	MRS25 1% 196E	5322 116 53492
R 4658	MRS25 1% 6K81	5322 116 53252
R 4659	MRS25 1% 2K15	5322 116 53239
R 4661	MRS25 1% 316E	5322 116 53514
R 4662	MRS25 1% 681E	4822 116 53123
R 4663	MRS25 1% 10E	4822 116 52891
R 4664	MRS25 1% 10E	4822 116 52891
R 4666	MRS25 1% 3K16	4822 116 53021
R 4667	VR68 5% 68M	5322 116 64035
R 4701	MCR18 1% 120E	4822 111 90339
R 4702	MCR18 1% 20E	4822 111 90352
R 4703	0,125W 5% 100M	5322 111 30376
R 4704	MCR18 1% 100E	5322 111 91134
R 4706	MCR18 1% 150E	5322 111 90098
R 4707	MCR18 1% 100K	4822 111 90214
R 4708	MCR18 1% 180E	5322 111 90242
R 4709	MCR18 1% 22E	4822 111 90186
R 4711	MCR18 1% 15E	4822 111 90344
R 4712	MCR18 1% 22E	4822 111 90186
R 4713	0,125W 5% 100M	5322 111 30376
R 4714	MCR18 1% 100E	5322 111 91134
R 4716	MCR18 1% 150E	5322 111 90098
R 4717	MCR18 1% 100K	4822 111 90214
R 5466	MCR18 1% 47E	4822 111 90217

POSNR	DESCRIPTION	ORDERING CODE
R 4718	MCR18 1% 47E	4822 111 90217
R 4719	MCR18 1% 100E	5322 111 91134
R 4721	MCR18 1% 820E	4822 111 90171
R 4722	MCR18 1% 100E	5322 111 91134
R 4723	MCR18 1% 270E	4822 111 90154
R 4724	MCR18 1% 220E	4822 111 90178
R 4726	MCR18 1% 1K	5322 111 90092
R 4727	MCR18 1% 100E	5322 111 91134
R 4728	MCR18 1% 1K2	5322 111 90096
R 4729	MCR18 1% 820E	4822 111 90171
R 4731	MCR18 1% 470E	5322 111 90109
R 4732	MCR18 1% 8K2	5322 111 90118
R 4733	MCR18 1% 1K	5322 111 90092
R 4734	MCR18 1% 2K7	4822 111 90569
R 4736	MCR18 1% 180E	5322 111 90242
R 4737	MCR18 1% 1K2	5322 111 90096
R 4738	MCR18 1% 680E	4822 111 90162
R 4739	MCR18 1% 10K	4822 111 90249
R 4741	MCR18 1% 47E	4822 111 90217
R 4742	MCR18 1% 2K7	4822 111 90569
R 4743	MCR18 1% 180E	5322 111 90242
R 4744	MCR18 1% 1K2	5322 111 90096
R 4746	MCR18 1% 680E	4822 111 90162
R 4747	MCR18 1% 10K	4822 111 90249
R 4748	MCR18 1% 47E	4822 111 90217
R 4749	MCR18 1% 270E	4822 111 90154
R 4750	MCR18 1% 560E	5322 111 90113
R 4751	0.3W 25% 100E	5322 105 20029
R 4752	MCR18 1% 560E	5322 111 90113
R 4753	0.3W 25% 100E	5322 105 20029
R 4754	MCR18 1% 56E	4822 111 90239
R 4755	MCR18 1% 56E	4822 111 90239
R 4756	MCR18 1% 270E	4822 111 90154
R 4757	MCR18 1% 56E	4822 111 90239
R 4758	MCR18 1% 33E	4822 111 90357
R 4759	MRS25 1% 215E	5322 116 53325
R 4760	MCR18 1% 56E	4822 111 90239
R 4761	MRS25 1% 866E	5322 116 53474
R 4762	MCR18 1% 10K	4822 111 90249
R 4763	MCR18 1% 27K	4822 111 90542
R 4764	MCR18 1% 27K	4822 111 90542
R 4766	MCR18 1% 82K	4822 111 90575
R 4767	MCR18 1% 27K	4822 111 90542
R 4768	MCR18 1% 82K	4822 111 90575
R 4769	MCR18 1% 27K	4822 111 90542
R 4771	MCR18 1% 10K	4822 111 90249
R 4772	MRS25 1% 100E	5322 116 53126
R 4773	MRS25 1% 10E	4822 116 52891
R 4774	MRS25 1% 10E	4822 116 52891
R 4776	MRS25 1% 100E	5322 116 53126
R 4777	0.4W 0.1% 1M	5322 116 51605
R 4778	MRS25 1% 2K87	5322 116 53513
R 4779	VR25 10% 22M	5322 116 51785
R 4781	MRS25 1% 10K	4822 116 53022
R 4782	MRS25 1% 10K	4822 116 53022
R 4783	1/4W 0.1% 196K	5322 116 52386
R 4784	1/4W 0.1% 23K7	5322 116 53169
R 4785	MRS25 1% 261K	5322 116 53609
R 4786	MRS25 1% 10K	4822 116 53022
R 4787	MRS25 1% 10K	4822 116 53022
R 4788	MRS25 1% 10K	4822 116 53022
R 4789	MRS25 1% 681K	5322 116 53593
R 4790	MRS25 1% 750K	5322 116 53727
R 4791	MRS25 1% 10K	4822 116 53022
R 4792	MRS25 1% 10K	4822 116 53022
R 4793	MRS25 1% 10K	4822 116 53022
R 4794	MRS25 1% 10E	4822 116 52891
R 4796	MRS25 1% 10E	4822 116 52891
R 4801	MCR18 1% 120E	4822 111 90339
R 4802	MCR18 1% 20E	4822 111 90352
R 4803	0,125W 5% 100M	5322 111 30376
R 4804	MCR18 1% 100E	5322 111 91134
R 4806	MCR18 1% 150E	5322 111 90098
R 4807	MCR18 1% 100K	4822 111 90214
R 4808	MCR18 1% 180E	5322 111 90242
R 4809	MCR18 1% 22E	4822 111 90186
R 4811	MCR18 1% 15E	4822 111 90344
R 4812	MCR18 1% 22E	4822 111 90186
R 4813	0,125W 5% 100M	5322 111 30376
R 4814	MCR18 1% 100E	5322 111 91134
R 4816	MCR18 1% 150E	5322 111 90098
R 4817	MCR18 1% 100K	4822 111 90214
R 4818	MCR18 1% 47E	4822 111 90217
R 4819	MCR18 1% 100E	5322 111 91134
R 4821	MCR18 1% 820E	4822 111 90171
R 4822	MCR18 1% 100E	5322 111 91134
R 4823	MCR18 1% 270E	4822 111 90154
R 4824	MCR18 1% 220E	4822 111 90178
R 4826	MCR18 1% 1K	5322 111 90092
R 4827	MCR18 1% 100E	5322 111 91134
R 4828	MCR18 1% 1K2	5322 111 90096
R 6456	MCR18 1% 100E	5322 111 91134
R 6457	MCR18 1% 100E	5322 111 91134

POSNR	DESCRIPTION	ORDERING CODE
R 4829	MCR18 1% 820E	4822 111 90171
R 4834	MCR18 1% 2K7	4822 111 90569
R 4836	MCR18 1% 180E	5322 111 90242
R 4837	MCR18 1% 1K2	5322 111 90096
R 4838	MCR18 1% 680E	4822 111 90162
R 4839	MCR18 1% 10K	4822 111 90249
R 4841	MCR18 1% 47E	4822 111 90217
R 4842	MCR18 1% 2K7	4822 111 90569
R 4843	MCR18 1% 180E	5322 111 90242
R 4844	MCR18 1% 1K2	5322 111 90096
R 4846	MCR18 1% 680E	4822 111 90162
R 4847	MCR18 1% 10K	4822 111 90249
R 4848	MCR18 1% 47E	4822 111 90217
R 4850	MCR18 1% 560E	5322 111 90113
R 4851	0.3W 25% 100E	5322 105 20029
R 4852	MCR18 1% 560E	5322 111 90113
R 4853	0.3W 25% 100E	5322 105 20029
R 4854	MCR18 1% 56E	4822 111 90239
R 4855	MCR18 1% 56E	4822 111 90239
R 4856	MCR18 1% 270E	4822 111 90154
R 4857	MCR18 1% 56E	4822 111 90239
R 4858	MCR18 1% 33E	4822 111 90357
R 4859	MRS25 1% 215E	5322 116 53325
R 4860	MCR18 1% 56E	4822 111 90239
R 4861	MRS25 1% 866E	5322 116 53474
R 4862	MCR18 1% 10K	4822 111 90249
R 4863	MCR18 1% 27K	4822 111 90542
R 4864	MCR18 1% 27K	4822 111 90542
R 4866	MCR18 1% 82K	4822 111 90575
R 4867	MCR18 1% 27K	4822 111 90542
R 4868	MCR18 1% 82K	4822 111 90575
R 4869	MCR18 1% 27K	4822 111 90542
R 4871	MCR18 1% 10K	4822 111 90249
R 4872	MRS25 1% 100E	5322 116 53126
R 4873	MRS25 1% 10E	4822 116 52891
R 4874	MRS25 1% 10E	4822 116 52891
R 4876	MRS25 1% 100E	5322 116 53126
R 4877	0.4W 0.1% 1M	5322 116 51605
R 4883	1/4W 0.1% 196K	5322 116 52386
R 4884	1/4W 0.1% 23K7	5322 116 53169
R 4885	MRS25 1% 261K	5322 116 53609
R 4886	MRS25 1% 10K	4822 116 53022
R 4887	MRS25 1% 10K	4822 116 53022
R 4888	MRS25 1% 10K	4822 116 53022
R 4894	MRS25 1% 10E	4822 116 52891
R 4896	MRS25 1% 10E	4822 116 52891
R 4897	MRS25 1% 1M	4822 116 52843
R 4898	MRS25 1% 110K	4822 116 52844
R 5001	MRS25 1% 2K87	5322 116 53513
R 5002	MRS25 1% 6K81	5322 116 53252
R 5003	MRS25 1% 26K1	5322 116 53261
R 5004	MRS25 1% 51E1	5322 116 53213
R 5005	MRS25 1% 3K83	4822 116 53079
R 5006	MRS25 1% 100E	5322 116 53126
R 5007	MRS25 1% 1K33	5322 116 53512
R 5008	MRS25 1% 4K22	5322 116 53246
R 5009	MRS25 1% 2K61	5322 116 53327
R 5010	MRS25 1% 681E	4822 116 53123
R 5011	MRS25 1% 1K	4822 116 53108
R 5012	MRS25 1% 1K78	5322 116 53208
R 5013	1/4W 0.1% 158E	5322 116 53172
R 5014	1/4W 0.1% 100E	5322 116 51701
R 5016	1/4W 0.1% 100E	5322 116 51701
R 5017	1/4W 0.1% 158E	5322 116 53172
R 5018	MRS25 1% 100E	5322 116 53126
R 5019	MRS25 1% 21K5	5322 116 53241
R 5020	MRS25 1% 51E1	5322 116 53213
R 5021	0.3W 25% 22K	5322 105 20035
R 5022	0.3W 25% 22K	5322 105 20035
R 5023	0.3W 25% 22K	5322 105 20035
R 5024	0.3W 25% 22K	5322 105 20035
R 5026	MRS25 1% 42K2	5322 116 53431
R 5027	MRS25 1% 42K2	5322 116 53431
R 5028	MRS25 1% 42K2	5322 116 53431
R 5029	MRS25 1% 3K48	4822 116 53315
R 5030	0.3W 25% 10K	4822 105 10455
R 5031	MRS25 1% 4K22	5322 116 53246
R 5032	MRS25 1% 1K47	5322 116 53185
R 5033	MRS25 1% 511E	5322 116 53135
R 5034	MRS25 1% 237E	5322 116 53259
R 5036	MRS25 1% 1K62	5322 116 53257
R 5038	MRS25 1% 10K	4822 116 53022
R 5039	MRS25 1% 100E	5322 116 53126
R 5041	MRS25 1% 10K	4822 116 53022
R 5042	MRS25 1% 121K	4822 116 52958
R 5043	MRS25 1% 1K62	5322 116 53257
R 5044	MRS25 1% 1K21	4822 116 52956
R 5045	MRS25 1% 100E	5322 116 53126
R 5046	0.3W 25% 2K2	5322 105 20033
R 5047	MRS25 1% 2K61	5322 116 53327
R 5048	MRS25 1% 3K16	4822 116 53021

POSNR	DESCRIPTION	ORDERING CODE
R 5049	MRS25 1% 10K	4822 116 53022
R 5051	MRS25 1% 1K47	5322 116 53185
R 5052	MRS25 1% 100E	5322 116 53126
R 5053	MRS25 1% 5K11	5322 116 53494
R 5054	MRS25 1% 5K11	5322 116 53494
R 5056	MRS25 1% 2K15	5322 116 53239
R 5057	MRS25 1% 2K15	5322 116 53239
R 5058	MRS25 1% 2K15	5322 116 53239
R 5061	MRS25 1% 100E	5322 116 53126
R 5062	MRS25 1% 100E	5322 116 53126
R 5063	MRS25 1% 100E	5322 116 53126
R 5064	MRS25 1% 100E	5322 116 53126
R 5066	MRS25 1% 100E	5322 116 53126
R 5101	MRS25 1% 2K87	5322 116 53513
R 5102	0.3W 25% 10K	4822 105 10455
R 5103	MRS25 1% 21K5	5322 116 53241
R 5104	MRS25 1% 51E1	5322 116 53213
R 5105	MRS25 1% 3K83	4822 116 53079
R 5106	MRS25 1% 100E	5322 116 53126
R 5107	MRS25 1% 1K33	5322 116 53512
R 5108	MRS25 1% 4K22	5322 116 53246
R 5109	MRS25 1% 2K61	5322 116 53327
R 5110	MRS25 1% 681E	4822 116 53123
R 5111	MRS25 1% 1K	4822 116 53108
R 5112	MRS25 1% 1K78	5322 116 53208
R 5113	1/4W 0.1% 158E	5322 116 53172
R 5114	1/4W 0.1% 100E	5322 116 51701
R 5116	1/4W 0.1% 100E	5322 116 51701
R 5117	1/4W 0.1% 158E	5322 116 53172
R 5118	MRS25 1% 100E	5322 116 53126
R 5119	MRS25 1% 21K5	5322 116 53241
R 5120	MRS25 1% 51E1	5322 116 53213
R 5121	0.3W 25% 22K	5322 105 20035
R 5122	0.3W 25% 22K	5322 105 20035
R 5123	0.3W 25% 22K	5322 105 20035
R 5124	0.3W 25% 22K	5322 105 20035
R 5126	MRS25 1% 42K2	5322 116 53431
R 5127	MRS25 1% 42K2	5322 116 53431
R 5128	MRS25 1% 42K2	5322 116 53431
R 5129	MRS25 1% 3K48	4822 116 53315
R 5130	0.3W 25% 10K	4822 105 10455
R 5131	MRS25 1% 4K22	5322 116 53246
R 5132	MRS25 1% 1K47	5322 116 53185
R 5133	MRS25 1% 511E	5322 116 53135
R 5134	MRS25 1% 237E	5322 116 53259
R 5136	MRS25 1% 1K62	5322 116 53257
R 5138	MRS25 1% 10K	4822 116 53022
R 5139	MRS25 1% 100E	5322 116 53126
R 5141	MRS25 1% 10K	4822 116 53022
R 5142	MRS25 1% 121K	4822 116 52958
R 5143	MRS25 1% 1K62	5322 116 53257
R 5144	MRS25 1% 1K21	4822 116 52956
R 5145	MRS25 1% 100E	5322 116 53126
R 5146	0.3W 25% 2K2	5322 105 20033
R 5147	MRS25 1% 2K61	5322 116 53327
R 5148	MRS25 1% 3K16	4822 116 53021
R 5149	MRS25 1% 10K	4822 116 53022
R 5151	MRS25 1% 1K47	5322 116 53185
R 5152	MRS25 1% 100E	5322 116 53126
R 5153	MRS25 1% 5K11	5322 116 53494
R 5154	MRS25 1% 5K11	5322 116 53494
R 5156	MRS25 1% 2K15	5322 116 53239
R 5157	MRS25 1% 2K15	5322 116 53239
R 5158	MRS25 1% 2K15	5322 116 53239
R 5161	MRS25 1% 100E	5322 116 53126
R 5162	MRS25 1% 100E	5322 116 53126
R 5163	MRS25 1% 100E	5322 116 53126
R 5164	MRS25 1% 100E	5322 116 53126
R 5166	MRS25 1% 100E	5322 116 53126
R 5201	1/4W .25% 16K2	5322 116 80231
R 5202	1/4W .25% 3K16	5322 116 80242
R 5203	MRS25 1% 95K3	5322 116 80291
R 5204	1/4W .25% 3K16	5322 116 80242
R 5206	MRS25 1% 16K2	5322 116 53589
R 5207	MRS25 1% 2K61	5322 116 53327
R 5208	MRS25 1% 2K61	5322 116 53327
R 5209	MRS25 1% 3K83	4822 116 53079
R 5211	MRS25 1% 3K83	4822 116 53079
R 5212	MRS25 1% 9K09	5322 116 53253
R 5213	MRS25 1% 619E	5322 116 53337
R 5214	MRS25 1% 825E	5322 116 53541
R 5216	MRS25 1% 215E	5322 116 53325
R 5217	MRS25 1% 681E	4822 116 53123
R 5218	MRS25 1% 46E4	5322 116 53248
R 5219	MRS25 1% 46E4	5322 116 53248
R 5221	MRS25 1% 46E4	5322 116 53248
R 5222	MRS25 1% 46E4	5322 116 53248
R 5223	MRS25 1% 46E4	5322 116 53248
R 5224	MRS25 1% 1K1	5322 116 53473
R 5226	MRS25 1% 75E	5322 116 53339
R 5227	MRS25 1% 75E	5322 116 53339

POSNR	DESCRIPTION	ORDERING CODE
R 5228	MRS25 1% 75E	5322 116 53339
R 5229	MRS25 1% 75E	5322 116 53339
R 5231	MRS25 1% 2K61	5322 116 53327
R 5232	MRS25 1% 46E4	5322 116 53248
R 5233	MRS25 1% 46E4	5322 116 53248
R 5234	MRS25 1% 46E4	5322 116 53248
R 5236	MRS25 1% 16K2	5322 116 53589
R 5237	MRS25 1% 95K3	5322 116 80291
R 5238	1/4W .25% 3K16	5322 116 80242
R 5242	1/4W .25% 16K2	5322 116 80231
R 5243	1/4W .25% 3K16	5322 116 80242
R 5244	MRS25 1% 681E	4822 116 53123
R 5246	MRS25 1% 215E	5322 116 53325
R 5247	MRS25 1% 825E	5322 116 53541
R 5248	MRS25 1% 619E	5322 116 53337
R 5271	MRS25 1% 2E15	5322 116 53722
R 5272	MRS25 1% 1E	4822 116 52976
R 5273	MRS25 1% 1E	4822 116 52976
R 5274	MRS25 1% 2E15	5322 116 53722
R 5276	MRS25 1% 2E15	5322 116 53722
R 5277	MRS25 1% 1E	4822 116 52976
R 5278	MRS25 1% 1E	4822 116 52976
R 5301	MCR18 1% 51E	5322 111 91352
R 5302	MCR18 1% 51E	5322 111 91352
R 5303	MCR18 1% 47E	4822 111 90217
R 5304	MCR18 1% 47E	4822 111 90217
R 5307	MCR18 1% 3K9	5322 111 91135
R 5308	MCR18 1% 2K2	4822 111 90248
R 5309	MCR18 1% 2K2	4822 111 90248
R 5311	MCR18 1% 3K9	5322 111 91135
R 5312	MCR18 1% 1K	5322 111 90092
R 5313	MCR18 1% 39E	4822 111 90361
R 5314	MCR18 1% 27K	4822 111 90542
R 5316	MCR18 1% 100E	5322 111 91134
R 5317	MCR18 1% 1K2	5322 111 90096
R 5318	MCR18 1% 100E	5322 111 91134
R 5319	MCR18 1% 100E	5322 111 91134
R 5320	MRS16T 1% 100E	4822 116 52757
R 5331	MCR18 1% 51E	5322 111 91352
R 5332	MCR18 1% 51E	5322 111 91352
R 5333	MCR18 1% 47E	4822 111 90217
R 5334	MCR18 1% 47E	4822 111 90217
R 5337	MCR18 1% 3K9	5322 111 91135
R 5338	MCR18 1% 2K2	4822 111 90248
R 5339	MCR18 1% 2K2	4822 111 90248
R 5341	MCR18 1% 3K9	5322 111 91135
R 5342	MCR18 1% 1K	5322 111 90092
R 5343	MCR18 1% 39E	4822 111 90361
R 5344	MCR18 1% 27K	4822 111 90542
R 5346	MCR18 1% 100E	5322 111 91134
R 5347	MCR18 1% 1K2	5322 111 90096
R 5348	MCR18 1% 100E	5322 111 91134
R 5349	MCR18 1% 100E	5322 111 91134
R 5350	MRS16T 1% 100E	4822 116 52757
R 5401	MCR18 1% 47E	4822 111 90217
R 5402	MCR18 1% 47E	4822 111 90217
R 5407	MCR18 1% 100E	5322 111 91134
R 5408	MCR18 1% 100E	5322 111 91134
R 5409	RC-01 5% 4E7	5322 111 90376
R 5411	RC-01 5% 4E7	5322 111 90376
R 5412	MCR18 1% 47E	4822 111 90217
R 5414	MCR18 1% 47E	4822 111 90217
R 5416	MCR18 1% 47E	4822 111 90217
R 5417	MCR18 1% 47E	4822 111 90217
R 5418	MCR18 1% 47E	4822 111 90217
R 5419	MCR18 1% 10K	4822 111 90249
R 5421	RC-01 5% 4E7	5322 111 90376
R 5422	RC-01 5% 4E7	5322 111 90376
R 5423	MCR18 1% 82E	4822 111 90124
R 5424	MCR18 1% 82E	4822 111 90124
R 5426	MCR18 1% 47E	4822 111 90217
R 5427	MCR18 1% 47E	4822 111 90217
R 5428	MCR18 1% 47E	4822 111 90217
R 5429	MCR18 1% 47E	4822 111 90217
R 5441	MCR18 1% 47E	4822 111 90217
R 5442	MCR18 1% 47E	4822 111 90217
R 5447	MCR18 1% 100E	5322 111 91134
R 5448	MCR18 1% 100E	5322 111 91134
R 5449	RC-01 5% 4E7	5322 111 90376
R 5451	RC-01 5% 4E7	5322 111 90376
R 5452	MCR18 1% 47E	4822 111 90217
R 5454	MCR18 1% 47E	4822 111 90217
R 5456	MCR18 1% 47E	4822 111 90217
R 5457	MCR18 1% 47E	4822 111 90217
R 5458	MCR18 1% 47E	4822 111 90217
R 5459	MCR18 1% 10K	4822 111 90249
R 5461	RC-01 5% 4E7	5322 111 90376
R 5462	RC-01 5% 4E7	5322 111 90376
R 5463	MCR18 1% 82E	4822 111 90124
R 5464	MCR18 1% 82E	4822 111 90124
R 5466	MCR18 1% 47E	4822 111 90217

POSNR	DESCRIPTION	ORDERING CODE
R 5467	MCR18 1% 47E	4822 111 90217
R 5468	MCR18 1% 47E	4822 111 90217
R 5469	MCR18 1% 47E	4822 111 90217
R 5471	MCR18 1% 47E	4822 111 90217
R 6001	NFR25 5% 1E	4822 111 30483
R 6002	NFR25 5% 1E	4822 111 30483
R 6006	MRS25 1% 5K11	5322 116 53494
R 6009	MRS25 1% 464E	5322 116 53232
R 6011	MRS25 1% 464E	5322 116 53232
R 6014	MRS25 1% 121E	4822 116 52955
R 6016	MRS25 1% 71E5	5322 116 53528
R 6017	MRS25 1% 31K6	5322 116 53262
R 6018	MRS25 1% 23K7	5322 116 53537
R 6019	MRS25 1% 1K	4822 116 53108
R 6021	MRS25 1% 909E	4822 116 53533
R 6022	MRS25 1% 51E1	5322 116 53213
R 6023	MRS25 1% 511E	5322 116 53135
R 6024	MRS25 1% 3K16	4822 116 53021
R 6026	MRS25 1% 1K33	5322 116 53512
R 6027	MRS25 1% 215E	5322 116 53325
R 6028	MRS25 1% 178E	5322 116 53572
R 6029	MRS25 1% 215E	5322 116 53325
R 6030	MRS25 1% 261E	5322 116 53549
R 6031	MRS25 1% 178E	5322 116 53572
R 6032	MRS25 1% 51E1	5322 116 53213
R 6033	MRS25 1% 1K96	5322 116 53237
R 6034	0.3W 25% 1K	5322 105 20032
R 6035	MRS25 1% 1K	4822 116 53108
R 6036	MRS25 1% 825E	5322 116 53541
R 6037	MRS25 1% 1K	4822 116 53108
R 6038	MRS25 1% 825E	5322 116 53541
R 6039	MRS25 1% 825E	5322 116 53541
R 6042	MRS25 1% 100K	4822 116 52973
R 6043	MRS25 1% 10K	4822 116 53022
R 6045	MRS25 1% 100E	5322 116 53126
R 6046	MRS25 1% 1K	4822 116 53108
R 6047	MRS25 1% 10K	4822 116 53022
R 6048	MRS25 1% 5K11	5322 116 53494
R 6049	MRS25 1% 5K11	5322 116 53494
R 6051	MRS25 1% 51E1	5322 116 53213
R 6052	MRS25 1% 51E1	5322 116 53213
R 6053	MRS25 1% 46E4	5322 116 53248
R 6054	MRS25 1% 46E4	5322 116 53248
R 6056	MRS25 1% 46E4	5322 116 53248
R 6057	MRS25 1% 46E4	5322 116 53248
R 6058	MRS25 1% 46E4	5322 116 53248
R 6059	MRS25 1% 46E4	5322 116 53248
R 6060	MRS25 1% 51E1	5322 116 53213
R 6061	MRS25 1% 10K	4822 116 53022
R 6401	MCR18 1% 100E	5322 111 91134
R 6403	MCR18 1% 100E	5322 111 91134
R 6406	MCR18 1% 100E	5322 111 91134
R 6407	MCR18 1% 100E	5322 111 91134
R 6408	MCR18 1% 2K7	4822 111 90569
R 6409	MCR18 1% 680E	4822 111 90162
R 6411	MCR18 1% 2K7	4822 111 90569
R 6412	MCR18 1% 680E	4822 111 90162
R 6413	MCR18 1% 100E	5322 111 91134
R 6414	MCR18 1% 100E	5322 111 91134
R 6416	MCR18 1% 100E	5322 111 91134
R 6417	MCR18 1% 100E	5322 111 91134
R 6418	MCR18 1% 100E	5322 111 91134
R 6419	MCR18 1% 100E	5322 111 91134
R 6421	MCR18 1% 100E	5322 111 91134
R 6422	MCR18 1% 100E	5322 111 91134
R 6423	MCR18 1% 100E	5322 111 91134
R 6424	MCR18 1% 100E	5322 111 91134
R 6426	MCR18 1% 51E	5322 111 91352
R 6427	MCR18 1% 51E	5322 111 91352
R 6428	MCR18 1% 2K7	4822 111 90569
R 6429	MCR18 1% 680E	4822 111 90162
R 6431	MCR18 1% 100E	5322 111 91134
R 6432	MCR18 1% 100E	5322 111 91134
R 6433	MCR18 1% 100E	5322 111 91134
R 6434	MCR18 1% 100E	5322 111 91134
R 6436	MCR18 1% 100E	5322 111 91134
R 6437	MCR18 1% 100E	5322 111 91134
R 6438	MCR18 1% 510E	4822 111 90245
R 6439	MCR18 1% 1K	5322 111 90092
R 6441	MCR18 1% 51E	5322 111 91352
R 6443	MCR18 1% 100E	5322 111 91134
R 6446	MCR18 1% 100E	5322 111 91134
R 6447	MCR18 1% 1K	5322 111 90092
R 6448	MCR18 1% 100E	5322 111 91134
R 6449	MCR18 1% 100E	5322 111 91134
R 6451	MCR18 1% 100E	5322 111 91134
R 6452	MCR18 1% 100E	5322 111 91134
R 6453	MCR18 1% 100E	5322 111 91134
R 6454	MCR18 1% 100E	5322 111 91134
R 6456	MCR18 1% 100E	5322 111 91134
R 6457	MCR18 1% 100E	5322 111 91134

POSNR	DESCRIPTION		ORDERING CODE
R 6458	MCR18	1% 100E	5322 111 91134
R 6459	MCR18	1% 10K	4822 111 90249
R 6461	MCR18	1% 15K	4822 111 90196
R 6462	MCR18	1% 680E	4822 111 90162
R 6463	MCR18	1% 680E	4822 111 90162
R 6464	MCR18	1% 680E	4822 111 90162
R 6466	MCR18	1% 2K7	4822 111 90569
R 6467	MCR18	1% 680E	4822 111 90162
R 6468	MCR18	1% 100E	5322 111 91134
R 6469	MCR18	1% 100E	5322 111 91134
R 6471	MCR18	1% 510E	4822 111 90245
R 6472	MCR18	1% 1K	5322 111 90092
R 6473	MCR18	1% 2K7	4822 111 90569
R 6474	MCR18	1% 120E	4822 111 90339
R 6476	MCR18	1% 120E	4822 111 90339
R 6477	MCR18	1% 51E	5322 111 91352
R 6478	MCR18	1% 51E	5322 111 91352
R 6479	MCR18	1% 51E	5322 111 91352
R 6501	MCR18	1% 10K	4822 111 90249
R 6502	MCR18	1% 15K	4822 111 90196
R 6503	MCR18	1% 100E	5322 111 91134
R 6504	MCR18	1% 100E	5322 111 91134
R 6506	MCR18	1% 510E	4822 111 90245
R 6507	MCR18	1% 510E	4822 111 90245
R 6508	MCR18	1% 1K	5322 111 90092
R 6509	MCR18	1% 100E	5322 111 91134
R 6511	MCR18	1% 100E	5322 111 91134
R 6512	MCR18	1% 100E	5322 111 91134
R 6513	MCR18	1% 100E	5322 111 91134
R 6514	MCR18	1% 100E	5322 111 91134
R 6516	MCR18	1% 100E	5322 111 91134
R 6517	MCR18	1% 100E	5322 111 91134
R 6518	MCR18	1% 100E	5322 111 91134
R 6519	MCR18	1% 100E	5322 111 91134
R 6521	MCR18	1% 1K	5322 111 90092
R 6522	MCR18	1% 1K	5322 111 90092
R 6523	MCR18	1% 510E	4822 111 90245
R 6524	MCR18	1% 100E	5322 111 91134
R 6526	MCR18	1% 100E	5322 111 91134
R 6527	MCR18	1% 2K7	4822 111 90569
R 6528	MCR18	1% 680E	4822 111 90162
R 6529	MCR18	1% 1K	5322 111 90092
R 6531	MCR18	1% 510E	4822 111 90245
R 6532	MCR18	1% 3K	5322 111 91351
R 6533	MCR18	1% 680E	4822 111 90162
R 6534	MCR18	1% 100E	5322 111 91134
R 6536	MCR18	1% 100E	5322 111 91134
R 6537	MCR18	1% 100E	5322 111 91134
R 6538	MCR18	1% 100E	5322 111 91134
R 6539	MCR18	1% 100E	5322 111 91134
R 6541	RC-01	5% 3E3	4822 111 90388
R 6542	RC-01	5% 3E3	4822 111 90388
R 6543	MCR18	1% 100E	5322 111 91134
R 6801	MCR18	1% 180E	5322 111 90242
R 6802	MCR18	1% 39E	4822 111 90361
R 6803	MCR18	1% 13E	4822 111 90343
R 6804	0,125W	5% 100M	5322 111 30376
R 6805	MCR18	1% 68K	4822 111 90202
R 6806	MCR18	1% 100E	5322 111 91134
R 6807	MCR18	1% 150E	5322 111 90098
R 6808	MCR18	1% 10K	4822 111 90249
R 6809	MCR18	1% 47E	4822 111 90217
R 6810	MCR18	1% 100E	5322 111 91134
R 6811	MCR18	1% 10K	4822 111 90249
R 6812	0,125W	5% 100M	5322 111 30376
R 6813	MCR18	1% 1K	5322 111 90092
R 6814	MCR18	1% 68K	4822 111 90202
R 6815	MCR18	1% 150E	5322 111 90098
R 6817	MCR18	1% 68E	4822 111 90203
R 6818	MCR18	1% 100E	5322 111 91134
R 6819	MCR18	1% 10K	4822 111 90249
R 6820	MCR18	1% 150E	5322 111 90098
R 6821	MCR18	1% 68K	4822 111 90202
R 6822	MCR18	1% 15E	4822 111 90344
R 6823	MCR18	1% 15E	4822 111 90344
R 6824	MCR18	1% 47E	4822 111 90217
R 6825	0,125W	5% 100M	5322 111 30376
R 6826	MCR18	1% 27K	4822 111 90542
R 6827	MCR18	1% 10K	4822 111 90249
R 6828	MCR18	1% 560E	5322 111 90113
R 6829	MCR18	1% 120E	4822 111 90339
R 6830	MCR18	1% 110E	4822 111 90335
R 6831	MCR18	1% 270E	4822 111 90154
R 6833	MCR18	1% 180E	5322 111 90242
R 6834	MCR18	1% 33E	4822 111 90357
R 6835	MCR18	1% 1K	5322 111 90092
R 6836	MCR18	1% 47E	4822 111 90217
R 6837	MCR18	1% 1K	5322 111 90092
R 6838	MCR18	1% 100E	5322 111 91134
R 6839	MCR18	1% 470E	5322 111 90109
R 6841	RC-01	5% 6E8	4822 111 90254

POSNR	DESCRIPTION		ORDERING CODE
R 6842	MCR18	1% 10K	4822 111 90249
R 6843	MCR18	1% 10K	4822 111 90249
R 6844	MCR18	1% 270E	4822 111 90154
R 6845	MCR18	1% 1K8	5322 111 90101
R 6846	MCR18	1% 3K9	5322 111 91135
R 6847	MCR18	1% 180E	5322 111 90242
R 6848	MCR18	1% 680E	4822 111 90162
R 6849	MCR18	1% 10E	5322 111 90095
R 6850		0.3W 25% 100E	5322 105 20029
R 6851	MCR18	1% 110E	4822 111 90335
R 6852	MCR18	1% 220E	4822 111 90178
R 6853	MCR18	1% 390E	5322 111 91205
R 6854		0.3W 25% 470E	5322 105 20028
R 6855	MCR18	1% 22E	4822 111 90186
R 6856	MCR18	1% 180E	5322 111 90242
R 6857	MCR18	1% 1K5	4822 111 90151
R 6858	MCR18	1% 2K2	4822 111 90248
R 6859	MCR18	1% 470E	5322 111 90109
R 6860	MCR18	1% 10K	4822 111 90249
R 6861	MCR18	1% 10K	4822 111 90249
R 6862	MCR18	1% 4K7	5322 111 90111
R 6863	MCR18	1% 33E	4822 111 90357
R 6864	MCR18	1% 270E	4822 111 90154
R 6865	MCR18	1% 33E	4822 111 90357
R 6866	MCR18	1% 33E	4822 111 90357
R 6867	MRS25	1% 162E	5322 116 53523
R 6868	MRS25	1% 536E	5322 116 53335
R 6869	MCR18	1% 330E	5322 111 90106
R 6870	MCR18	1% 10K	4822 111 90249
R 6871	MCR18	1% 4K7	5322 111 90111
R 6872	MCR18	1% 680E	4822 111 90162
R 6873	MCR18	1% 10K	4822 111 90249
R 6874	MCR18	1% 10K	4822 111 90249
R 6875	MCR18	1% 1K5	4822 111 90151
R 6876	MCR18	1% 120K	4822 111 90168
R 6877	MCR18	1% 68K	4822 111 90202
R 6878	MCR18	1% 10K	4822 111 90249
R 6879	MCR18	1% 15K	4822 111 90196
R 6880	MCR18	1% 1K5	4822 111 90151
R 6881	MCR18	1% 15K	4822 111 90196
R 6882	MCR18	1% 6K8	4822 111 90544
R 6883	MCR18	1% 100E	5322 111 91134
R 6884	MCR18	1% 1K	5322 111 90092
R 6885	MCR18	1% 68K	4822 111 90202
R 6886	MCR18	1% 220K	4822 111 90197
R 6887	MCR18	1% 3K3	4822 111 90157
R 6889	MCR18	1% 10K	4822 111 90249
R 6890	MCR18	1% 1K	5322 111 90092
R 6894	MCR18	1% 1K	5322 111 90092
R 6901	0.4W 0.1%	1M	5322 116 51605
R 6902	MRS25	1% 2K87	5322 116 53513
R 6903	MRS25	1% 1M	4822 116 52843
R 6904	MRS25	1% 100K	4822 116 52973
R 6905	MRS25	1% 10E	4822 116 52891
R 6906	MRS25	1% 100K	4822 116 52973
R 6907	VR25	10% 22M	5322 116 51785
R 6908	MRS25	1% 10K	4822 116 53022
R 6909	1/4W 0.1%	866K	5322 116 53174
R 6911	MRS25	1% 422E	5322 116 53592
R 6912	1/4W 0.1%	95K3	5322 116 80244
R 6913	1/4W 0.1%	8K66	5322 116 51778
R 6914	MRS25	1% 422K	5322 116 53577
R 6916	1/4W 0.1%	110K	5322 116 80245
R 6917	MRS25	1% 10K	4822 116 53022
R 6918	MRS25	1% 17K8	5322 116 53235
R 6919	MRS25	1% 100K	4822 116 52973
R 6920	1/4W 0.1%	1M	5322 116 80243
R 6921	MRS25	1% 100K	4822 116 52973
R 6922	1/4W 0.1%	10K	5322 116 51702
R 6923	MRS25	1% 100K	4822 116 52973
R 6924	MRS25	1% 10E	4822 116 52891
R 6926	MRS25	1% 100E	5322 116 53126
R 6927	MRS25	1% 750E	5322 116 53265
R 7001	1/4W .25%	475E	5322 116 80238
R 7002	1/4W .25%	475E	5322 116 80238
R 7003	MRS25	1% 46E4	5322 116 53248
R 7004	MRS25	1% 2K15	5322 116 53239
R 7006	MRS25	1% 100E	5322 116 53126
R 7007	MRS25	1% 46E4	5322 116 53248
R 7008	MRS25	1% 2K15	5322 116 53239
R 7009	MRS25	1% 2K15	5322 116 53239
R 7010	MRS25	1% 4K64	5322 116 53212
R 7011	MRS25	1% 237E	5322 116 53259
R 7012	MRS25	1% 237E	5322 116 53259
R 7013	MRS25	1% 4K64	5322 116 53212
R 7014	1/4W .25%	196E	5322 116 80239
R 7016	MRS25	1% 46E4	5322 116 53248
R 7017	MRS25	1% 46E4	5322 116 53248
R 7018	1/4W .25%	196E	5322 116 80239
R 7019		0.3W 25% 100K	5322 105 20038
R 7021	MRS25	1% 31K6	5322 116 53262

POSNR	DESCRIPTION	ORDERING CODE
R 7022	0.3W 25% 100K	5322 105 20038
R 7023	MRS25 1% 31K6	5322 116 53262
R 7024	MRS25 1% 10K	4822 116 53022
R 7026	1/4W .25% 316E	5322 116 80236
R 7027	1/4W .25% 316E	5322 116 80236
R 7028	MRS25 1% 1K33	5322 116 53512
R 7029	MRS25 1% 562E	5322 116 53214
R 7031	1/4W .25% 196E	5322 116 80239
R 7032	MRS25 1% 1K	4822 116 53108
R 7033	MRS25 1% 1K78	5322 116 53208
R 7034	MRS25 1% 31K6	5322 116 53262
R 7036	0.3W 25% 100K	5322 105 20038
R 7037	MRS25 1% 31K6	5322 116 53262
R 7038	MRS25 1% 10K	4822 116 53022
R 7039	1/4W .25% 196E	5322 116 80239
R 7041	MRS25 1% 3K48	4822 116 53315
R 7042	MRS25 1% 12K1	4822 116 52957
R 7043	MRS25 1% 4K22	5322 116 53246
R 7044	MRS25 1% 5K62	5322 116 53495
R 7045	MRS25 1% 1M	4822 116 52843
R 7046	0.3W 25% 100K	5322 105 20038
R 7047	VR25 5% 10M	4822 110 72214
R 7048	VR25 5% 10M	4822 110 72214
R 7049	VR25 5% 10M	4822 110 72214
R 7051	VR25 5% 10M	4822 110 72214
R 7052	0.3W 25% 100K	5322 105 20038
R 7053	VR25 5% 2M7	4822 110 72198
R 7054	1/4W .25% 249K	5322 116 53205
R 7056	1/4W .25% 249K	5322 116 53205
R 7057	1/4W .25% 249K	5322 116 53205
R 7058	1/4W .25% 249K	5322 116 53205
R 7059	MRS25 1% 10K	4822 116 53022
R 7062	MRS25 1% 10K	4822 116 53022
R 7063	MRS25 1% 68E1	5322 116 53264
R 7064	MRS25 1% 46E4	5322 116 53248
R 7066	MRS25 1% 46E4	5322 116 53248
R 7067	1/4W .25% 150E	5322 116 53399
R 7068	1/4W .25% 150E	5322 116 53399
R 7069	MRS25 1% 68E1	5322 116 53264
R 7070	MRS25 1% 681E	4822 116 53123
R 7071	MRS25 1% 10K	4822 116 53022
R 7072	MRS25 1% 110E	4822 116 52906
R 7073	MRS25 1% 110E	4822 116 52906
R 7074	MRS25 1% 110E	4822 116 52906
R 7076	MRS25 1% 46E4	5322 116 53248
R 7077	MRS25 1% 46E4	5322 116 53248
R 7078	1/4W .25% 562E	5322 116 80235
R 7079	1/4W .25% 562E	5322 116 80235
R 7081	1/4W .25% 562E	5322 116 80235
R 7082	1/4W .25% 562E	5322 116 80235
R 7083	MRS25 1% 26K1	5322 116 53261
R 7084	0.3W 25% 100K	5322 105 20038
R 7086	MRS25 1% 26K1	5322 116 53261
R 7087	MRS25 1% 46E4	5322 116 53248
R 7088	MRS25 1% 46E4	5322 116 53248
R 7089	MRS25 1% 2K15	5322 116 53239
R 7091	MRS25 1% 2K15	5322 116 53239
R 7094	MRS25 1% 383E	5322 116 53332
R 7096	MRS25 1% 383E	5322 116 53332
R 7097	MRS25 1% 10K	4822 116 53022
R 7098	1/4W .25% 375E	5322 116 53407
R 7099	1/4W .25% 375E	5322 116 53407
R 7103	1/4W .25% 316E	5322 116 80236
R 7104	MRS25 1% 10K	4822 116 53022
R 7106	1/4W .25% 316E	5322 116 80236
R 7107	MRS25 1% 46E4	5322 116 53248
R 7108	MRS25 1% 68E1	5322 116 53264
R 7109	MRS25 1% 68E1	5322 116 53264
R 7110	MRS25 1% 10K	4822 116 53022
R 7111	MRS25 1% 46E4	5322 116 53248
R 7112	MRS25 1% 10K	4822 116 53022
R 7113	MRS25 1% 16K2	5322 116 53589
R 7114	MRS25 1% 3K83	4822 116 53079
R 7116	0.3W 25% 470E	5322 105 20028
R 7117	MRS25 1% 2K37	5322 116 53536
R 7118	MRS25 1% 2K15	5322 116 53239
R 7119	MRS25 1% 147E	5322 116 53569
R 7121	MRS25 1% 3K83	4822 116 53079
R 7122	MRS25 1% 11K	4822 116 52907
R 7123	MRS25 1% 10K	4822 116 53022
R 7124	MRS25 1% 100K	4822 116 52973
R 7126	MRS25 1% 100K	4822 116 52973
R 7127	MRS25 1% 10K	4822 116 53022
R 7128	MRS25 1% 10K	4822 116 53022
R 7129	0.3W 25% 47K	5322 105 20036
R 7131	MRS25 1% 10K	4822 116 53022
R 7132	1/4W .25% 475E	5322 116 80238
R 7133	1/4W .25% 475E	5322 116 80238
R 7134	1/4W .25% 475E	5322 116 80238
R 7136	1/4W .25% 475E	5322 116 80238
R 7137	MRS25 1% 2K15	5322 116 53239

POSNR	DESCRIPTION	ORDERING CODE
R 7138	MRS25 1% 46E4	5322 116 53248
R 7139	MRS25 1% 196E	5322 116 53492
R 7141	MRS25 1% 4K64	5322 116 53212
R 7142	MRS25 1% 100K	4822 116 52973
R 7143	MRS25 1% 10K	4822 116 53022
R 7144	MRS25 1% 34K8	5322 116 53429
R 7146	MRS25 1% 681E	4822 116 53123
R 7147	MRS25 1% 121K	4822 116 52958
R 7148	MRS25 1% 511E	5322 116 53135
R 7149	MRS25 1% 2K15	5322 116 53239
R 7151	MRS25 1% 681E	4822 116 53123
R 7152	MRS25 1% 2K15	5322 116 53239
R 7153	MRS25 1% 4K64	5322 116 53212
R 7154	MRS25 1% 4K64	5322 116 53212
R 7156	0.3W 25% 10K	4822 105 10455
R 7158	0.3W 25% 100K	5322 105 20038
R 7159	0.3W 25% 22K	5322 105 20035
R 7161	MRS25 1% 4K64	5322 116 53212
R 7162	MRS25 1% 1K	4822 116 53108
R 7163	MRS25 1% 3E48	4822 116 52994
R 7164	MRS25 1% 6E81	4822 116 53009
R 7166	MRS25 1% 2E15	5322 116 53722
R 7168	MRS25 1% 2E15	5322 116 53722
R 7169	MRS25 1% 1E47	5322 116 80247
R 7171	MRS25 1% 121E	4822 116 52955
R 7172	MRS25 1% 71E5	5322 116 53528
R 7173	MRS25 1% 121E	4822 116 52955
R 7174	MRS25 1% 71E5	5322 116 53528
R 7176	MRS25 1% 100E	5322 116 53126
R 7177	MRS25 1% 1E	4822 116 52976
R 7178	MRS25 1% 1E47	5322 116 80247
R 7179	MRS25 1% 2E15	5322 116 53722
R 7181	MRS25 1% 10K	4822 116 53022
R 7182	MRS25 1% 10K	4822 116 53022
R 7201	MCR18 1% 47E	4822 111 90217
R 7202	MCR18 1% 100E	5322 111 91134
R 7203	MCR18 1% 100E	5322 111 91134
R 7204	MCR18 1% 3K9	5322 111 91135
R 7206	MCR18 1% 2K2	4822 111 90248
R 7207	MCR18 1% 100E	5322 111 91134
R 7209	MCR18 1% 2K2	4822 111 90248
R 7211	MCR18 1% 3K9	5322 111 91135
R 7212	MCR18 1% 47E	4822 111 90217
R 7213	MCR18 1% 51E	5322 111 91352
R 7216	MCR18 1% 100E	5322 111 91134
R 7217	MCR18 1% 1K2	5322 111 90096
R 7218	MCR18 1% 47E	4822 111 90217
R 7221	MCR18 1% 47E	4822 111 90217
R 7222	MCR18 1% 47E	4822 111 90217
R 7223	MCR18 1% 47E	4822 111 90217
R 7224	MCR18 1% 100E	5322 111 91134
R 7226	MCR18 1% 100E	5322 111 91134
R 7227	MCR18 1% 47E	4822 111 90217
R 7228	MCR18 1% 47E	4822 111 90217
R 7229	MCR18 1% 47E	4822 111 90217
R 7231	MCR18 1% 47E	4822 111 90217
R 7232	MCR18 1% 1K2	5322 111 90096
R 7233	MCR18 1% 1K2	5322 111 90096
R 7234	MCR18 1% 27K	4822 111 90542
R 7235	MCR18 1% 39E	4822 111 90361
R 7236	MCR18 1% 1K8	5322 111 90101
R 7237	MCR18 1% 1K8	5322 111 90101
R 7238	MCR18 1% 47E	4822 111 90217
R 7239	MCR18 1% 100E	5322 111 91134
R 7240	MCR18 1% 39E	4822 111 90361
R 7241	MCR18 1% 47E	4822 111 90217
R 7242	MCR18 1% 3K9	5322 111 91135
R 7243	MCR18 1% 100E	5322 111 91134
R 7244	MCR18 1% 100E	5322 111 91134
R 7246	MCR18 1% 680E	4822 111 90162
R 7247	MCR18 1% 680E	4822 111 90162
R 7248	MCR18 1% 47E	4822 111 90217
R 7249	MCR18 1% 47E	4822 111 90217
R 7251	MCR18 1% 2K7	4822 111 90569
R 7252	MCR18 1% 1K5	4822 111 90151
R 7253	MCR18 1% 100E	5322 111 91134
R 7254	MCR18 1% 68E	4822 111 90203
R 7256	MCR18 1% 1K5	4822 111 90151
R 7257	MCR18 1% 2K7	4822 111 90569
R 7258	MCR18 1% 330E	5322 111 90106
R 7259	MCR18 1% 330E	5322 111 90106
R 7261	MCR18 1% 100E	5322 111 91134
R 7262	MCR18 1% 47E	4822 111 90217
R 7263	MCR18 1% 100E	5322 111 91134
R 7264	MCR18 1% 47E	4822 111 90217
R 7266	MCR18 1% 100E	5322 111 91134
R 7267	MCR18 1% 3K9	5322 111 91135
R 7268	MCR18 1% 100E	5322 111 91134
R 7269	MCR18 1% 100E	5322 111 91134
R 7271	MCR18 1% 470E	5322 111 90109
R 7272	MCR18 1% 47E	4822 111 90217

POSNR	DESCRIPTION		ORDERING CODE
R 7273	MCR18	1% 470E	5322 111 90109
R 7274	MCR18	1% 47E	4822 111 90217
R 7276	MCR18	1% 3K9	5322 111 91135
R 7277	MCR18	1% 3K9	5322 111 91135
R 7278	MCR18	1% 47E	4822 111 90217
R 7279	MCR18	1% 1K8	5322 111 90101
R 7281	MCR18	1% 47E	4822 111 90217
R 7282	MCR18	1% 680E	4822 111 90162
R 7283	MCR18	1% 47E	4822 111 90217
R 7284	MCR18	1% 680E	4822 111 90162
R 7286	MCR18	1% 47E	4822 111 90217
R 7287	MCR18	1% 100E	5322 111 91134
R 7288	MCR18	1% 330E	5322 111 90106
R 7289	MCR18	1% 47E	4822 111 90217
R 7291	MCR18	1% 330E	5322 111 90106
R 7292	MCR18	1% 68E	4822 111 90203
R 7293	MCR18	1% 68E	4822 111 90203
R 7294	MCR18	1% 560E	5322 111 90113
R 7297	MCR18	1% 47E	4822 111 90217
R 7298	MCR18	1% 470E	5322 111 90109
R 7299	MCR18	1% 47E	4822 111 90217
R 7301	MCR18	1% 470E	5322 111 90109
R 7302	MCR18	1% 47E	4822 111 90217
R 7303	MCR18	1% 3K9	5322 111 91135
R 7304	MCR18	1% 3K9	5322 111 91135
R 7306	MCR18	1% 1K8	5322 111 90101
R 7307	MCR18	1% 47E	4822 111 90217
R 7308	MCR18	1% 680E	4822 111 90162
R 7309	MCR18	1% 47E	4822 111 90217
R 7311	MCR18	1% 680E	4822 111 90162
R 7312	MCR18	1% 47E	4822 111 90217
R 7313	MCR18	1% 100E	5322 111 91134
R 7314	MCR18	1% 330E	5322 111 90106
R 7316	MCR18	1% 47E	4822 111 90217
R 7317	MCR18	1% 560E	5322 111 90113
R 7318	MCR18	1% 330E	5322 111 90106
R 7319	MCR18	1% 68E	4822 111 90203
R 7321	MCR18	1% 68E	4822 111 90203
R 7351	MCR18	1% 10K	4822 111 90249
R 7352	MCR18	1% 10K	4822 111 90249
R 7353	MCR18	1% 68E	4822 111 90203
R 7354	MCR18	1% 270E	4822 111 90154
R 7356	MCR18	1% 56E	4822 111 90239
R 7357	MCR18	1% 68E	4822 111 90203
R 7358	MCR18	1% 68E	4822 111 90203
R 7359	MCR18	1% 51E	5322 111 91352
R 7361	MCR18	1% 68E	4822 111 90203
R 7362	MCR18	1% 270E	4822 111 90154
R 7363	MCR18	1% 56E	4822 111 90239
R 7364	MCR18	1% 68E	4822 111 90203
R 7366	MCR18	1% 10K	4822 111 90249
R 7367	MCR18	1% 10K	4822 111 90249
R 7368	MCR18	1% 68E	4822 111 90203
R 7369	MCR18	1% 680E	4822 111 90162
R 7371	MCR18	1% 680E	4822 111 90162
R 7372	MCR18	1% 68E	4822 111 90203
R 7373	MCR18	1% 270E	4822 111 90154
R 7374	MCR18	1% 56E	4822 111 90239
R 7376	MCR18	1% 68E	4822 111 90203
R 7401	MCR18	1% 27K	4822 111 90542
R 7402	MCR18	1% 47E	4822 111 90217
R 7403	MCR18	1% 100E	5322 111 91134
R 7404	MCR18	1% 100E	5322 111 91134
R 7406	MCR18	1% 3K9	5322 111 91135
R 7407	MCR18	1% 1K5	4822 111 90151
R 7409	MCR18	1% 1K5	4822 111 90151
R 7411	MCR18	1% 3K9	5322 111 91135
R 7412	MCR18	1% 68E	4822 111 90203
R 7413	MCR18	1% 47E	4822 111 90217
R 7414	MCR18	1% 100E	5322 111 91134
R 7416	MCR18	1% 51E	5322 111 91352
R 7418	MCR18	1% 1K2	5322 111 90096
R 7419	MCR18	1% 82E	4822 111 90124
R 7421	MCR18	1% 100E	5322 111 91134
R 7422	MCR18	1% 100E	5322 111 91134
R 7423	MCR18	1% 47E	4822 111 90217
R 7424	MCR18	1% 47E	4822 111 90217
R 7426	MCR18	1% 3K9	5322 111 91135
R 7427	MCR18	1% 3K9	5322 111 91135
R 7428	MCR18	1% 47E	4822 111 90217
R 7429	MCR18	1% 1K8	5322 111 90101
R 7431	MCR18	1% 47E	4822 111 90217
R 7432	MCR18	1% 680E	4822 111 90162
R 7433	MCR18	1% 680E	4822 111 90162
R 7434	MCR18	1% 100E	5322 111 91134
R 7436	MCR18	1% 330E	5322 111 90106
R 7437	MCR18	1% 47E	4822 111 90217
R 7438	MCR18	1% 18E	5322 111 90139
R 7439	MCR18	1% 330E	5322 111 90106
R 7441	MCR18	1% 100E	5322 111 91134
R 7442	MCR18	1% 560E	5322 111 90113

POSNR	DESCRIPTION		ORDERING CODE
R 7443	MCR18	1% 47E	4822 111 90217
R 7444	MCR18	1% 47E	4822 111 90217
R 7451	MTP10	20% 10K	5322 101 14066
R 7452	MRS25	1% 511K	5322 116 53334
R 7453	MRS25	1% 21K5	5322 116 53241
R 7454	MTP10	20% 10K	5322 101 14066
R 7456	MRS25	1% 511K	5322 116 53334
R 7457	MRS25	1% 21K5	5322 116 53241
R 7458	MRS25	1% 100E	5322 116 53126
R 7459	MRS25	1% 100E	5322 116 53126
R 7461	MRS25	1% 100E	5322 116 53126
R 7461	MRS25	1% 56K2	5322 116 53222
R 7462	MRS25	1% 56K2	5322 116 53222
R 7463	MRS25	1% 56K2	5322 116 53222
R 7464	MRS25	1% 56K2	5322 116 53222
R 7466	MRS25	1% 422E	5322 116 53592
R 7467	MRS25	1% 56K2	5322 116 53222
R 7468	MRS25	1% 56K2	5322 116 53222
R 7469	MRS25	1% 56K2	5322 116 53222
R 7471	MRS25	1% 56K2	5322 116 53222
R 7472	MRS25	1% 422E	5322 116 53592
R 7501	MRS25	1% 19K6	5322 116 53258
R 7502	MRS25	1% 2K15	5322 116 53239
R 7503	MRS25	1% 4K22	5322 116 53246
R 7504	MRS25	1% 2K87	5322 116 53513
R 7506	MRS25	1% 681E	4822 116 53123
R 7507	MCR18	1% 47E	4822 111 90217
R 7508	MCR18	1% 51E	5322 111 91352
R 7509	MCR18	1% 51E	5322 111 91352
R 7511	MCR18	1% 47E	4822 111 90217
R 7512	0.3W	25% 100K	5322 105 20038
R 7513	0.3W	25% 100K	5322 105 20038
R 7514	MRS25	1% 100E	5322 116 53126
R 7515	0.3W	25% 2K2	5322 105 20033
R 7516	MRS25	1% 100K	4822 116 52973
R 7517	MRS25	1% 100K	4822 116 52973
R 7518	MRS25	1% 5K62	5322 116 53495
R 7519	MRS25	1% 10E	4822 116 52891
R 7520	MRS25	1% 68E1	5322 116 53264
R 7521	MRS25	1% 10E	4822 116 52891
R 7522	MRS25	1% 147E	5322 116 53569
R 7523	MRS25	1% 348E	5322 116 53591
R 7524	MRS25	1% 1K78	5322 116 53208
R 7525	MRS25	1% 68E1	5322 116 53264
R 7526	MRS25	1% 100E	5322 116 53126
R 7527	MRS25	1% 100E	5322 116 53126
R 7528	MRS25	1% 10E	4822 116 52891
R 7529	MRS25	1% 10E	4822 116 52891
R 7530	MRS25	1% 68E1	5322 116 53264
R 7531	MRS25	1% 46E4	5322 116 53248
R 7532	MRS25	1% 100E	5322 116 53126
R 7533	MRS25	1% 1K78	5322 116 53208
R 7534	MRS25	1% 147E	5322 116 53569
R 7535	MRS25	1% 68E1	5322 116 53264
R 7536	MRS25	1% 348E	5322 116 53591
R 7537	MRS25	1% 1K78	5322 116 53208
R 7538	MRS25	1% 100E	5322 116 53126
R 7539	MRS25	1% 100E	5322 116 53126
R 7541	MRS25	1% 10E	4822 116 52891
R 7542	MRS25	1% 10E	4822 116 52891
R 7543	MRS25	1% 46E4	5322 116 53248
R 7544	MRS25	1% 100E	5322 116 53126
R 7546	MRS25	1% 1K78	5322 116 53208
R 7547	MRS25	1% 100K	4822 116 52973
R 7548	MRS25	1% 100K	4822 116 52973
R 7554	MRS25	1% 10K	4822 116 53022
R 7556	MRS25	1% 10E	4822 116 52891
R 7557	MRS25	1% 3K16	4822 116 53021
R 7558	MRS25	1% 3K16	4822 116 53021
R 7559	MRS25	1% 1E	4822 116 52976
R 7561	MRS25	1% 1K	4822 116 53108
R 7562	MRS25	1% 1K	4822 116 53108
R 7563	MRS25	1% 261E	5322 116 53549
R 7564	MRS25	1% 100E	5322 116 53126
R 7566	0.3W	25% 10K	4822 105 10455
R 7569	MRS25	1% 1K62	5322 116 53257
R 7571	MRS25	1% 51E1	5322 116 53213
R 7572	MRS25	1% 1K	4822 116 53108
R 7573	MRS25	1% 1K	4822 116 53108
R 7574	MRS25	1% 261E	5322 116 53549
R 7576	MRS25	1% 100E	5322 116 53126
R 7577	MRS25	1% 1K1	5322 116 53473
R 7578	MRS25	1% 100E	5322 116 53126
R 7579	MRS25	1% 261E	5322 116 53549
R 7581	MRS25	1% 619E	5322 116 53337
R 7582	MRS25	1% 619E	5322 116 53337
R 7583	0.3W	25% 1K	5322 105 20032
R 7584	0.3W	25% 1K	5322 105 20032
R 7586	MRS25	1% 511E	5322 116 53135
R 7587	MRS25	1% 511E	5322 116 53135
R 7588	MRS25	1% 511E	5322 116 53135

POSNR	DESCRIPTION	ORDERING CODE
R 7589	MCR18 1% 390E	5322 111 91205
R 7592	0.3W 25% 220K	5322 105 20039
R 7596	MRS25 1% 511E	5322 116 53135
R 7597	MRS25 1% 511E	5322 116 53135
R 7598	MRS25 1% 511E	5322 116 53135
R 7601	-105-103 10K	5322 111 90473
R 7602	-105-103 10K	5322 111 90473
R 7603	0.3W 25% 220K	5322 105 20039
R 7606	0.3W 25% 220K	5322 105 20039
R 7611	MRS25 1% 1K	4822 116 53108
R 7612	0.3W 25% 1K	5322 105 20032
R 7613	MCR18 1% 1K	5322 111 90092
R 7614	MCR18 1% 1K	5322 111 90092
R 7702	MRS25 1% 1K96	5322 116 53237
R 7703	MRS25 1% 4K22	5322 116 53246
R 7704	MRS25 1% 2K87	5322 116 53513
R 7705	MCR18 1% 1K	5322 111 90092
R 7706	MRS25 1% 619E	5322 116 53337
R 7707	MCR18 1% 47E	4822 111 90217
R 7708	MCR18 1% 51E	5322 111 91352
R 7709	MCR18 1% 51E	5322 111 91352
R 7710	MCR18 1% 1K	5322 111 90092
R 7711	MCR18 1% 47E	4822 111 90217
R 7712	0.3W 25% 100K	5322 105 20038
R 7713	0.3W 25% 100K	5322 105 20038
R 7714	MRS25 1% 100E	5322 116 53126
R 7715	0.3W 25% 2K2	5322 105 20033
R 7717	MRS25 1% 100K	4822 116 52973
R 7718	MRS25 1% 100K	4822 116 52973
R 7719	MRS25 1% 10E	4822 116 52891
R 7720	MRS25 1% 68E1	5322 116 53264
R 7721	MRS25 1% 10E	4822 116 52891
R 7722	MRS25 1% 147E	5322 116 53569
R 7723	MRS25 1% 348E	5322 116 53591
R 7724	MRS25 1% 1K78	5322 116 53208
R 7725	MRS25 1% 68E1	5322 116 53264
R 7726	MRS25 1% 100E	5322 116 53126
R 7727	MRS25 1% 100E	5322 116 53126
R 7728	MRS25 1% 10E	4822 116 52891
R 7729	MRS25 1% 10E	4822 116 52891
R 7730	MRS25 1% 68E1	5322 116 53264
R 7731	MRS25 1% 46E4	5322 116 53248
R 7732	MRS25 1% 100E	5322 116 53126
R 7733	MRS25 1% 1K78	5322 116 53208
R 7734	MRS25 1% 147E	5322 116 53569
R 7735	MRS25 1% 68E1	5322 116 53264
R 7736	MRS25 1% 348E	5322 116 53591
R 7737	MRS25 1% 1K78	5322 116 53208
R 7738	MRS25 1% 100E	5322 116 53126
R 7739	MRS25 1% 100E	5322 116 53126
R 7741	MRS25 1% 10E	4822 116 52891
R 7742	MRS25 1% 10E	4822 116 52891
R 7743	MRS25 1% 46E4	5322 116 53248
R 7744	MRS25 1% 100E	5322 116 53126
R 7746	MRS25 1% 1K78	5322 116 53208
R 7747	MRS25 1% 100K	4822 116 52973
R 7748	MRS25 1% 100K	4822 116 52973
R 7754	MRS25 1% 10K	4822 116 53022
R 7756	MRS25 1% 10E	4822 116 52891
R 7761	MRS25 1% 1K	4822 116 53108
R 7762	MRS25 1% 1K	4822 116 53108
R 7763	MRS25 1% 261E	5322 116 53549
R 7764	MRS25 1% 100E	5322 116 53126
R 7765	MRS25 1% 5K11	5322 116 53494
R 7766	0.3W 25% 10K	4822 105 10455
R 7769	MRS25 1% 1K62	5322 116 53257
R 7770	MRS25 1% 121E	4822 116 52955
R 7771	MRS25 1% 51E1	5322 116 53213
R 7772	MRS25 1% 1K	4822 116 53108
R 7773	MRS25 1% 1K	4822 116 53108
R 7774	MRS25 1% 261E	5322 116 53549
R 7775	MRS25 1% 5K11	5322 116 53494
R 7776	MRS25 1% 100E	5322 116 53126
R 7777	MRS25 1% 1K1	5322 116 53473
R 7778	MRS25 1% 100E	5322 116 53126
R 7779	MRS25 1% 261E	5322 116 53549
R 7781	MRS25 1% 619E	5322 116 53337
R 7782	MRS25 1% 619E	5322 116 53337
R 7783	0.3W 25% 1K	5322 105 20032
R 7784	0.3W 25% 1K	5322 105 20032
R 7786	MRS25 1% 511E	5322 116 53135
R 7787	MRS25 1% 511E	5322 116 53135
R 7788	MRS25 1% 511E	5322 116 53135
R 7789	MCR18 1% 390E	5322 111 91205
R 7792	0.3W 25% 220K	5322 105 20039
R 7796	MRS25 1% 511E	5322 116 53135
R 7797	MRS25 1% 511E	5322 116 53135
R 7798	MRS25 1% 511E	5322 116 53135
R 7801	-105-103 10K	5322 111 90473
R 7802	-105-103 10K	5322 111 90473
R 7803	0.3W 25% 220K	5322 105 20039

POSNR	DESCRIPTION	ORDERING CODE
R 7806	0.3W 25% 220K	5322 105 20039
R 7851	MRS25 1% 1E	4822 116 52976
R 7852	MRS25 1% 1E	4822 116 52976
R 7853	MRS25 1% 5E11	4822 116 52999
R 7854	MRS25 1% 1E	4822 116 52976
R 7856	MRS25 1% 1E	4822 116 52976
R 7857	MRS25 1% 1E	4822 116 52976
R 7858	MRS25 1% 1E	4822 116 52976
R 7859	MRS25 1% 5E11	4822 116 52999
R 7861	MRS25 1% 162E	5322 116 53523
R 7862	MRS25 1% 464E	5322 116 53232
R 7863	MRS25 1% 1E	4822 116 52976
R 7864	MRS25 1% 1E	4822 116 52976
R 7866	MRS25 1% 1K47	5322 116 53185
R 7867	MRS25 1% 1E	4822 116 52976
R 7868	MRS25 1% 1E	4822 116 52976
R 7901	RC-01 5% 1E	4822 111 90184
R 7902	RC-01 5% 1E	4822 111 90184
R 7903	RC-01 5% 1E	4822 111 90184
R 7904	RC-01 5% 1E	4822 111 90184
R 7906	MCR18 1% 68K	4822 111 90202
R 7907	MCR18 1% 3K9	5322 111 91135
R 7908	MCR18 1% 1K	5322 111 90092
R 7909	MCR18 1% 820E	4822 111 90171
R 7911	MCR18 1% 150E	5322 111 90098
R 7912	MCR18 1% 820E	4822 111 90171
R 7913	MCR18 1% 150E	5322 111 90098
R 7914	MCR18 1% 820E	4822 111 90171
R 7938	MCR18 1% 7K5	5322 116 80609
R 7939	0.3W 25% 22K	5322 105 20035
R 7941	MCR18 1% 15K	4822 111 90196
R 7942	MCR18 1% 1K6	5322 116 80596
R 7943	MCR18 1% 1K1	5322 111 91466
R 7944	MCR18 1% 1K1	5322 111 91466
R 7946	MCR18 1% 24K	5322 116 80602
R 7947	MCR18 1% 1K6	5322 116 80596
R 7948	MCR18 1% 1K1	5322 111 91466
R 7949	MCR18 1% 1K1	5322 111 91466
R 7951	MCR18 1% 24K	5322 116 80602
R 7952	MCR18 1% 3K6	5322 116 80604
R 7953	0.3W 25% 4K7	5322 105 20034
R 7954	MCR18 1% 3K3	4822 111 90157
R 7957	MCR18 1% 2K	5322 116 80858
R 7958	MCR18 1% 100E	5322 111 91134
R 7959	0.3W 25% 4K7	5322 105 20034
R 7962	MCR18 1% 4K3	5322 116 80605
R 7963	MCR18 1% 1K	5322 111 90092
R 7964	MCR18 1% 3K3	4822 111 90157
R 7965	MCR18 1% 1K	5322 111 90092
R 7967	MCR18 1% 2K2	4822 111 90248
R 8001	MCR18 1% 1K	5322 111 90092
R 8002	MCR18 1% 1K	5322 111 90092
R 8003	MCR18 1% 4K7	5322 111 90111
R 8004	MCR18 1% 1K8	5322 111 90101
R 8008	MCR18 1% 10K	4822 111 90249
R 8011	MCR18 1% 1K	5322 111 90092
R 8012	MCR18 1% 10K	4822 111 90249
R 8013	MCR18 1% 10K	4822 111 90249
R 8014	MCR18 1% 33E	4822 111 90357
R 8016	MCR18 1% 3K9	5322 111 91135
R 8017	MCR18 1% 33E	4822 111 90357
R 8018	MCR18 1% 1K	5322 111 90092
R 8019	MCR18 1% 47E	4822 111 90217
R 8021	MCR18 1% 100E	5322 111 91134
R 8022	MCR18 1% 10K	4822 111 90249
R 8023	MCR18 1% 10K	4822 111 90249
R 8027	MCR18 1% 100K	4822 111 90214
R 8028	MCR18 1% 4K7	5322 111 90111
R 8029	MCR18 1% 4K7	5322 111 90111
R 8031	MCR18 1% 68K	4822 111 90202
R 8041	MCR18 1% 1K	5322 111 90092
R 8042	MCR18 1% 1K	5322 111 90092
R 8043	MCR18 1% 4K7	5322 111 90111
R 8044	MCR18 1% 1K8	5322 111 90101
R 8048	MCR18 1% 10K	4822 111 90249
R 8051	MCR18 1% 1K	5322 111 90092
R 8052	MCR18 1% 10K	4822 111 90249
R 8053	MCR18 1% 10K	4822 111 90249
R 8054	MCR18 1% 33E	4822 111 90357
R 8056	MCR18 1% 3K9	5322 111 91135
R 8057	MCR18 1% 33E	4822 111 90357
R 8058	MCR18 1% 1K	5322 111 90092
R 8059	MCR18 1% 47E	4822 111 90217
R 8061	MCR18 1% 100E	5322 111 91134
R 8062	MCR18 1% 33E	4822 111 90357
R 8063	MCR18 1% 4K7	5322 111 90111
R 8064	MCR18 1% 33E	4822 111 90357
R 8066	MCR18 1% 4K7	5322 111 90111
R 8067	MCR18 1% 100K	4822 111 90214
R 8068	MCR18 1% 4K7	5322 111 90111
R 8069	MCR18 1% 4K7	5322 111 90111

POSNR	DESCRIPTION			ORDERING CODE
R 8071	MCR18	1%	68K	4822 111 90202
R 8084	MCR18	1%	6K8	4822 111 90544
R 8086	MCR18	1%	8K2	5322 111 90118
R 8087	MCR18	1%	2K2	4822 111 90248
R 8088	MCR18	1%	33E	4822 111 90357
R 8089	MCR18	1%	100E	5322 111 91134
R 8091	MCR18	1%	33E	4822 111 90357
R 8092	MCR18	1%	15K	4822 111 90196
R 8093	MCR18	1%	15K	4822 111 90196
R 8101	MCR18	1%	330E	5322 111 90106
R 8138	MCR18	1%	7K5	5322 116 80609
R 8139	0.3W	25%	22K	5322 105 20035
R 8141	MCR18	1%	15K	4822 111 90196
R 8142	MCR18	1%	1K6	5322 116 80596
R 8143	MCR18	1%	1K1	5322 111 91466
R 8144	MCR18	1%	1K1	5322 111 91466
R 8146	MCR18	1%	24K	5322 116 80602
R 8147	MCR18	1%	1K6	5322 116 80596
R 8148	MCR18	1%	1K1	5322 111 91466
R 8149	MCR18	1%	1K1	5322 111 91466
R 8151	MCR18	1%	24K	5322 116 80602
R 8152	MCR18	1%	3K6	5322 116 80604
R 8153	0.3W	25%	4K7	5322 105 20034
R 8154	MCR18	1%	3K3	4822 111 90157
R 8157	MCR18	1%	2K	5322 116 80858
R 8158	MCR18	1%	100E	5322 111 91134
R 8159	0.3W	25%	4K7	5322 105 20034
R 8162	MCR18	1%	4K3	5322 116 80605
R 8163	MCR18	1%	1K	5322 111 90092
R 8164	MCR18	1%	3K3	4822 111 90157
R 8165	MCR18	1%	1K	5322 111 90092
R 8167	MCR18	1%	2K2	4822 111 90248
R 8201	MCR18	1%	1K	5322 111 90092
R 8202	MCR18	1%	1K	5322 111 90092
R 8203	MCR18	1%	4K7	5322 111 90111
R 8204	MCR18	1%	1K8	5322 111 90101
R 8208	MCR18	1%	10K	4822 111 90249
R 8211	MCR18	1%	1K	5322 111 90092
R 8212	MCR18	1%	10K	4822 111 90249
R 8213	MCR18	1%	10K	4822 111 90249
R 8214	MCR18	1%	33E	4822 111 90357
R 8216	MCR18	1%	3K9	5322 111 91135
R 8217	MCR18	1%	33E	4822 111 90357
R 8218	MCR18	1%	1K	5322 111 90092
R 8219	MCR18	1%	47E	4822 111 90217
R 8221	MCR18	1%	100E	5322 111 91134
R 8227	MCR18	1%	100K	4822 111 90214
R 8228	MCR18	1%	4K7	5322 111 90111
R 8229	MCR18	1%	4K7	5322 111 90111
R 8231	MCR18	1%	68K	4822 111 90202
R 8241	MCR18	1%	1K	5322 111 90092
R 8242	MCR18	1%	1K	5322 111 90092
R 8243	MCR18	1%	4K7	5322 111 90111
R 8244	MCR18	1%	1K8	5322 111 90101
R 8248	MCR18	1%	10K	4822 111 90249
R 8251	MCR18	1%	1K	5322 111 90092
R 8252	MCR18	1%	10K	4822 111 90249
R 8253	MCR18	1%	10K	4822 111 90249
R 8254	MCR18	1%	33E	4822 111 90357
R 8256	MCR18	1%	3K9	5322 111 91135
R 8257	MCR18	1%	33E	4822 111 90357
R 8258	MCR18	1%	1K	5322 111 90092
R 8259	MCR18	1%	47E	4822 111 90217
R 8261	MCR18	1%	100E	5322 111 91134
R 8262	MCR18	1%	33E	4822 111 90357
R 8263	MCR18	1%	4K7	5322 111 90111
R 8264	MCR18	1%	33E	4822 111 90357
R 8266	MCR18	1%	4K7	5322 111 90111
R 8267	MCR18	1%	100K	4822 111 90214
R 8268	MCR18	1%	4K7	5322 111 90111
R 8269	MCR18	1%	4K7	5322 111 90111
R 8271	MCR18	1%	68K	4822 111 90202
R 8284	MCR18	1%	6K8	4822 111 90544
R 8286	MCR18	1%	8K2	5322 111 90118
R 8287	MCR18	1%	2K2	4822 111 90248
R 8288	MCR18	1%	33E	4822 111 90357
R 8289	MCR18	1%	100E	5322 111 91134
R 8291	MCR18	1%	33E	4822 111 90357
R 8292	MCR18	1%	15K	4822 111 90196
R 8293	MCR18	1%	15K	4822 111 90196
R 8301	MCR18	1%	1K5	4822 111 90151
R 8302	MCR18	1%	3K9	5322 111 91135
R 8303	MCR18	1%	3K9	5322 111 91135
R 8304	MCR18	1%	3K9	5322 111 91135
R 8306	MCR18	1%	3K9	5322 111 91135
R 8307	MCR18	1%	3K9	5322 111 91135
R 8308	MCR18	1%	3K9	5322 111 91135
R 8309	MCR18	1%	1K	5322 111 90092
R 8311	MCR18	1%	33E	4822 111 90357
R 8312	MCR18	1%	4K7	5322 111 90111

POSNR	DESCRIPTION			ORDERING CODE
R 8314	MCR18	1%	1K	5322 111 90092
R 8316	MCR18	1%	1K8	5322 111 90101
R 8317	MCR18	1%	1K6	5322 116 80596
R 8321	MCR18	1%	2K7	4822 111 90569
R 8322	MCR18	1%	8K2	5322 111 90118
R 8323	MCR18	1%	1K	5322 111 90092
R 8324	MCR18	1%	1K2	5322 111 90096
R 8326	0.3W	25%	1K	5322 105 20032
R 8331	MCR18	1%	33E	4822 111 90357
R 8332	MCR18	1%	4K7	5322 111 90111
R 8333	MCR18	1%	33E	4822 111 90357
R 8334	MCR18	1%	1K	5322 111 90092
R 8336	MCR18	1%	1K8	5322 111 90101
R 8351	MCR18	1%	33E	4822 111 90357
R 8352	MCR18	1%	4K7	5322 111 90111
R 8353	MCR18	1%	33E	4822 111 90357
R 8354	MCR18	1%	1K	5322 111 90092
R 8356	MCR18	1%	1K8	5322 111 90101
R 8371	MCR18	1%	33E	4822 111 90357
R 8372	MCR18	1%	4K7	5322 111 90111
R 8373	MCR18	1%	33E	4822 111 90357
R 8374	MCR18	1%	1K	5322 111 90092
R 8376	MCR18	1%	1K8	5322 111 90101
R 8417	MCR18	1%	1K	5322 111 90092
R 8419	0.3W	25%	10K	4822 105 10455
R 8421	0.3W	25%	1K	5322 105 20032
R 8422	0.3W	25%	1K	5322 105 20032
R 8423	0.3W	25%	1K	5322 105 20032
R 8424	0.3W	25%	1K	5322 105 20032
R 8426	0.3W	25%	1K	5322 105 20032
R 8427	0.3W	25%	1K	5322 105 20032
R 8428	0.3W	25%	1K	5322 105 20032
R 8429	0.3W	25%	1K	5322 105 20032
R 8432	MCR18	1%	1K	5322 111 90092
R 8434	0.3W	25%	10K	4822 105 10455
R 8436	0.3W	25%	10K	4822 105 10455
R 8438	MCR18	1%	1K	5322 111 90092
R 8441	0.3W	25%	1K	5322 105 20032
R 8442	0.3W	25%	1K	5322 105 20032
R 8443	0.3W	25%	1K	5322 105 20032
R 8444	0.3W	25%	1K	5322 105 20032
R 8446	0.3W	25%	1K	5322 105 20032
R 8447	0.3W	25%	1K	5322 105 20032
R 8448	0.3W	25%	1K	5322 105 20032
R 8449	0.3W	25%	1K	5322 105 20032
R 8451	0.3W	25%	10K	4822 105 10455
R 8453	MCR18	1%	1K	5322 111 90092
R 8456	RC-01	5%	8E2	4822 111 90357
R 8457	RC-01	5%	8E2	4822 111 90357
R 8458	RC-01	5%	8E2	4822 111 90357
R 8459	RC-01	5%	8E2	4822 111 90357
R 8461	RC-01	5%	8E2	4822 111 90357
R 8462	RC-01	5%	8E2	4822 111 90357
R 8463	RC-01	5%	8E2	4822 111 90357
R 8464	RC-01	5%	8E2	4822 111 90357
R 8501	MRS25	1%	51E1	5322 116 53213
R 8502	MRS25	1%	562E	5322 116 53214
R 8503	MRS25	1%	51E1	5322 116 53213
R 8504	MRS25	1%	215E	5322 116 53325
R 8506	MRS25	1%	215E	5322 116 53325
R 8507	MRS25	1%	562E	5322 116 53214
R 8508	MRS25	1%	10E	4822 116 52891
R 8509	MRS25	1%	562E	5322 116 53214
R 8511	MRS25	1%	51E1	5322 116 53213
R 8512	MRS25	1%	10E	4822 116 52891
R 8513	MRS25	1%	51E1	5322 116 53213
R 8514	MRS25	1%	31E6	5322 116 54964
R 8516	MRS25	1%	31E6	5322 116 54964
R 8517	MRS25	1%	909E	4822 116 53533
R 8518	MRS25	1%	51E1	5322 116 53213
R 8519	MRS25	1%	909E	4822 116 53533
R 8521	MRS25	1%	31E6	5322 116 54964
R 8522	MRS25	1%	2K61	5322 116 53327
R 8523	MRS25	1%	3K48	4822 116 53315
R 8524	MRS25	1%	100E	5322 116 53126
R 8526	MRS25	1%	1K33	5322 116 53512
R 8527	MRS25	1%	2K15	5322 116 53239
R 8528	MRS25	1%	1K62	5322 116 53257
R 8529	MRS25	1%	2K61	5322 116 53327
R 8531	MRS25	1%	8K25	5322 116 53267
R 8532	MRS25	1%	464E	5322 116 53232
R 8533	MRS25	1%	31E6	5322 116 54964
R 8534	MRS25	1%	100E	5322 116 53126
R 8536	MRS25	1%	100E	5322 116 53126
R 8537	MRS25	1%	100E	5322 116 53126
R 8538	MRS25	1%	261E	5322 116 53549
R 8539	MRS25	1%	2K15	5322 116 53239
R 8541	MRS25	1%	10K	4822 116 53022
R 8542	MRS25	1%	3K83	4822 116 53079
R 8543	MRS25	1%	261E	5322 116 53549

POSNR	DESCRIPTION	ORDERING CODE
R 8547	MRS25 1% 133E	5322 116 53424
R 8548	MRS25 1% 12K1	4822 116 52957
R 8549	MRS25 1% 34K8	5322 116 53429
R 8551	MRS25 1% 237K	5322 116 80145
R 8559	MRS25 1% 619E	5322 116 53337
R 8561	MRS25 1% 2K15	5322 116 53239
R 8562	MRS25 1% 10K	4822 116 53022
R 8563	MRS25 1% 619E	5322 116 53337
R 8564	MRS25 1% 2K15	5322 116 53239
R 8566	MRS25 1% 10K	4822 116 53022
R 8567	MRS25 1% 619E	5322 116 53337
R 8568	MRS25 1% 619E	5322 116 53337
R 8569	MRS25 1% 75E	5322 116 53339
R 8571	MRS25 1% 121E	4822 116 52955
R 8579	MRS25 1% 2K15	5322 116 53239
R 8581	MRS25 1% 1K	4822 116 53108
R 8582	MRS25 1% 422E	5322 116 53592
R 8583	MRS25 1% 1K	4822 116 53108
R 8584	MRS25 1% 237E	5322 116 53259
R 8586	MRS25 1% 51E1	5322 116 53213
R 8587	MRS25 1% 2K15	5322 116 53239
R 8588	MRS25 1% 1K	4822 116 53108
R 8589	MRS25 1% 422E	5322 116 53592
R 8591	MRS25 1% 1K	4822 116 53108
R 8592	MRS25 1% 147E	5322 116 53569
R 8593	MRS25 1% 51E1	5322 116 53213
R 8594	MRS25 1% 196E	5322 116 53492
R 8597	MRS25 1% 2K61	5322 116 53327
R 8598	MRS25 1% 100K	4822 116 52973
R 8599	MRS25 1% 82E5	5322 116 53538
R 8601	MRS25 1% 681E	4822 116 53123
R 8604	MRS25 1% 2K61	5322 116 53327
R 8606	MRS25 1% 16K2	5322 116 53589
R 8607	0.3W 25% 1K	5322 105 20032
R 8608	MRS25 1% 2K37	5322 116 53536
R 8609	MRS25 1% 1K96	5322 116 53237
R 8611	MRS25 1% 2K15	5322 116 53239
R 8612	MRS25 1% 10K	4822 116 53022
R 8613	MRS25 1% 51E1	5322 116 53213
R 8614	MRS25 1% 51E1	5322 116 53213
R 8616	MRS25 1% 51E1	5322 116 53213
R 8617	MRS25 1% 51E1	5322 116 53213
R 8620	MRS25 1% 100E	5322 116 53126
R 8701	MCR18 1% 100E	5322 111 91134
R 8702	MCR18 1% 51E	5322 111 91352
R 8703	MCR18 1% 6K8	4822 111 90544
R 8704	MCR18 1% 68K	4822 111 90202
R 8706	MCR18 1% 51E	5322 111 91352
R 8707	MCR18 1% 470E	5322 111 90109
R 8708	MCR18 1% 51E	5322 111 91352
R 8709	MCR18 1% 200E	5322 116 80599
R 8711	MCR18 1% 100K	4822 111 90214
R 8712	MCR18 1% 10K	4822 111 90249
R 8713	MCR18 1% 6K8	4822 111 90544
R 8714	MCR18 1% 680E	4822 111 90162
R 8716	MCR18 1% 3K	5322 111 91351
R 8717	MCR18 1% 10K	4822 111 90249
R 8718	MCR18 1% 10K	4822 111 90249
R 8719	MCR18 1% 390E	5322 111 91205
R 9001	MRS25 1% 100E	5322 116 53126
R 9002	MRS25 1% 100E	5322 116 53126
R 9003	MRS25 1% 100E	5322 116 53126
R 9007	MRS25 1% 100E	5322 116 53126
R 9008	MRS25 1% 100E	5322 116 53126
R 9009	MRS25 1% 100E	5322 116 53126
R 9011	MRS25 1% 100E	5322 116 53126
R 9012	MRS25 1% 100E	5322 116 53126
R 9013	MRS25 1% 100E	5322 116 53126
R 9014	MRS25 1% 100E	5322 116 53126
R 9018	MRS25 1% 100E	5322 116 53126
R 9019	MRS25 1% 100E	5322 116 53126
R 9021	MRS25 1% 100E	5322 116 53126
R 9022	MRS25 1% 100E	5322 116 53126
R 9023	MRS25 1% 100E	5322 116 53126
R 9024	MRS25 1% 100E	5322 116 53126
R 9026	MRS25 1% 100E	5322 116 53126
R 9027	MRS25 1% 100E	5322 116 53126
R 9028	MRS25 1% 100E	5322 116 53126
R 9029	MRS25 1% 100E	5322 116 53126
R 9031	MRS25 1% 100E	5322 116 53126
R 9032	MRS25 1% 100E	5322 116 53126
R 9033	MRS25 1% 100E	5322 116 53126
R 9034	MRS25 1% 100E	5322 116 53126
R 9036	MRS25 1% 100E	5322 116 53126
R 9037	MRS25 1% 100E	5322 116 53126
R 9038	MRS25 1% 100E	5322 116 53126
R 9039	MRS25 1% 100E	5322 116 53126
R 9041	MRS25 1% 100E	5322 116 53126
R 9042	MRS25 1% 100E	5322 116 53126
R 9043	MRS25 1% 100E	5322 116 53126
R 9044	MRS25 1% 100E	5322 116 53126

POSNR	DESCRIPTION	ORDERING CODE
R 9046	MRS25 1% 100E	5322 116 53126
R 9201	MCR18 1% 51E	5322 111 91352
R 9202	MCR18 1% 51E	5322 111 91352
R 9203	30E 2% 0,125W	4822 111 90356
R 9204	30E 2% 0,125W	4822 111 90356
R 9206	30E 2% 0,125W	4822 111 90356
R 9207	30E 2% 0,125W	4822 111 90356
R 9208	MCR18 1% 680E	4822 111 90162
R 9209	MCR18 1% 680E	4822 111 90162
R 9211	MCR18 1% 680E	4822 111 90162
R 9212	MCR18 1% 680E	4822 111 90162
R 9251	MCR18 1% 47E	4822 111 90217
R 9252	MCR18 1% 47E	4822 111 90217
R 9253	MCR18 1% 750E	5322 111 91539
R 9254	MCR18 1% 750E	5322 111 91539
R 9256	MCR18 1% 270E	4822 111 90154
R 9257	MCR18 1% 270E	4822 111 90154
R 9258	MCR18 1% 15E	4822 111 90344
R 9259	MCR18 1% 15E	4822 111 90344
R 9261	MCR18 1% 51E	5322 111 91352
R 9262	MCR18 1% 51E	5322 111 91352
R 9263	MCR18 1% 18E	5322 111 90139
R 9264	MCR18 1% 18E	5322 111 90139
R 9266	RC-01 5% 5E6	4822 111 90394
R 9267	RC-01 5% 5E6	4822 111 90394
R 9268	MCR18 1% 20E	4822 111 90352
R 9269	MCR18 1% 20E	4822 111 90352
R 9271	MCR18 1% 120E	4822 111 90339
R 9272	MCR18 1% 120E	4822 111 90339
R 9273	MCR18 1% 470E	5322 111 90109
R 9274	MCR18 1% 470E	5322 111 90109
R 9276	MCR18 1% 10K	4822 111 90249
R 9277	MCR18 1% 10K	4822 111 90249
R 9278	30E 2% 0,125W	4822 111 90356
R 9279	30E 2% 0,125W	4822 111 90356
R 9281	MCR18 1% 51E	5322 111 91352
R 9282	MCR18 1% 51E	5322 111 91352
R 9283	MCR18 1% 10K	4822 111 90249
R 9284	MCR18 1% 10K	4822 111 90249
R 9286	MCR18 1% 100E	5322 111 91134
R 9287	RC-01 5% 4E7	5322 111 90376
R 9288	RC-01 5% 4E7	5322 111 90376
R 9289	MCR18 1% 10E	5322 111 90095
R 9291	MCR18 1% 200E	5322 116 80599
R 9292	MCR18 1% 1K2	5322 111 90096
R 9301	MCR18 1% 47E	4822 111 90217
R 9302	MCR18 1% 47E	4822 111 90217
R 9303	MCR18 1% 1K	5322 111 90092
R 9304	MCR18 1% 1K	5322 111 90092
R 9306	MCR18 1% 270E	4822 111 90154
R 9307	MCR18 1% 270E	4822 111 90154
R 9308	MCR18 1% 15E	4822 111 90344
R 9309	MCR18 1% 15E	4822 111 90344
R 9311	MCR18 1% 51E	5322 111 91352
R 9312	MCR18 1% 51E	5322 111 91352
R 9313	MCR18 1% 18E	5322 111 90139
R 9314	MCR18 1% 18E	5322 111 90139
R 9316	RC-01 5% 5E6	4822 111 90394
R 9317	RC-01 5% 5E6	4822 111 90394
R 9318	MCR18 1% 20E	4822 111 90352
R 9319	MCR18 1% 20E	4822 111 90352
R 9321	MCR18 1% 120E	4822 111 90339
R 9322	MCR18 1% 120E	4822 111 90339
R 9323	MCR18 1% 470E	5322 111 90109
R 9324	MCR18 1% 470E	5322 111 90109
R 9326	MCR18 1% 10K	4822 111 90249
R 9327	MCR18 1% 10K	4822 111 90249
R 9328	30E 2% 0,125W	4822 111 90356
R 9329	30E 2% 0,125W	4822 111 90356
R 9331	MCR18 1% 75E	4822 111 90371
R 9332	MCR18 1% 75E	4822 111 90371
R 9333	MCR18 1% 10K	4822 111 90249
R 9334	MCR18 1% 10K	4822 111 90249
R 9336	MCR18 1% 100E	5322 111 91134
R 9337	RC-01 5% 4E7	5322 111 90376
R 9338	RC-01 5% 4E7	5322 111 90376
R 9339	MCR18 1% 10E	5322 111 90095
R 9341	MCR18 1% 200E	5322 116 80599
R 9342	MCR18 1% 1K2	5322 111 90096
R 9343	MCR18 1% 51E	5322 111 91352
R 9344	MCR18 1% 15E	4822 111 90344
R 9351	MCR18 1% 47E	4822 111 90217
R 9352	MCR18 1% 47E	4822 111 90217
R 9353	MCR18 1% 750E	5322 111 91539
R 9354	MCR18 1% 750E	5322 111 91539
R 9356	MCR18 1% 270E	4822 111 90154
R 9357	MCR18 1% 270E	4822 111 90154
R 9358	MCR18 1% 15E	4822 111 90344
R 9359	MCR18 1% 15E	4822 111 90344
R 9361	MCR18 1% 51E	5322 111 91352
R 9362	MCR18 1% 51E	5322 111 91352

POSNR	DESCRIPTION		ORDERING CODE
R 9363	MCR18	1% 18E	5322 111 90139
R 9364	MCR18	1% 18E	5322 111 90139
R 9366	RC-01	5% 5E6	4822 111 90394
R 9367	RC-01	5% 5E6	4822 111 90394
R 9368	MCR18	1% 20E	4822 111 90352
R 9369	MCR18	1% 20E	4822 111 90352
R 9371	MCR18	1% 120E	4822 111 90339
R 9372	MCR18	1% 120E	4822 111 90339
R 9373	MCR18	1% 470E	5322 111 90109
R 9374	MCR18	1% 470E	5322 111 90109
R 9376	MCR18	1% 10K	4822 111 90249
R 9377	MCR18	1% 10K	4822 111 90249
R 9378	30E	2% 0,125W	4822 111 90356
R 9379	30E	2% 0,125W	4822 111 90356
R 9381	MCR18	1% 51E	5322 111 91352
R 9382	MCR18	1% 51E	5322 111 91352
R 9383	MCR18	1% 10K	4822 111 90249
R 9384	MCR18	1% 10K	4822 111 90249
R 9386	MCR18	1% 100E	5322 111 91134
R 9387	RC-01	5% 4E7	5322 111 90376
R 9388	RC-01	5% 4E7	5322 111 90376
R 9389	MCR18	1% 10E	5322 111 90095
R 9391	MCR18	1% 200E	5322 116 80599
R 9392	MCR18	1% 1K2	5322 111 90096
R 9401	MCR18	1% 51E	5322 111 91352
R 9402	MCR18	1% 51E	5322 111 91352
R 9403	30E	2% 0,125W	4822 111 90356
R 9404	30E	2% 0,125W	4822 111 90356
R 9406	30E	2% 0,125W	4822 111 90356
R 9407	30E	2% 0,125W	4822 111 90356
R 9408	MCR18	1% 680E	4822 111 90162
R 9409	MCR18	1% 680E	4822 111 90162
R 9411	MCR18	1% 680E	4822 111 90162
R 9412	MCR18	1% 680E	4822 111 90162
R 9451	MCR18	1% 47E	4822 111 90217
R 9452	MCR18	1% 47E	4822 111 90217
R 9453	MCR18	1% 750E	5322 111 91539
R 9454	MCR18	1% 750E	5322 111 91539
R 9456	MCR18	1% 270E	4822 111 90154
R 9457	MCR18	1% 270E	4822 111 90154
R 9458	MCR18	1% 15E	4822 111 90344
R 9459	MCR18	1% 15E	4822 111 90344
R 9461	MCR18	1% 51E	5322 111 91352
R 9462	MCR18	1% 51E	5322 111 91352
R 9463	MCR18	1% 18E	5322 111 90139
R 9464	MCR18	1% 18E	5322 111 90139
R 9466	RC-01	5% 5E6	4822 111 90394
R 9467	RC-01	5% 5E6	4822 111 90394
R 9468	MCR18	1% 20E	4822 111 90352
R 9469	MCR18	1% 20E	4822 111 90352
R 9471	MCR18	1% 120E	4822 111 90339
R 9472	MCR18	1% 120E	4822 111 90339
R 9473	MCR18	1% 470E	5322 111 90109
R 9474	MCR18	1% 470E	5322 111 90109
R 9476	MCR18	1% 10K	4822 111 90249
R 9477	MCR18	1% 10K	4822 111 90249
R 9478	30E	2% 0,125W	4822 111 90356
R 9479	30E	2% 0,125W	4822 111 90356
R 9481	MCR18	1% 51E	5322 111 91352
R 9482	MCR18	1% 51E	5322 111 91352
R 9483	MCR18	1% 10K	4822 111 90249
R 9484	MCR18	1% 10K	4822 111 90249
R 9486	MCR18	1% 100E	5322 111 91134
R 9487	RC-01	5% 4E7	5322 111 90376
R 9488	RC-01	5% 4E7	5322 111 90376
R 9489	MCR18	1% 10E	5322 111 90095
R 9491	MCR18	1% 200E	5322 116 80599
R 9492	MCR18	1% 1K2	5322 111 90096
R 9501	MCR18	1% 47E	4822 111 90217
R 9502	MCR18	1% 47E	4822 111 90217
R 9503	MCR18	1% 1K	5322 111 90092
R 9504	MCR18	1% 1K	5322 111 90092
R 9506	MCR18	1% 270E	4822 111 90154
R 9507	MCR18	1% 270E	4822 111 90154
R 9508	MCR18	1% 15E	4822 111 90344
R 9509	MCR18	1% 15E	4822 111 90344
R 9511	MCR18	1% 51E	5322 111 91352
R 9512	MCR18	1% 51E	5322 111 91352
R 9513	MCR18	1% 18E	5322 111 90139
R 9514	MCR18	1% 18E	5322 111 90139
R 9516	RC-01	5% 5E6	4822 111 90394
R 9517	RC-01	5% 5E6	4822 111 90394
R 9518	MCR18	1% 20E	4822 111 90352
R 9519	MCR18	1% 20E	4822 111 90352
R 9521	MCR18	1% 120E	4822 111 90339
R 9522	MCR18	1% 120E	4822 111 90339
R 9523	MCR18	1% 470E	5322 111 90109
R 9524	MCR18	1% 470E	5322 111 90109
R 9526	MCR18	1% 10K	4822 111 90249
R 9527	MCR18	1% 10K	4822 111 90249

POSNR	DESCRIPTION		ORDERING CODE
R 9529	30E	2% 0,125W	4822 111 90356
R 9531	MCR18	1% 75E	4822 111 90371
R 9532	MCR18	1% 75E	4822 111 90371
R 9533	MCR18	1% 10K	4822 111 90249
R 9534	MCR18	1% 10K	4822 111 90249
R 9536	MCR18	1% 100E	5322 111 91134
R 9537	RC-01	5% 4E7	5322 111 90376
R 9538	RC-01	5% 4E7	5322 111 90376
R 9539	MCR18	1% 10E	5322 111 90095
R 9541	MCR18	1% 200E	5322 116 80599
R 9542	MCR18	1% 1K2	5322 111 90096
R 9543	MCR18	1% 51E	5322 111 91352
R 9544	MCR18	1% 51E	5322 111 91352
R 9551	MCR18	1% 47E	4822 111 90217
R 9552	MCR18	1% 47E	4822 111 90217
R 9553	MCR18	1% 750E	5322 111 91539
R 9554	MCR18	1% 750E	5322 111 91539
R 9556	MCR18	1% 270E	4822 111 90154
R 9557	MCR18	1% 270E	4822 111 90154
R 9558	MCR18	1% 15E	4822 111 90344
R 9559	MCR18	1% 15E	4822 111 90344
R 9561	MCR18	1% 51E	5322 111 91352
R 9562	MCR18	1% 51E	5322 111 91352
R 9563	MCR18	1% 18E	5322 111 90139
R 9564	MCR18	1% 18E	5322 111 90139
R 9566	RC-01	5% 5E6	4822 111 90394
R 9567	RC-01	5% 5E6	4822 111 90394
R 9568	MCR18	1% 20E	4822 111 90352
R 9569	MCR18	1% 20E	4822 111 90352
R 9571	MCR18	1% 120E	4822 111 90339
R 9572	MCR18	1% 120E	4822 111 90339
R 9573	MCR18	1% 470E	5322 111 90109
R 9574	MCR18	1% 470E	5322 111 90109
R 9576	MCR18	1% 10K	4822 111 90249
R 9577	MCR18	1% 10K	4822 111 90249
R 9578	30E	2% 0,125W	4822 111 90356
R 9579	30E	2% 0,125W	4822 111 90356
R 9581	MCR18	1% 51E	5322 111 91352
R 9582	MCR18	1% 51E	5322 111 91352
R 9583	MCR18	1% 10K	4822 111 90249
R 9584	MCR18	1% 10K	4822 111 90249
R 9586	MCR18	1% 100E	5322 111 91134
R 9587	RC-01	5% 4E7	5322 111 90376
R 9588	RC-01	5% 4E7	5322 111 90376
R 9589	MCR18	1% 10E	5322 111 90095
R 9591	MCR18	1% 200E	5322 116 80599
R 9592	MCR18	1% 1K2	5322 111 90096
R 9601	MCR18	1% 10K	4822 111 90249
R 9602	MCR18	1% 10K	4822 111 90249

SEMICONDUCTORS

POSNR	DESCRIPTION		ORDERING CODE
V 0401	BAT82	PEL	4822 130 32964
V 0402	BAT82	PEL	4822 130 32964
V 0403	BZV12	PEL	5322 130 34269
V 0404	BAW62	PEL	4822 130 30613
V 0406	BAW62	PEL	4822 130 30613
V 0407	BZV86-C2V0	PEL	4822 130 81424
V 0408	BZV86-C2V0	PEL	4822 130 81424
V 0409	BZV86-C2V0	PEL	4822 130 81424
V 0411	BZV86-C2V0	PEL	4822 130 81424
V 0412	BAT82	PEL	4822 130 32964
V 0413	BAT82	PEL	4822 130 32964
V 0414	BAT82	PEL	4822 130 32964
V 0601	BFQ22S	PEL	5322 130 42031
V 0602	BFQ22S	PEL	5322 130 42031
V 0603	BC558B	PEL	4822 130 44197
V 0604	BFQ24	PEL	5322 130 41664
V 0606	BFQ24	PEL	5322 130 41664
V 0607	BFQ22S	PEL	5322 130 42031
V 0608	BFQ24	PEL	5322 130 41664
V 0609	BC558B	PEL	4822 130 44197
V 0611	BF199	PEL	4822 130 44154
V 0612	BC548C	PEL	4822 130 44196
V 0613	BZX79-C4V7	PEL	4822 130 34174
V 0614	BZX79-C4V7	PEL	4822 130 34174
V 0616	BZV86-C1V4	PEL	4822 130 81423
V 0617	BAW62	PEL	4822 130 30613
V 0618	BAW62	PEL	4822 130 30613
V 0619	BZX79-C5V1	PEL	4822 130 34233
V 0620	BZX79-C5V1	PEL	4822 130 34233
V 0621	BC558B	PEL	4822 130 44197
V 0622	BC548C	PEL	4822 130 44196
V 0623	BC548C	PEL	4822 130 44196

POSNR	DESCRIPTION		ORDERING CODE
V 0626	BSV78	PEL	5322 130 44093
V 1401	BSX20	PEL	4822 130 41705
V 1402	BSX20	PEL	4822 130 41705
V 1701	BZV86-C2V0	PEL	4822 130 81424
V 1702	BC548C	PEL	4822 130 44196
V 1703	BAW62	PEL	4822 130 30613
V 1704	BC548C	PEL	4822 130 44196
V 1706	BC548C	PEL	4822 130 44196
V 1707	BAT85	PEL	4822 130 31983
V 1708	BC558B	PEL	4822 130 44197
V 1709	BZX79-C3V9	PEL	4822 130 31981
V 1711	BC548C	PEL	4822 130 44196
V 1712	BD140	PEL	4822 130 40824
V 1713	BZX79-C3V9	PEL	4822 130 31981
V 1714	BAW62	PEL	4822 130 30613
V 1791	BAT85	PEL	4822 130 31983
V 1792	BAT85	PEL	4822 130 31983
V 1793	BAT85	PEL	4822 130 31983
V 1794	BAT85	PEL	4822 130 31983
V 1801	BAT85	PEL	4822 130 31983
V 1802	BAT85	PEL	4822 130 31983
V 1803	BAT85	PEL	4822 130 31983
V 1804	BAT85	PEL	4822 130 31983
V 2001	BSX20	PEL	4822 130 41705
V 2002	BSX20	PEL	4822 130 41705
V 2301	BC558B	PEL	4822 130 44197
V 2302	BC558B	PEL	4822 130 44197
V 2303	ON4057	PEL	5322 130 42366
V 2304	BC548C	PEL	4822 130 44196
V 2306	BSX20	PEL	4822 130 41705
V 2307	BC548C	PEL	4822 130 44196
V 2308	BSX20	PEL	4822 130 41705
V 2309	BC558B	PEL	4822 130 44197
V 2311	BC558B	PEL	4822 130 44197
V 2312	BZX79-C4V3	PEL	4822 130 31554
V 2317	ON4057	PEL	5322 130 42366
V 2318	BC548C	PEL	4822 130 44196
V 2321	BC548C	PEL	4822 130 44196
V 2323	BZV12	PEL	5322 130 34269
V 2501	BAW62	PEL	4822 130 30613
V 2502	BAW62	PEL	4822 130 30613
V 2503	BAW62	PEL	4822 130 30613
V 2506	BAW62	PEL	4822 130 30613
V 2507	BC548C	PEL	4822 130 44196
V 2508	BC558B	PEL	4822 130 44197
V 2509	BC548C	PEL	4822 130 44196
V 2511	BF199	PEL	4822 130 44154
V 2512	BF199	PEL	4822 130 44154
V 2513	BZV86-C1V4	PEL	4822 130 81423
V 2514	BZV86-C1V4	PEL	4822 130 81423
V 2516	BF199	PEL	4822 130 44154
V 2517	BF199	PEL	4822 130 44154
V 2521	BAW62	PEL	4822 130 30613
V 2522	BAW62	PEL	4822 130 30613
V 2523	BAW62	PEL	4822 130 30613
V 2524	BC548C	PEL	4822 130 44196
V 2526	BC558B	PEL	4822 130 44197
V 2527	BC548C	PEL	4822 130 44196
V 2528	BF422	PEL	4822 130 41782
V 2529	BF422	PEL	4822 130 41782
V 2531	BZV86-C1V4	PEL	4822 130 81423
V 2532	BZV86-C1V4	PEL	4822 130 81423
V 2533	BF422	PEL	4822 130 41782
V 2534	BF422	PEL	4822 130 41782
V 2535	BC558B	PEL	4822 130 44197
V 2601	BAW62	PEL	4822 130 30613
V 2602	BAW62	PEL	4822 130 30613
V 2604	BZV86-C1V4	PEL	4822 130 81423
V 2605	BAW62	PEL	4822 130 30613
V 2606	BF199	PEL	4822 130 44154
V 2607	BC548C	PEL	4822 130 44196
V 2608	BSX20	PEL	4822 130 41705
V 2609	BZV86-C1V4	PEL	4822 130 81423
V 2611	BC548C	PEL	4822 130 44196
V 2613	BC558B	PEL	4822 130 44197
V 2616	BZX79-C3V9	PEL	4822 130 31981
V 2623	BC558B	PEL	4822 130 44197
V 2626	BC558B	PEL	4822 130 44197
V 2627	BF199	PEL	4822 130 44154
V 2628	BSX20	PEL	4822 130 41705
V 2631	BF450	PEL	4822 130 44237
V 2632	BAT82	PEL	4822 130 32964
V 2633	BAT82	PEL	4822 130 32964
V 2634	BF450	PEL	4822 130 44237
V 2636	BF450	PEL	4822 130 44237
V 2637	BAT82	PEL	4822 130 32964
V 2638	BAT82	PEL	4822 130 32964
V 2639	BF450	PEL	4822 130 44237
V 2646	BF423	PEL	4822 130 41646
V 2647	BAV21	PEL	4822 130 30842

POSNR	DESCRIPTION		ORDERING CODE
V 2648	BAV21	PEL	4822 130 30842
V 2649	BF423	PEL	4822 130 41646
V 2651	BF423	PEL	4822 130 41646
V 2652	BAV21	PEL	4822 130 30842
V 2653	BAV21	PEL	4822 130 30842
V 2654	BF423	PEL	4822 130 41646
V 2662	BC548C	PEL	4822 130 44196
V 2663	BC558B	PEL	4822 130 44197
V 2664	BZX79-C4V7	PEL	4822 130 34174
V 2666	BZX79-C4V7	PEL	4822 130 34174
V 2671	BAT82	PEL	4822 130 32964
V 2674	BC548C	PEL	4822 130 44196
V 2676	BC548C	PEL	4822 130 44196
V 2677	BC548C	PEL	4822 130 44196
V 2681	BZX79-B33	PEL	4822 130 34142
V 2801	BF422	PEL	4822 130 41782
V 2802	BF422	PEL	4822 130 41782
V 2803	BF423	PEL	4822 130 41646
V 2804	BAV21	PEL	4822 130 30842
V 2806	BAV21	PEL	4822 130 30842
V 2807	BZX79-C8V2	PEL	4822 130 34382
V 2808	BF422	PEL	4822 130 41782
V 2809	BF422	PEL	4822 130 41782
V 2816	BF423	PEL	4822 130 41646
V 2817	BF423	PEL	4822 130 41646
V 2818	BF423	PEL	4822 130 41646
V 2819	BF423	PEL	4822 130 41646
V 2821	BAW62	PEL	4822 130 30613
V 2822	BAV21	PEL	4822 130 30842
V 3001	BC548C	PEL	4822 130 44196
V 3002	BC558B	PEL	4822 130 44197
V 3003	BD140	PEL	4822 130 40824
V 4201	BAW62	PEL	4822 130 30613
V 4202	BAW62	PEL	4822 130 30613
V 4203	BAW62	PEL	4822 130 30613
V 4204	BAW62	PEL	4822 130 30613
V 4206	BAW62	PEL	4822 130 30613
V 4207	BAW62	PEL	4822 130 30613
V 4208	BAW62	PEL	4822 130 30613
V 4209	BAW62	PEL	4822 130 30613
V 4211	BAW62	PEL	4822 130 30613
V 4212	BAW62	PEL	4822 130 30613
V 4213	BAW62	PEL	4822 130 30613
V 4214	BAW62	PEL	4822 130 30613
V 4216	BAW62	PEL	4822 130 30613
V 4217	BAW62	PEL	4822 130 30613
V 4218	BAW62	PEL	4822 130 30613
V 4219	BAW62	PEL	4822 130 30613
V 4221	BAW62	PEL	4822 130 30613
V 4222	BAW62	PEL	4822 130 30613
V 4223	BAW62	PEL	4822 130 30613
V 4224	BAW62	PEL	4822 130 30613
V 4226	BAW62	PEL	4822 130 30613
V 4227	BAW62	PEL	4822 130 30613
V 4228	BAW62	PEL	4822 130 30613
V 4229	BAW62	PEL	4822 130 30613
V 4231	BAW62	PEL	4822 130 30613
V 4232	BAW62	PEL	4822 130 30613
V 4233	BAW62	PEL	4822 130 30613
V 4234	BAW62	PEL	4822 130 30613
V 4236	BAW62	PEL	4822 130 30613
V 4237	BAW62	PEL	4822 130 30613
V 4238	BAW62	PEL	4822 130 30613
V 4239	BAW62	PEL	4822 130 30613
V 4241	BAW62	PEL	4822 130 30613
V 4242	BAW62	PEL	4822 130 30613
V 4243	BAW62	PEL	4822 130 30613
V 4244	BAW62	PEL	4822 130 30613
V 4246	BAW62	PEL	4822 130 30613
V 4247	BAW62	PEL	4822 130 30613
V 4248	BAW62	PEL	4822 130 30613
V 4249	BAW62	PEL	4822 130 30613
V 4251	BAW62	PEL	4822 130 30613
V 4252	BAW62	PEL	4822 130 30613
V 4253	BAW62	PEL	4822 130 30613
V 4254	BAW62	PEL	4822 130 30613
V 4256	BAW62	PEL	4822 130 30613
V 4257	BAW62	PEL	4822 130 30613
V 4258	BAW62	PEL	4822 130 30613
V 4401	BYM56E	PEL	4822 130 80254
V 4402	BYM56E	PEL	4822 130 80254
V 4403	BYM56E	PEL	4822 130 80254
V 4404	BYM56E	PEL	4822 130 80254
V 4406	BF423	PEL	4822 130 41646
V 4407	BF423	PEL	4822 130 41646
V 4408	BF423	PEL	4822 130 41646
V 4409	BZX79-C15	PEL	4822 130 34281
V 4411	BYW56	PEL	5322 130 34973
V 4412	BYW56	PEL	5322 130 34973
V 4414	BT149-E	PEL	5322 130 80268
V 4416	BT149-E	PEL	5322 130 80268

POSNR	DESCRIPTION		ORDERING CODE
V 4418	BYV26C	PEL	4822 130 32343
V 4419	BYV28-150	PEL	5322 130 32043
V 4422	BYV26C	PEL	4822 130 32343
V 4423	BYV26C	PEL	4822 130 32343
V 4427	BZX79-C15	PEL	4822 130 34281
V 4428	BYV26C	PEL	4822 130 32343
V 4431	BYV27-150	PEL	4822 130 31628
V 4433	BC337	PEL	4822 130 40855
V 4434	BAX12	PEL	5322 130 34605
V 4436	BZX79-C3V6	PEL	5322 130 34834
V 4437	BAX12	PEL	5322 130 34605
V 4438	BAX12	PEL	5322 130 34605
V 4439	BZX79-C15	PEL	4822 130 34281
V 4441	BRY39	PEL	5322 130 40482
V 4442	BAX12	PEL	5322 130 34605
V 4443	BZX79-C5V6	PEL	4822 130 34173
V 4444	BZT03-C220	PEL	5322 130 80269
V 4446	BZT03-C220	PEL	5322 130 80269
V 4447	MBR2545CT	MOT	5322 130 81179
V 4448	MBR2545CT	MOT	5322 130 81179
V 4449	BYV95C	PEL	4822 130 41487
V 4451	BYV95C	PEL	4822 130 41487
V 4452	BYV95C	PEL	4822 130 41487
V 4453	BYV95C	PEL	4822 130 41487
V 4454	BYV95C	PEL	4822 130 41487
V 4455	BYV19-45	PEL	5322 130 32703
V 4456	BYV19-45	PEL	5322 130 32703
V 4457	BYV19-45	PEL	5322 130 32703
V 4459	BAX12	PEL	5322 130 34605
V 4461	BYV28-150	PEL	5322 130 32043
V 4462	BYV28-150	PEL	5322 130 32043
V 4463	BYV28-150	PEL	5322 130 32043
V 4464	BYV28-150	PEL	5322 130 32043
V 4466	BYV95C	PEL	4822 130 41487
V 4467	BYV95C	PEL	4822 130 41487
V 4468	BYV95C	PEL	4822 130 41487
V 4469	BYV95C	PEL	4822 130 41487
V 4471	BZX79-C7V5	PEL	4822 130 30861
V 4472	BAX12	PEL	5322 130 34605
V 4473	BC548C	PEL	4822 130 44196
V 4474	BC327	PEL	4822 130 40854
V 4475	BAX12	PEL	5322 130 34605
V 4476	BC548C	PEL	4822 130 44196
V 4477	BAX12	PEL	5322 130 34605
V 4478	BZX79-C4V7	PEL	4822 130 34174
V 4479	BZX79-C15	PEL	4822 130 34281
V 4481	BAX12	PEL	5322 130 34605
V 4482	BZX79-C9V1	PEL	4822 130 30862
V 4483	BAX12	PEL	5322 130 34605
V 4484	BAX12	PEL	5322 130 34605
V 4486	BC327	PEL	4822 130 40854
V 4601	BZV12	PEL	5322 130 34269
V 4602	BAX12	PEL	5322 130 34605
V 4603	BC337	PEL	4822 130 40855
V 4604	BZX79-C22	PEL	4822 130 34441
V 4606	BAV21	PEL	4822 130 30842
V 4607	BAV21	PEL	4822 130 30842
V 4608	BC327	PEL	4822 130 40854
V 4609	BAV21	PEL	4822 130 30842
V 4611	BYV27-150	PEL	4822 130 31628
V 4612	BUV26A	PEL	5322 130 42722
V 4613	BY509	PEL	4822 130 41485
V 4616	BAX12	PEL	5322 130 34605
V 4617	BSV78	PEL	5322 130 44093
V 4618	BZX79-C18	PEL	4822 130 80234
V 4619	BAX12	PEL	5322 130 34605
V 4621	BC639	PEL	4822 130 41053
V 4622	BD139	PEL	4822 130 40823
V 4623	BZX79-B27	PEL	4822 130 34379
V 4624	BAT85	PEL	4822 130 31983
V 4701	BF512	PEL	5322 130 44875
V 4702	BAS45	PEL	5322 130 32256
V 4703	BFR92	PEL	5322 130 42145
V 4704	BAV70	PEL	5322 130 34331
V 4706	BF512	PEL	4822 130 44875
V 4707	BFR92R	PEL	5322 130 44606
V 4708	BAW56	PEL	5322 130 30691
V 4709	BFR92R	PEL	5322 130 44606
V 4711	BFT92R	PEL	5322 130 44713
V 4712	BAW56	PEL	5322 130 30691
V 4713	BFR92R	PEL	5322 130 44606
V 4714	BCW30R	PEL	5322 130 44341
V 4717	BFT92R	PEL	5322 130 44713
V 4718	BFQ19	PEL	4822 130 42707
V 4719	BCW33R	PEL	5322 130 44342
V 4721	BFR92	PEL	5322 130 42145
V 4722	BFR92	PEL	5322 130 42145
V 4723	BFR92	PEL	5322 130 42145
V 4724	BFR92R	PEL	5322 130 44606
V 4726	BCW33	PEL	5322 130 44337
V 4727	BAV70	PEL	5322 130 34331

POSNR	DESCRIPTION		ORDERING CODE
V 4728	BCW30	PEL	5322 130 44335
V 4729	BAV70	PEL	5322 130 34331
V 4731	BCW30R	PEL	5322 130 44341
V 4733	BAW62	PEL	4822 130 30613
V 4734	BSV80	PEL	5322 130 34044
V 4736	BSV80	PEL	5322 130 34044
V 4737	BSV80	PEL	5322 130 34044
V 4738	BSV80	PEL	5322 130 34044
V 4739	BSV80	PEL	5322 130 34044
V 4741	BSV80	PEL	5322 130 34044
V 4742	BC558B	PEL	4822 130 44197
V 4743	BAW62	PEL	4822 130 30613
V 4744	BAW62	PEL	4822 130 30613
V 4746	BAW62	PEL	4822 130 30613
V 4747	BAW62	PEL	4822 130 30613
V 4748	BC548C	PEL	4822 130 44196
V 4801	BF512	PEL	5322 130 44875
V 4802	BAS45	PEL	5322 130 32256
V 4803	BFR92R	PEL	5322 130 44606
V 4804	BAV70	PEL	5322 130 34331
V 4806	BF512	PEL	5322 130 44875
V 4807	BFR92	PEL	5322 130 42145
V 4808	BAW56	PEL	5322 130 30691
V 4809	BFR92	PEL	5322 130 42145
V 4811	BFT92	PEL	5322 130 44711
V 4812	BAW56	PEL	5322 130 30691
V 4813	BFR92	PEL	5322 130 42145
V 4817	BFT92	PEL	5322 130 44711
V 4818	BFQ19R	PEL	5322 130 42719
V 4819	BCW33	PEL	5322 130 44337
V 4821	BFR92R	PEL	5322 130 44606
V 4822	BFR92R	PEL	5322 130 44606
V 4823	BFR92R	PEL	5322 130 44606
V 4824	BFR92	PEL	5322 130 42145
V 4826	BCW33R	PEL	5322 130 44342
V 4827	BAV70	PEL	5322 130 34331
V 4828	BCW30R	PEL	5322 130 44341
V 4831	BCW30	PEL	5322 130 44335
V 4832	BAW62	PEL	4822 130 30613
V 4833	BAW62	PEL	4822 130 30613
V 4837	BSV80	PEL	5322 130 34044
V 4838	BSV80	PEL	5322 130 34044
V 4841	BSV80	PEL	5322 130 34044
V 4842	BC558B	PEL	4822 130 44197
V 4846	BAW62	PEL	4822 130 30613
V 5001	BZV12	PEL	5322 130 34269
V 5002	BC548C	PEL	4822 130 44196
V 5003	BC548C	PEL	4822 130 44196
V 5004	BC558B	PEL	4822 130 44197
V 5005	BC558B	PEL	4822 130 44197
V 5006	BC548C	PEL	4822 130 44196
V 5007	BC558B	PEL	4822 130 44197
V 5008	BC548C	PEL	4822 130 44196
V 5009	BZV12	PEL	5322 130 34269
V 5011	BAW62	PEL	4822 130 30613
V 5012	BAW62	PEL	4822 130 30613
V 5013	BC558B	PEL	4822 130 44197
V 5014	BC558B	PEL	4822 130 44197
V 5101	BZV12	PEL	5322 130 34269
V 5102	BC548C	PEL	4822 130 44196
V 5103	BC548C	PEL	4822 130 44196
V 5104	BC558B	PEL	4822 130 44197
V 5105	BC558B	PEL	4822 130 44197
V 5106	BC548C	PEL	4822 130 44196
V 5107	BC558B	PEL	4822 130 44197
V 5108	BC548C	PEL	4822 130 44196
V 5109	BZV12	PEL	5322 130 34269
V 5111	BAW62	PEL	4822 130 30613
V 5112	BAW62	PEL	4822 130 30613
V 5113	BC558B	PEL	4822 130 44197
V 5114	BC558B	PEL	4822 130 44197
V 5201	BC558B	PEL	4822 130 44197
V 5202	BC558B	PEL	4822 130 44197
V 5203	BC558B	PEL	4822 130 44197
V 5204	BC558B	PEL	4822 130 44197
V 5206	BC548C	PEL	4822 130 44196
V 5401	BZX84-C15	PEL	5322 130 33662
V 5402	BZX84-C15	PEL	5322 130 33662
V 5441	BZX84-C15	PEL	5322 130 33662
V 5442	BZX84-C15	PEL	5322 130 33662
V 6001	BC548C	PEL	4822 130 44196
V 6002	BC548C	PEL	4822 130 44196
V 6003	BAW62	PEL	4822 130 30613
V 6004	BC548C	PEL	4822 130 44196
V 6005	BC558B	PEL	4822 130 44197
V 6006	BC558B	PEL	4822 130 44197
V 6007	BAW62	PEL	4822 130 30613
V 6008	BFQ22S	PEL	5322 130 42031
V 6009	BFQ24	PEL	5322 130 41664
V 6010	BAW62	PEL	4822 130 30613

POSNR	DESCRIPTION		ORDERING CODE
V 6011	BAW62	PEL	4822 130 30613
V 6012	BFQ22S	PEL	5322 130 42031
V 6013	BFQ24	PEL	5322 130 41664
V 6014	BAW62	PEL	4822 130 30613
V 6015	BAW62	PEL	4822 130 30613
V 6016	BFQ22S	PEL	5322 130 42031
V 6017	BFQ24	PEL	5322 130 41664
V 6018	BAT82	PEL	4822 130 32964
V 6019	BAT82	PEL	4822 130 32964
V 6020	BAT82	PEL	4822 130 32964
V 6021	BAT82	PEL	4822 130 32964
V 6401	BCW33	PEL	5322 130 44337
V 6402	BCW33	PEL	5322 130 44337
V 6403	BCW30	PEL	5322 130 44335
V 6406	BCW33	PEL	5322 130 44337
V 6407	BCW33	PEL	5322 130 44337
V 6408	BCW33	PEL	5322 130 44337
V 6409	BCW33	PEL	5322 130 44337
V 6411	BAW56	PEL	5322 130 30691
V 6412	BAW56	PEL	5322 130 30691
V 6413	BCW33	PEL	5322 130 44337
V 6414	BCW33	PEL	5322 130 44337
V 6416	BCW30	PEL	5322 130 44335
V 6417	BCW30	PEL	5322 130 44335
V 6418	BCW30	PEL	5322 130 44335
V 6801	BF512	PEL	5322 130 44875
V 6802	BCW30	PEL	5322 130 44335
V 6803	BFR92	PEL	5322 130 42145
V 6804	BAS45	PEL	5322 130 32256
V 6806	BF512	PEL	5322 130 44875
V 6807	BCW30R	PEL	5322 130 44341
V 6808	BAT17	PEL	5322 130 31544
V 6809	BFR92	PEL	5322 130 42145
V 6811	BAV70	PEL	5322 130 34331
V 6812	BAV70	PEL	5322 130 34331
V 6813	BAS45	PEL	5322 130 32256
V 6814	BF512	PEL	5322 130 44875
V 6816	BCW30	PEL	5322 130 44335
V 6817	BFR92R	PEL	5322 130 44606
V 6818	BFR92	PEL	5322 130 42145
V 6819	BFR93R	PEL	5322 130 44802
V 6821	BAV70	PEL	5322 130 34331
V 6822	BFR92R	PEL	5322 130 44606
V 6823	BFS20	PEL	5322 130 42718
V 6824	BCW33R	PEL	5322 130 44342
V 6826	BCW33R	PEL	5322 130 44342
V 6827	BCW30R	PEL	5322 130 44341
V 6828	BCW30R	PEL	5322 130 44341
V 6829	BFR93	PEL	5322 130 44801
V 6831	BAV70	PEL	5322 130 34331
V 6833	BFT93	PEL	5322 130 44824
V 6834	BAW56	PEL	5322 130 30691
V 6836	BFS20R	PEL	5322 130 44177
V 6837	BFT92	PEL	5322 130 44711
V 6838	BAV99	PEL	5322 130 34337
V 6839	BFQ19	PEL	4822 130 42707
V 6841	BSR56	PEL	4822 130 42633
V 6842	BSR56	PEL	4822 130 42633
V 6843	BAV70	PEL	5322 130 34331
V 6846	BCW30	PEL	5322 130 44335
V 6901	BAW62	PEL	4822 130 30613
V 6902	BAW62	PEL	4822 130 30613
V 6903	BSV81	PEL	5322 130 44041
V 6904	BSV81	PEL	5322 130 44041
V 6906	BSV80	PEL	5322 130 34044
V 6907	BSV80	PEL	5322 130 34044
V 6909	BC558B	PEL	4822 130 44197
V 6911	BSV81	PEL	5322 130 44041
V 6912	BSV80	PEL	5322 130 34044
V 6913	BSV80	PEL	5322 130 34044
V 6914	BZX79-C9V1	PEL	4822 130 30862
V 7001	BZX79-C3V9	PEL	4822 130 31981
V 7002	BCY88	PEL	5322 130 41805
V 7003	BC558B	PEL	4822 130 44197
V 7004	BC558B	PEL	4822 130 44197
V 7006	BAW62	PEL	4822 130 30613
V 7007	BC558B	PEL	4822 130 44197
V 7008	BC558B	PEL	4822 130 44197
V 7009	BZX79-C15	PEL	4822 130 34281
V 7011	BC548C	PEL	4822 130 44196
V 7012	BF450	PEL	4822 130 44237
V 7013	BF450	PEL	4822 130 44237
V 7017	BAW62	PEL	4822 130 30613
V 7018	BC558B	PEL	4822 130 44197
V 7019	BC558B	PEL	4822 130 44197
V 7021	BC558B	PEL	4822 130 44197
V 7022	BC558B	PEL	4822 130 44197
V 7023	BC558B	PEL	4822 130 44197
V 7024	BC558B	PEL	4822 130 44197
V 7026	BCY88	PEL	5322 130 41805
V 7027	BC548C	PEL	4822 130 44196

POSNR	DESCRIPTION		ORDERING CODE
V 7028	BC548C	PEL	4822 130 44196
V 7029	BC548C	PEL	4822 130 44196
V 7031	BC558B	PEL	4822 130 44197
V 7032	BC558B	PEL	4822 130 44197
V 7033	BZV12	PEL	5322 130 34269
V 7034	BCY88	PEL	5322 130 41805
V 7036	BZV12	PEL	5322 130 34269
V 7037	BC548C	PEL	4822 130 44196
V 7038	BC558B	PEL	4822 130 44197
V 7039	BC558B	PEL	4822 130 44197
V 7201	BFT92	PEL	5322 130 44711
V 7202	BFT92	PEL	5322 130 44711
V 7203	BAW56	PEL	5322 130 30691
V 7204	BFT92	PEL	5322 130 44711
V 7206	BFT92	PEL	5322 130 44711
V 7251	BFT92	PEL	5322 130 44711
V 7252	BFT92	PEL	5322 130 44711
V 7253	BFR92	PEL	5322 130 42145
V 7254	BFR92	PEL	5322 130 42145
V 7257	BFT92	PEL	5322 130 44711
V 7258	BFT92	PEL	5322 130 44711
V 7259	BFR92	PEL	5322 130 42145
V 7261	BFR92	PEL	5322 130 42145
V 7401	BFT92	PEL	5322 130 44711
V 7402	BFT92	PEL	5322 130 44711
V 7403	BFR92	PEL	5322 130 42145
V 7404	BFR92	PEL	5322 130 42145
V 7501	BC548C	PEL	4822 130 44196
V 7502	BFR92	PEL	5322 130 42145
V 7503	BFR92R	PEL	5322 130 44606
V 7504	BZX79-C3V3	PEL	5322 130 31504
V 7506	BAW62	PEL	4822 130 30613
V 7507	BAW62	PEL	4822 130 30613
V 7508	BZX79-C6V2	PEL	4822 130 34167
V 7509	BZX79-C6V2	PEL	4822 130 34167
V 7511	BFQ24	PEL	5322 130 41664
V 7512	BFQ24	PEL	5322 130 41664
V 7513	BFQ24	PEL	5322 130 41664
V 7514	BFQ24	PEL	5322 130 41664
V 7516	BZX79-C3V3	PEL	5322 130 31504
V 7517	BAW62	PEL	4822 130 30613
V 7518	BAW62	PEL	4822 130 30613
V 7519	BZX79-C6V2	PEL	4822 130 34167
V 7521	BZX79-C6V2	PEL	4822 130 34167
V 7522	BC558B	PEL	4822 130 44197
V 7523	BC548C	PEL	4822 130 44196
V 7524	BZV86-C1V4	PEL	4822 130 81423
V 7526	BAW62	PEL	4822 130 30613
V 7527	BAW62	PEL	4822 130 30613
V 7528	BAW62	PEL	4822 130 30613
V 7529	BAW62	PEL	4822 130 30613
V 7531	BZX79-C3V9	PEL	4822 130 31981
V 7532	BZX79-C3V9	PEL	4822 130 31981
V 7533	BAW62	PEL	4822 130 30613
V 7534	BAW62	PEL	4822 130 30613
V 7536	BAW62	PEL	4822 130 30613
V 7537	BAW62	PEL	4822 130 30613
V 7538	BAW62	PEL	4822 130 30613
V 7539	BAW62	PEL	4822 130 30613
V 7541	BAW62	PEL	4822 130 30613
V 7542	BAW62	PEL	4822 130 30613
V 7543	BAW62	PEL	4822 130 30613
V 7544	BAW62	PEL	4822 130 30613
V 7546	BAW62	PEL	4822 130 30613
V 7547	BAW62	PEL	4822 130 30613
V 7548	BAW62	PEL	4822 130 30613
V 7549	BAW62	PEL	4822 130 30613
V 7551	BAW62	PEL	4822 130 30613
V 7552	BAW62	PEL	4822 130 30613
V 7553	BAW62	PEL	4822 130 30613
V 7554	BAW62	PEL	4822 130 30613
V 7556	BC558B	PEL	4822 130 44197
V 7557	BZV86-C2V0	PEL	4822 130 81424
V 7558	BZV86-C2V0	PEL	4822 130 81424
V 7559	BAW62	PEL	4822 130 30613
V 7561	BZX79-C4V7	PEL	4822 130 34174
V 7562	BC558B	PEL	4822 130 44197
V 7563	BC558B	PEL	4822 130 44197
V 7701	BC548C	PEL	4822 130 44196
V 7702	BFR92	PEL	5322 130 42145
V 7703	BFR92R	PEL	5322 130 44606
V 7704	BZX79-C3V3	PEL	5322 130 31504
V 7706	BAW62	PEL	4822 130 30613
V 7707	BAW62	PEL	4822 130 30613
V 7708	BZX79-C6V2	PEL	4822 130 34167
V 7709	BZX79-C6V2	PEL	4822 130 34167
V 7711	BFQ24	PEL	5322 130 41664
V 7712	BFQ24	PEL	5322 130 41664
V 7713	BFQ24	PEL	5322 130 41664
V 7714	BFQ24	PEL	5322 130 41664
V 7716	BZX79-C3V3	PEL	5322 130 31504

POSNR	DESCRIPTION		ORDERING CODE
V 7717	BAW62	PEL	4822 130 30613
V 7718	BAW62	PEL	4822 130 30613
V 7719	BZX79-C6V2	PEL	4822 130 34167
V 7721	BZX79-C6V2	PEL	4822 130 34167
V 7724	BZV86-C1V4	PEL	4822 130 81423
V 7726	BAW62	PEL	4822 130 30613
V 7727	BAW62	PEL	4822 130 30613
V 7728	BAW62	PEL	4822 130 30613
V 7729	BAW62	PEL	4822 130 30613
V 7731	BZX79-C3V9	PEL	4822 130 31981
V 7732	BZX79-C3V9	PEL	4822 130 31981
V 7733	BAW62	PEL	4822 130 30613
V 7734	BAW62	PEL	4822 130 30613
V 7736	BAW62	PEL	4822 130 30613
V 7737	BAW62	PEL	4822 130 30613
V 7738	BAW62	PEL	4822 130 30613
V 7739	BAW62	PEL	4822 130 30613
V 7741	BAW62	PEL	4822 130 30613
V 7742	BAW62	PEL	4822 130 30613
V 7743	BAW62	PEL	4822 130 30613
V 7744	BAW62	PEL	4822 130 30613
V 7746	BAW62	PEL	4822 130 30613
V 7747	BAW62	PEL	4822 130 30613
V 7748	BAW62	PEL	4822 130 30613
V 7749	BAW62	PEL	4822 130 30613
V 7751	BAW62	PEL	4822 130 30613
V 7752	BAW62	PEL	4822 130 30613
V 7753	BAW62	PEL	4822 130 30613
V 7754	BAW62	PEL	4822 130 30613
V 7757	BZV86-C2V0	PEL	4822 130 81424
V 7758	BZV86-C2V0	PEL	4822 130 81424
V 7759	BAW62	PEL	4822 130 30613
V 7851	BZV86-C2V0	PEL	4822 130 81424
V 7918	BZV12	PEL	5322 130 34269
V 7919	BCW30R	PEL	5322 130 44341
V 7922	BCW30R	PEL	5322 130 44341
V 7924	BZV12	PEL	5322 130 34269
V 7926	BCW30	PEL	5322 130 44335
V 7927	BCW30R	PEL	5322 130 44341
V 7928	BCW30R	PEL	5322 130 44341
V 8001	BF550	PEL	4822 130 42131
V 8002	BCW33	PEL	5322 130 44337
V 8003	BFT92	PEL	5322 130 44711
V 8004	BSV52	PEL	5322 130 44336
V 8041	BF550	PEL	4822 130 42131
V 8042	BCW33	PEL	5322 130 44337
V 8043	BFT92R	PEL	5322 130 44713
V 8101	BZV86-C2V0	PEL	4822 130 81424
V 8118	BZV12	PEL	5322 130 34269
V 8119	BCW30R	PEL	5322 130 44341
V 8122	BCW30R	PEL	5322 130 44341
V 8124	BZV12	PEL	5322 130 34269
V 8126	BCW30	PEL	5322 130 44335
V 8127	BCW30R	PEL	5322 130 44341
V 8128	BCW30R	PEL	5322 130 44341
V 8201	BF550	PEL	4822 130 42131
V 8202	BCW33	PEL	5322 130 44337
V 8203	BFT92	PEL	5322 130 44711
V 8204	BSV52	PEL	5322 130 44336
V 8241	BF550	PEL	4822 130 42131
V 8242	BCW33	PEL	5322 130 44337
V 8243	BFT92R	PEL	5322 130 44713
V 8301	BZV86-C2V0	PEL	4822 130 81424
V 8309	BZV86-C2V0	PEL	4822 130 81424
V 8310	BZV86-C2V0	PEL	4822 130 81424
V 8311	BCW33R	PEL	5322 130 44342
V 8312	BCW33R	PEL	5322 130 44342
V 8313	BZV12	PEL	5322 130 34269
V 8314	BZV86-C2V0	PEL	4822 130 81424
V 8316	BCW33R	PEL	5322 130 44342
V 8317	BCW33	PEL	5322 130 44337
V 8318	BCW33	PEL	5322 130 44337
V 8319	BCW33R	PEL	5322 130 44342
V 8321	BCW33R	PEL	5322 130 44342
V 8322	BCW33	PEL	5322 130 44337
V 8323	BCW33	PEL	5322 130 44337
V 8324	BCW33R	PEL	5322 130 44342
V 8327	BCW33R	PEL	5322 130 44342
V 8331	BCW33	PEL	5322 130 44337
V 8332	BCW33	PEL	5322 130 44337
V 8351	BCW33R	PEL	5322 130 44342
V 8352	BCW33R	PEL	5322 130 44342
V 8371	BCW33	PEL	5322 130 44337
V 8372	BCW33	PEL	5322 130 44337
V 8501	BFQ22S	PEL	5322 130 42031
V 8502	BFQ22S	PEL	5322 130 42031
V 8503	BFQ22S	PEL	5322 130 42031
V 8504	BFQ22S	PEL	5322 130 42031
V 8506	BF410C	PEL	4822 130 41482
V 8507	BAW62	PEL	4822 130 30613

POSNR	DESCRIPTION		ORDERING CODE
V 8509	BAW62	PEL	4822 130 30613
V 8511	BZV12	PEL	5322 130 34269
V 8512	BF199	PEL	4822 130 44154
V 8513	BAW62	PEL	4822 130 30613
V 8514	BFQ24	PEL	5322 130 41664
V 8515	BZX79-C6V2	PEL	4822 130 34167
V 8516	BFQ24	PEL	5322 130 41664
V 8517	BC558B	PEL	4822 130 44197
V 8518	BC558B	PEL	4822 130 44197
V 8519	BZX79-C6V2	PEL	4822 130 34167
V 8521	BC548C	PEL	4822 130 44196
V 8522	BC548C	PEL	4822 130 44196
V 8523	BC548C	PEL	4822 130 44196
V 8524	BC548C	PEL	4822 130 44196
V 8534	BC558B	PEL	4822 130 44197
V 8536	BZV86-C2V0	PEL	4822 130 81424
V 8537	BZV86-C1V4	PEL	4822 130 81423
V 8538	BAW62	PEL	4822 130 30613
V 8539	BAW62	PEL	4822 130 30613
V 8541	BFQ22S	PEL	5322 130 42031
V 8542	BF370	PEL	4822 130 42589
V 8543	BC558B	PEL	4822 130 44197
V 8544	BZV86-C2V0	PEL	4822 130 81424
V 8546	BZV86-C1V4	PEL	4822 130 81423
V 8547	BAW62	PEL	4822 130 30613
V 8548	BAW62	PEL	4822 130 30613
V 8549	BFQ22S	PEL	5322 130 42031
V 8551	BF370	PEL	4822 130 42589
V 8552	BZV86-C2V0	PEL	4822 130 81424
V 8553	BZV86-C2V0	PEL	4822 130 81424
V 8554	BC558B	PEL	4822 130 44197
V 8556	BC558B	PEL	4822 130 44197
V 8701	BFR92R	PEL	5322 130 44606
V 8702	BF991	PEL	5322 130 61707
V 8703	BFQ67	PEL	5322 130 42567
V 8704	BAT17	PEL	5322 130 31544
V 8706	BAV99	PEL	5322 130 34337
V 8707	BCW30	PEL	5322 130 44335
V 8707	BCW30	PEL	5322 130 44335
V 8708	BAT17	PEL	5322 130 31544
V 8709	BAT17	PEL	5322 130 31544
V 9201	BFQ19	PEL	4822 130 42707
V 9202	BFQ19	PEL	4822 130 42707
V 9203	BFQ19	PEL	4822 130 42707
V 9204	BFQ19	PEL	4822 130 42707
V 9251	BFG32	PEL	5322 130 61711
V 9252	BFG32	PEL	5322 130 61711
V 9253	BFG195	PEL	5322 130 61712
V 9254	BFG195	PEL	5322 130 61712
V 9256	BLU98	PEL	5322 130 61709
V 9257	BLU98	PEL	5322 130 61709
V 9258	BCX54-10	PEL	5322 130 61708
V 9259	BCX54-10	PEL	5322 130 61708
V 9301	BFG32	PEL	5322 130 61711
V 9302	BFG32	PEL	5322 130 61711
V 9303	BFG195	PEL	5322 130 61712
V 9304	BFG195	PEL	5322 130 61712
V 9306	BLU98	PEL	5322 130 61709
V 9307	BLU98	PEL	5322 130 61709
V 9308	BCX54-10	PEL	5322 130 61708
V 9309	BCX54-10	PEL	5322 130 61708
V 9351	BFG32	PEL	5322 130 61711
V 9352	BFG32	PEL	5322 130 61711
V 9353	BFG195	PEL	5322 130 61712
V 9354	BFG195	PEL	5322 130 61712
V 9356	BLU98	PEL	5322 130 61709
V 9357	BLU98	PEL	5322 130 61709
V 9358	BCX54-10	PEL	5322 130 61708
V 9359	BCX54-10	PEL	5322 130 61708
V 9401	BFQ19R	PEL	5322 130 42719
V 9402	BFQ19R	PEL	5322 130 42719
V 9403	BFQ19R	PEL	5322 130 42719
V 9404	BFQ19R	PEL	5322 130 42719
V 9451	BFG32	PEL	5322 130 61711
V 9452	BFG32	PEL	5322 130 61711
V 9453	BFG195	PEL	5322 130 61712
V 9454	BFG195	PEL	5322 130 61712
V 9456	BLU98	PEL	5322 130 61709
V 9457	BLU98	PEL	5322 130 61709
V 9458	BCX54-10	PEL	5322 130 61708
V 9459	BCX54-10	PEL	5322 130 61708
V 9501	BFG32	PEL	5322 130 61711
V 9502	BFG32	PEL	5322 130 61711
V 9503	BFG195	PEL	5322 130 61712
V 9504	BFG195	PEL	5322 130 61712
V 9506	BLU98	PEL	5322 130 61709
V 9507	BLU98	PEL	5322 130 61709
V 9508	BCX54-10	PEL	5322 130 61708
V 9509	BCX54-10	PEL	5322 130 61708
V 9551	BFG32	PEL	5322 130 61711
V 9552	BFG32	PEL	5322 130 61711

POSNR	DESCRIPTION		ORDERING CODE
V 9553	BFG195	PEL	5322 130 61712
V 9554	BFG195	PEL	5322 130 61712
V 9556	BLU98	PEL	5322 130 61709
V 9557	BLU98	PEL	5322 130 61709
V 9558	BCX54-10	PEL	5322 130 61708
V 9559	BCX54-10	PEL	5322 130 61708

INTERGRATED CICUITS

POSNR	DESCRIPTION		ORDERING CODE
D 0401	SN74LS245N	T.I	5322 209 86225
D 0402	SN74LS245N	T.I	5322 209 86225
D 0403	PC74HCT573P	PEL	5322 209 11488
D 0404	74F32PC	FSC	4822 209 82133
D 0406	PC74HCT138P	PEL	5322 209 11111
D 0407	PC74HCT238P	PEL	5322 209 11482
D 0408	PC74HCT14P	PEL	5322 209 11378
D 0409	PC74HCT574P	PEL	5322 209 11489
D 0411	PC74HCT574P	PEL	5322 209 11489
D 0412	PC74HCT574P	PEL	5322 209 11489
D 0413	PC74HCT574P	PEL	5322 209 11489
D 0414	N7407N	SIG	5322 209 84761
D 0416	N7407N	SIG	5322 209 84761
D 0417	PC74HCT574P	PEL	5322 209 11489
D 0419	PC74HCT541P	PEL	5322 209 11487
D 0421	PC74HCT574P	PEL	5322 209 11489
D 0422	PC74HCT574P	PEL	5322 209 11489
D 0423	CD74HCT4066E	RC	5322 209 71655
D 0424	PC74HCT299P	PEL	5322 209 11486
D 0426	PC74HCT299P	PEL	5322 209 11486
D 0427	PC74HCT574P	PEL	5322 209 11489
D 0428	PC74HCT107P	PEL	5322 209 11108
D 0429	PC74HCT574P	PEL	5322 209 11489
D 0431	PC74HCT574P	PEL	5322 209 11489
D 0432	PC74HCT123P	PEL	5322 209 11379
D 0433	PC74HCT238P	PEL	5322 209 11482
D 0434	PC74HCT541P	PEL	5322 209 11487
D 0436	PC74HCT574P	PEL	5322 209 11489
D 0601	N74LS266N	SIG	5322 209 86163
D 0602	N74LS266N	SIG	5322 209 86163
D 0603	N74LS266N	SIG	5322 209 86163
D 0604	PC74HCT374P	PEL	5322 209 11119
D 0606	PC74HCT374P	PEL	5322 209 11119
D 0607	74F08PC	FSC	5322 209 81574
D 0608	PC74HCT74P	PEL	5322 209 11109
D 0609	PC74HCT74P	PEL	5322 209 11109
D 0611	PC74HCT161P	PEL	5322 209 11476
D 0612	ARRAY OQ 0127		5322 209 80992
D 0614	PC74HCT04P	PEL	4822 209 82341
D 1201	PC74HCT04P	PEL	4822 209 82341
D 1202	PC74HCT11P	PEL	4822 209 11427
D 1203	PC74HCT245P	PEL	5322 209 11117
D 1204	PC74HCT243P	PEL	5322 209 11474
D 1206	PC74HCT243P	PEL	5322 209 11474
D 1207	PC74HCT373P	PEL	5322 209 11118
D 1208	PC74HCT373P	PEL	5322 209 11118
D 1209	74F08PC	FSC	5322 209 81574
D 1211	PC74HCT86P	PEL	5322 209 11473
D 1212	PC74HCT86P	PEL	5322 209 11473
D 1213	PC74HCT86P	PEL	5322 209 11473
D 1214	PC74HCT86P	PEL	5322 209 11473
D 1216	PC74HCT273P	PEL	5322 209 11485
D 1217	PC74HCT273P	PEL	5322 209 11485
D 1218	74F283PC	FSC	5322 209 81588
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D 1221	74F283PC	FSC	5322 209 81588
D 1222	74F283PC	FSC	5322 209 81588
D 1223	74F86PC	FSC	5322 209 81539
D 1224	PC74HCT374P	PEL	5322 209 11119
D 1226	PC74HCT374P	PEL	5322 209 11119
D 1227	74F32PC	FSC	4822 209 82133
D 1228	74F00PC	FSC	5322 209 81534
D 1229	74F32PC	FSC	4822 209 82133
D 1231	74F74PC	FSC	5322 209 81474
D 1232	PC74HCT157P	PEL	5322 209 11263
D 1233	74F175PC	FSC	5322 209 81542
D 1234	74F257APC	FSC	5322 209 71672
D 1236	PC74HCT257P	PEL	5322 209 11114
D 1237	PC74HCT257P	PEL	5322 209 11114
D 1238	PC74HCT257P	PEL	5322 209 11114
D 1239	PC74HCT257P	PEL	5322 209 11114
D 1241	PC74HCT257P	PEL	5322 209 11114
D 1242	PC74HCT299P	PEL	5322 209 11486
D 1243	PC74HCT299P	PEL	5322 209 11486
D 1244	PC74HCT04P	PEL	4822 209 82341
D 1246	PC74HCT04P	PEL	4822 209 82341
D 1247	PC74HCT30P	PEL	5322 209 11492
D 1248	PC74HCT30P	PEL	5322 209 11492
D 1249	RAM 8KX8 35NS		5322 209 61146
D 1251	RAM 8KX8 35NS		5322 209 61146
D 1252	D2147H	INT	5322 209 11495
D 1253	D2147H	INT	5322 209 11495
D 1254	74F139PC	FSC	5322 209 82234
D 1401	PC74HCT138P	PEL	5322 209 11111
D 1402	74F251APC	FSC	5322 209 71656
D 1403	74F251APC	FSC	5322 209 71656
D 1404	PC74HCT11P	PEL	4822 209 11427
D 1406	74F04PC	FSC	5322 209 81577
D 1407	74F08PC	FSC	5322 209 81574
D 1408	SN74LS38N	T.I	5322 209 85605
D 1409	74F257APC	FSC	5322 209 71672
D 1411	74F257APC	FSC	5322 209 71672
D 1412	74F257APC	FSC	5322 209 71672
D 1413	PC74HCT541P	PEL	5322 209 11487
D 1414	PC74HCT541P	PEL	5322 209 11487
D 1416	PC74HCT541P	PEL	5322 209 11487
D 1417	PC74HCT541P	PEL	5322 209 11487
D 1418	74F574PC	FSC	5322 209 72659
D 1419	PC74HCT574P	PEL	5322 209 11489
D 1421	PC74HCT574P	PEL	5322 209 11489
D 1422	PC74HCT173P	PEL	5322 209 11477
D 1423	SN74LS125AN	T.I	5322 209 81569
D 1424	74F74PC	FSC	5322 209 81474
D 1426	MM2016AP-90	TOS	5322 209 71653
D 1427	MM2016AP-90	TOS	5322 209 71653
D 1428	MM2016AP-90	TOS	5322 209 71653
D 1429	MM2016AP-90	TOS	5322 209 71653
D 1431	74F574PC	FSC	5322 209 72659
D 1432	74F574PC	FSC	5322 209 72659
D 1433	74F574PC	FSC	5322 209 72659
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D 1436	74F574PC	FSC	5322 209 72659
D 1437	74F174PC	FSC	5322 209 83326
D 1438	74F174PC	FSC	5322 209 83326
D 1439	74F174PC	FSC	5322 209 83326
D 1441	74F174PC	FSC	5322 209 83326
D 1442	74F174PC	FSC	5322 209 83326
D 1443	PC74HCT174P	PEL	5322 209 11478
D 1444	PC74HCT174P	PEL	5322 209 11478
D 1446	74F283PC	FSC	5322 209 81588
D 1447	74F283PC	FSC	5322 209 81588
D 1448	74F283PC	FSC	5322 209 81588
D 1449	PC74HCT257P	PEL	5322 209 11114
D 1451	PC74HCT257P	PEL	5322 209 11114
D 1452	PC74HCT257P	PEL	5322 209 11114
D 1453	PC74HCT191P	PEL	5322 209 11481
D 1454	PC74HCT191P	PEL	5322 209 11481
D 1456	PC74HCT191P	PEL	5322 209 11481
D 1457	PLS105F-PROG		5322 209 51456
D 1458	74F175PC	FSC	5322 209 81542
D 1459	74F175PC	FSC	5322 209 81542
D 1461	74F32PC	FSC	4822 209 82133
D 1702	74F04PC	FSC	5322 209 81577
D 1703	PC74HCT393P	PEL	4822 209 83045
D 1704	74F74PC	FSC	5322 209 81474
D 1706	PC74HCT390P	PEL	5322 209 11483
D 1707	PC74HCT390P	PEL	5322 209 11483
D 1708	SN74LS148N	T.I	4822 209 80452
D 1709	PC74HCT123P	PEL	5322 209 11379
D 1712	PC74HCT132P	PEL	4822 209 83044
D 1713	PC74HCT175P	PEL	5322 209 11479
D 1714	SN74LS05N	T.I	5322 209 84994
D 1716	PC74HCT03P	PEL	5322 209 11316
D 1717	MC68000RC8	MOT	5322 209 71666
D 1718	SN74LS541N	T.I	5322 209 71671
D 1719	SN74LS541N	T.I	5322 209 71671
D 1721	SN74LS541N	T.I	5322 209 71671
D 1722	SN74LS245N	T.I	5322 209 86225
D 1723	SN74LS245N	T.I	5322 209 86225
D 1729	PC74HCT04P	PEL	4822 209 82341
D 1731	C2606NQD	SIG	5322 209 86197
D 1732	PC74HCT32P	PEL	5322 209 11266
D 1733	PC74HCT00P	PEL	5322 209 11105
D 1734	PC74HCT08P	PEL	5322 209 11265
D 1736	PC74HCT74P	PEL	5322 209 11109
D 1737	PC74HCT10P	PEL	5322 209 11107
D 1738	PC74HCT32P	PEL	5322 209 11266
D 1739	PC74HCT32P	PEL	5322 209 11266
D 1741	PC74HCT139P	PEL	5322 209 11112
D 1742	PC74HCT02P	PEL	5322 209 11106
D 1743	PC74HCT30P	PEL	5322 209 11492
D 1744	PC74HCT138P	PEL	5322 209 11111
D 1746	SN74LS541N	T.I	5322 209 71671
D 1747	SN74LS541N	T.I	5322 209 71671
D 1751	PC74HCT164P	PEL	5322 209 11268
D 1801	P8254	INT	5322 209 82406

POSNR	DESCRIPTION	ORDERING CODE
D 1802	P8254 INT	5322 209 82406
D 1803	PLS105F-PROG	5322 209 51454
D 1804	PLS105F-PROG	5322 209 51455
D 1806	PC74HCT139P PEL	5322 209 11112
D 1807	PC74HCT574P PEL	5322 209 11489
D 1808	74F163APC FSC	5322 209 83343
D 1809	74F08PC FSC	5322 209 81574
D 1811	PC74HCT574P PEL	5322 209 11489
D 1812	PC74HCT04P PEL	4822 209 82341
D 1813	HEF4731VP PEL	5322 209 14859
D 1814	PC74HCT164P PEL	5322 209 11268
D 1816	PC74HCT273P PEL	5322 209 11485
D 1817	PC74HCT151P PEL	5322 209 11442
D 1818	PC74HCT151P PEL	5322 209 11442
D 1819	PC74HCT175P PEL	5322 209 11479
D 1821	PC74HCT74P PEL	5322 209 11109
D 1822	74F541PC FSC	5322 209 72658
D 1823	SN74LS245N T.I	5322 209 86225
D 1824	SN74LS245N T.I	5322 209 86225
D 1826	PC74HCT574P PEL	5322 209 11489
D 1827	PC74HCT574P PEL	5322 209 11489
D 1828	PC74HCT573P PEL	5322 209 11488
D 1829	PC74HCT32P PEL	5322 209 11266
D 1831	PC74HCT32P PEL	5322 209 11266
D 1832	SN74LS38N T.I	5322 209 85605
D 1833	CD74HCT4066E RC	5322 209 71655
D 1834	M62256LP-12 HIT	5322 209 72129
D 1836	M62256LP-12 HIT	5322 209 72129
D 1837	M62256LP-12 HIT	5322 209 72129
D 1838	M62256LP-12 HIT	5322 209 72129
D 1841	PC74HCT14P PEL	5322 209 11378
D 2001	PC74HCT373P PEL	5322 209 11118
D 2002	PC74HCT373P PEL	5322 209 11118
D 2003	SN74LS652N T.I	5322 209 71654
D 2004	SN74LS652N T.I	5322 209 71654
D 2006	PC74HCT245P PEL	5322 209 11117
D 2007	PC74HCT245P PEL	5322 209 11117
D 2008	M6264ALP-12 HIT	5322 209 60192
D 2009	M6264ALP-12 HIT	5322 209 60192
D 2011	M6264ALP-12 HIT	5322 209 60192
D 2012	M6264ALP-12 HIT	5322 209 60192
D 2013	CD74HCT4066E RC	5322 209 71655
D 2014	M6264ALP-12 HIT	5322 209 60192
D 2016	M6264ALP-12 HIT	5322 209 60192
D 2017	PC74HCT74P PEL	5322 209 11109
D 2018	PC74HCT161P PEL	5322 209 11476
D 2019	PC74HCT161P PEL	5322 209 11476
D 2021	PC74HCT161P PEL	5322 209 11476
D 2022	PC74HCT174P PEL	5322 209 11478
D 2023	PC74HCT174P PEL	5322 209 11478
D 2024	PC74HCT85P PEL	5322 209 11484
D 2026	PC74HCT85P PEL	5322 209 11484
D 2027	PC74HCT85P PEL	5322 209 11484
D 2028	PC74HCT374P PEL	5322 209 11119
D 2029	PC74HCT374P PEL	5322 209 11119
D 2031	PC74HCT374P PEL	5322 209 11119
D 2032	PC74HCT374P PEL	5322 209 11119
D 2033	PC74HCT173P PEL	5322 209 11477
D 2034	PC74HCT374P PEL	5322 209 11119
D 2036	PC74HCT374P PEL	5322 209 11119
D 2037	74F257APC FSC	5322 209 71672
D 2038	74F257APC FSC	5322 209 71672
D 2039	74F257APC FSC	5322 209 71672
D 2041	PC74HCT173P PEL	5322 209 11477
D 2101	PC74HCT541P PEL	5322 209 11487
D 2102	PC74HCT541P PEL	5322 209 11487
D 2103	PC74HCT574P PEL	5322 209 11489
D 2104	PC74HCT574P PEL	5322 209 11489
D 2106	PC74HCT574P PEL	5322 209 11489
D 2107	PC74HCT574P PEL	5322 209 11489
D 2108	PC74HCT574P PEL	5322 209 11489
D 2109	74F04PC FSC	5322 209 81577
D 2111	PC74HCT191P PEL	5322 209 11481
D 2112	PC74HCT191P PEL	5322 209 11481
D 2113	PC74HCT191P PEL	5322 209 11481
D 2114	PC74HCT109P PEL	5322 209 11475
D 2116	PC74HCT74P PEL	5322 209 11109
D 2117	PC74HCT02P PEL	5322 209 11106
D 2118	PC74HCT257P PEL	5322 209 11114
D 2119	PC74HCT08P PEL	5322 209 11265
D 2121	PC74HCT244P PEL	5322 209 11116
D 2122	PC74HCT244P PEL	5322 209 11116
D 2123	PC74HCT244P PEL	5322 209 11116
D 2124	PC74HCT244P PEL	5322 209 11116
D 2126	P8254 INT	5322 209 82406
D 2127	PC74HCT123P PEL	5322 209 11379
D 2128	SN74LS38N T.I	5322 209 85605
D 2129	PC74HCT32P PEL	5322 209 11266
D 2131	PC74HCT139P PEL	5322 209 11112
D 2132	PC74HCT138P PEL	5322 209 11111

POSNR	DESCRIPTION	ORDERING CODE
D 2133	PC74HCT107P PEL	5322 209 11108
D 2134	74F163APC FSC	5322 209 83343
D 2136	74F04PC FSC	5322 209 81577
D 2137	PC74HCT32P PEL	5322 209 11266
D 2138	PC74HCT08P PEL	5322 209 11265
D 2139	74F109PC FSC	5322 209 81669
D 2141	74F109PC FSC	5322 209 81669
D 2142	PLS155F-PROG	5322 209 51452
D 2143	PC74HCT00P PEL	5322 209 11105
D 2144	PC74HCT123P PEL	5322 209 11379
D 2146	PC74HCT27P PEL	5322 209 11472
D 2147	74F32PC FSC	4822 209 82133
D 2148	74F74PC FSC	5322 209 81474
D 2149	74F08PC FSC	5322 209 81574
D 2151	PLS100F-PROG	5322 209 51453
D 2152	74F32PC FSC	4822 209 82133
D 2153	74F11PC FSC	5322 209 81536
D 2154	74F00PC FSC	5322 209 81534
D 2156	PC74HCT174P PEL	5322 209 11478
D 2157	PC74HCT27P PEL	5322 209 11472
D 2158	74F32PC FSC	4822 209 82133
D 2301	PLS155F-PROG	5322 209 51449
D 2302	PLS155F-PROG	5322 209 51451
D 2303	PC74HCT244P PEL	5322 209 11116
D 2304	PC74HCT244P PEL	5322 209 11116
D 2306	PC74HCT257P PEL	5322 209 11114
D 2307	PC74HCT257P PEL	5322 209 11114
D 2308	PC74HCT257P PEL	5322 209 11114
D 2309	PC74HCT175P PEL	5322 209 11479
D 2311	PC74HCT257P PEL	5322 209 11114
D 2312	PC74HCT257P PEL	5322 209 11114
D 2313	PC74HCT257P PEL	5322 209 11114
D 2314	PC74HCT574P PEL	5322 209 11489
D 2316	PC74HCT574P PEL	5322 209 11489
D 2317	PC74HCT574P PEL	5322 209 11489
D 2318	PC74HCT574P PEL	5322 209 11489
D 2319	PC74HCT283P PEL	5322 209 11493
D 2321	PC74HCT283P PEL	5322 209 11493
D 2322	PC74HCT283P PEL	5322 209 11493
D 2323	PC74HCT283P PEL	5322 209 11493
D 2324	PC74HCT283P PEL	5322 209 11493
D 2326	PC74HCT283P PEL	5322 209 11493
D 2327	PC74HCT283P PEL	5322 209 11493
D 2328	PC74HCT283P PEL	5322 209 11493
D 2329	PC74HCT174P PEL	5322 209 11478
D 2331	PC74HCT174P PEL	5322 209 11478
D 2332	PC74HCT574P PEL	5322 209 11489
D 2333	N74LS298N SIG	5322 209 85937
D 2334	N74LS298N SIG	5322 209 85937
D 2336	N74LS298N SIG	5322 209 85937
D 2337	PC74HCT00P PEL	5322 209 11105
D 2338	PC74HCT27P PEL	5322 209 11472
D 2339	PC74HCT08P PEL	5322 209 11265
D 2341	C74HCT4053P PEL	4822 209 71584
D 2342	C74HCT4053P PEL	4822 209 71584
D 2343	C74HCT4053P PEL	4822 209 71584
D 2501	HEF4053BP PEL	5322 209 10576
D 2502	PC74HCT390P PEL	5322 209 11483
D 2503	PC74HCT74P PEL	5322 209 11109
D 2504	PC74HCT86P PEL	5322 209 11473
D 4001	HEF40106BP PEL	4822 209 10318
D 4002	HEF40106BP PEL	4822 209 10318
D 4003	HEF4070BP PEL	4822 209 10265
D 4004	HEF4070BP PEL	4822 209 10265
D 4006	HEF4082BP PEL	4822 209 10271
D 4007	HEF4070BP PEL	4822 209 10265
D 4008	HEF40106BP PEL	4822 209 10318
D 4009	PC74HCT374P PEL	5322 209 11119
D 4011	PC74HCT374P PEL	5322 209 11119
D 4012	PC74HCT374P PEL	5322 209 11119
D 4013	PC74HCT138P PEL	5322 209 11111
D 4014	HEF4073BP PEL	4822 209 10266
D 4016	HEF4013BP PEL	4822 209 10248
D 4017	HEF40106BP PEL	4822 209 10318
D 4201	C74HCT4051P PEL	5322 209 71662
D 4202	PC74HCT27P PEL	5322 209 11472
D 4203	SN74LS245N T.I	5322 209 86225
D 4204	PC74HCT138P PEL	5322 209 11111
D 4206	PC74HCT374P PEL	5322 209 11119
D 4207	PC74HCT374P PEL	5322 209 11119
D 5001	HEF4066BP PEL	5322 209 10357
D 5201	ARRAY OQ 0127	5322 209 80992
D 6001	INTERGR.CIRC. OQ0206	5322 209 11606
D 6002	60Z14A020H SPR	5322 209 71673
D 6003	60Z14A020H SPR	5322 209 71673
D 6004	C74HCT4052P PEL	4822 209 71583
D 6006	PC74HCT138P PEL	5322 209 11111
D 6007	PC74HCT00P PEL	5322 209 11105
D 6008	PC74HCT123P PEL	5322 209 11379
D 6009	PC74HCT74P PEL	5322 209 11109
D 6010	PC74HCT10P PEL	5322 209 11107

POSNR	DESCRIPTION		ORDERING CODE
D 6011	PC74HCT14P	PEL	5322 209 11378
D 6012	74F00PC	FSC	5322 209 81534
D 6016	PC74HCT191P	PEL	5322 209 11481
D 6017	PC74HCT191P	PEL	5322 209 11481
D 6018	PC74HCT191P	PEL	5322 209 11481
D 6019	PC74HCT191P	PEL	5322 209 11481
D 6021	PC74HCT20P	PEL	5322 209 11471
D 6022	74F191PC	FSC	5322 209 81676
D 6026	PC74HCT191P	PEL	5322 209 11481
D 6027	PC74HCT191P	PEL	5322 209 11481
D 6028	PC74HCT191P	PEL	5322 209 11481
D 6029	PC74HCT191P	PEL	5322 209 11481
D 6031	PC74HCT574P	PEL	5322 209 11489
D 6032	PC74HCT574P	PEL	5322 209 11489
D 6033	PC74HCT574P	PEL	5322 209 11489
D 6034	PC74HCT574P	PEL	5322 209 11489
D 6036	PC74HCT574P	PEL	5322 209 11489
D 6037	PC74HCT574P	PEL	5322 209 11489
D 6401	100124FC	FSC	5322 209 71667
D 6402	100102FC	FSC	5322 209 85518
D 6403	100102FC	FSC	5322 209 85518
D 6404	100131FC	FSC	5322 209 82939
D 6406	100131FC	FSC	5322 209 82939
D 6407	100131FC	FSC	5322 209 82939
D 6408	100131FC	FSC	5322 209 82939
D 6409	100102FC	FSC	5322 209 85518
D 6801	HEF4052BT	PEL	5322 209 11102
D 6901	HEF4052BP	PEL	4822 209 10263
D 7003	PC74HCT123P	PEL	5322 209 11379
D 7004	PC74HCT74P	PEL	5322 209 11109
D 7351	100114FC	FSC	5322 209 73375
D 7352	100107FC	FSC	5322 209 61143
D 7852	PC74HCT02P	PEL	5322 209 11106
D 7853	PC74HCT04P	PEL	4822 209 82341
D 7854	PC74HCT157P	PEL	5322 209 11263
D 8001	P2CCD OM3021		5322 209 61141
D 8201	P2CCD OM3021		5322 209 61141
D 8301	74F574PC	FSC	5322 209 72659
D 8302	74F112PC	FSC	5322 209 70101
D 8303	PAL20R8ACJS-PROG		5322 209 51457
D 8304	74F163APC	FSC	5322 209 83343
D 8306	PAL16R8ACN-PROG		5322 209 51458
D 8308	74F08PC	FSC	5322 209 81574
D 8309	74F257APC	FSC	5322 209 71672
D 8311	74F163APC	FSC	5322 209 83343
D 8321	C74HCT4066T	PEL	5322 209 61129
D 8331	C74HCT4052T	PEL	5322 209 61132
D 8351	C74HCT4066T	PEL	5322 209 61129
D 8361	C74HCT4066T	PEL	5322 209 61129
D 8371	C74HCT4052T	PEL	5322 209 61132
D 8401	C74HCT4066T	PEL	5322 209 61129
D 8501	C74HCT4051T	PEL	5322 209 61131
N 0401	ARRAY OQ-0145		5322 209 81324
N 0402	AD7541AJN	AND	5322 209 11277
N 0403	AD7574JN	AND	5322 209 82102
N 0404	TDA1540P	PEL	4822 209 81453
N 0406	TDA1540P	PEL	4822 209 81453
N 0407	TDA1540P	PEL	4822 209 81453
N 0408	TDA1540P	PEL	4822 209 81453
N 0409	OP-77GP	PMI	5322 130 60937
N 0411	OP-77GP	PMI	5322 130 60937
N 0412	LF398N	N.S	5322 209 83291
N 0413	LF398N	N.S	5322 209 83291
N 0414	LF398N	N.S	5322 209 83291
N 0416	LF398N	N.S	5322 209 83291
N 0417	OP-77GP	PMI	5322 130 60937
N 0418	OP-77GP	PMI	5322 130 60937
N 0419	OP-77GP	PMI	5322 130 60937
N 0421	OP-77GP	PMI	5322 130 60937
N 0422	OP-77GP	PMI	5322 130 60937
N 0423	OP-77GP	PMI	5322 130 60937
N 0424	OP-77GP	PMI	5322 130 60937
N 0426	OP-77GP	PMI	5322 130 60937
N 0601	CA3086	RCA	5322 209 11225
N 0602	LM79L15ACZ	N.S	5322 209 82751
N 0603	LM78L15ACZ	N.S	4822 209 80889
N 0604	LM78L15ACZ	N.S	4822 209 80889
N 0606	ADC806BM	BBR	5322 209 61147
N 0607	LM317LZ	MOT	5322 209 82943
N 0609	LM337LZ	NSC	5322 209 83228
N 1711	LM311N	NSC	5322 209 85503
N 2301	DAC10FX	PMI	5322 209 71665
N 2302	DAC-08EP	PMI	5322 209 11253
N 2303	DAC10FX	PMI	5322 209 71665
N 2304	LM358N	NSC	4822 209 70672
N 2306	LM79L15ACZ	N.S	5322 209 82751
N 2307	LM79L05ACZ	NSC	5322 209 86434
N 2503	LM358N	NSC	4822 209 70672
N 2506	TL082CP	T.I	5322 209 86064

POSNR	DESCRIPTION		ORDERING CODE
N 2507	LF398N	N.S	5322 209 83291
N 2508	LF398N	N.S	5322 209 83291
N 4401	LM358N	NSC	4822 209 70672
N 4601	LM324N	NSC	4822 209 80587
N 4602	LM339AN	NSC	5322 209 60188
N 4701	OP-77GP	PMI	5322 130 60937
N 4702	LM324N	NSC	4822 209 80587
N 4801	OP-77GP	PMI	5322 130 60937
N 5001	NE5532P	T.I	5322 209 83339
N 5002	NE5532P	T.I	5322 209 83339
N 5101	NE5532P	T.I	5322 209 83339
N 5201	CA3086	RCA	5322 209 11225
N 6001	LM337T	N.S	5322 209 81236
N 6803	LM358D	MOT	5322 209 82941
N 6901	OP-77GP	PMI	5322 130 60937
N 6903	ULN2003AN	T.I	5322 209 86299
N 7001	LM324N	NSC	4822 209 80587
N 7002	LM324N	NSC	4822 209 80587
N 7003	LM324N	NSC	4822 209 80587
N 7006	LM337T	N.S	5322 209 81236
N 7007	LM317LZ	MOT	5322 209 82943
N 7008	LM337LZ	NSC	5322 209 83228
N 7461	OP-77GP	PMI	5322 130 60937
N 7462	OP-77GP	PMI	5322 130 60937
N 7503	CA3086	RCA	5322 209 11225
N 7703	CA3086	RCA	5322 209 11225
N 7851	LM337LZ	NSC	5322 209 83228
N 7852	LM317T	N.S	4822 209 80591
N 7853	LM317T	N.S	4822 209 80591
N 7854	LM337LZ	NSC	5322 209 83228
N 8201	LM741CM	NSC	5322 209 61136
N 8202	M285BXZ-1.2	NSC	5322 209 73655
N 8311	HA3-2525-5	HAR	5322 209 71661
N 8331	HA3-2525-5	HAR	5322 209 71661
N 8351	HA3-2525-5	HAR	5322 209 71661
N 8371	HA3-2525-5	HAR	5322 209 71661
N 8401	HA3-2525-5	HAR	5322 209 71661
N 8411	HA3-2525-5	HAR	5322 209 71661
N 8501	NE521N	SIG	5322 209 14441
N 8502	LF356N	NSC	5322 209 86451
N 8503	ADC80MAH-12	BBR	5322 209 61134
N 8504	UA714TC	FSC	5322 209 70275
N 8506	LM358N	NSC	4822 209 70672
N 8507	OP-77GP	PMI	5322 130 60937
N 8508	OP-77GP	PMI	5322 130 60937
N 8509	LM337T	N.S	5322 209 81236
N 8511	TDA1540P	PEL	4822 209 81453
N 8512	OP-77GP	PMI	5322 130 60937
N 8513	OP-77GP	PMI	5322 130 60937
N 8701	LM741CM	NSC	5322 209 61136
N 9251	LM358D	MOT	5322 209 82941
N 9252	LM337LZ	NSC	5322 209 83228
N 9301	LM358D	MOT	5322 209 82941
N 9302	LM337LZ	NSC	5322 209 83228
N 9352	LM337LZ	NSC	5322 209 83228
N 9451	LM358D	MOT	5322 209 82941
N 9452	LM337LZ	NSC	5322 209 83228
N 9501	LM358D	MOT	5322 209 82941
N 9502	LM337LZ	NSC	5322 209 83228
N 9552	LM337LZ	NSC	5322 209 83228
N 9601	M285BXZ-1.2	NSC	5322 209 73655
N 9602	M285BXZ-1.2	NSC	5322 209 73655

CONNECTORS

POSNR	DESCRIPTION	ORDERING CODE
X 0101	10-P DBL RT.ANG	5322 265 51188
X 0103	4-P SNG RT.ANG	5322 265 30533
X 0104	5-P SNG RT.ANG	5322 265 30529
X 0106	10-P DBL RT.ANG	5322 265 51188
X 0501	64-P RGHT ANGL	5322 265 61124
X 0502	64-P SKT 2.54	5322 267 70233
X 0503	64-P SKT 2.54	5322 267 70233
X 0504	96-P BUS A-B-C	5322 267 70234
X 0506	96-P BUS A-B-C	5322 267 70234
X 0507	96-P BUS A-B-C	5322 267 70234
X 0508	96-P BUS A-B-C	5322 267 70234
X 0509	96-P BUS A-B-C	5322 267 70234
X 0511	64-P SKT 2.54	5322 267 70233
X 0512	96-P BUS A-B-C	5322 267 70234
X 0513	96-P BUS A-B-C	5322 267 70234
X 0514	64-P SKT 2.54	5322 267 70233
X 0516	96-P BUS A-B-C	5322 267 70234
X 0517	64-P SKT 2.54	5322 267 70233
X 0518	96-P BUS A-B-C	5322 267 70234
X 0519	64-P SKT 2.54	5322 267 70233

POSNR	DESCRIPTION	ORDERING CODE
X 0521	96-P BUS A-B-C	5322 267 70234
X 0522	64-P SKT 2.54	5322 267 70233
X 0523	96-P BUS A-B-C	5322 267 70234
X 0524	64-P SKT 2.54	5322 267 70233
X 0526	P RECHT QF50	5322 265 51185
X 0527	P RECHT QF50	5322 265 51185
X 0528	4-P SNG STRGHT	5322 265 30534
X 0606	2-P	5322 263 60062
X 0607	64-P PIN 2.54MM	5322 265 61146
X 0609	3-P SNG 2.54	5322 265 30392
X 0609	2-P	5322 263 60062
X 1201	64-P PIN 2.54MM	5322 265 61146
X 1202	64-P PIN 2.54MM	5322 265 61146
X 1401	96-P PIN 2.54	5322 265 61147
X 1402	64-P PIN 2.54MM	5322 265 61146
X 1501	10-P DBL STRGHT	5322 265 40485
X 1502	4-P SNG STRGHT	5322 265 30474
X 1503	3-P SNG RT.ANG	5322 265 30433
X 1701	96-P PIN 2.54	5322 265 61147
X 1702	10-P DBL RT.ANG	5322 265 51188
X 1703	3-P SNG 2.54	5322 265 30392
X 1703	2-P	5322 263 60062
X 1704	3-P SNG 2.54	5322 265 30392
X 1704	2-P	5322 263 60062
X 1706	3-P SNG 2.54	5322 265 30392
X 1706	2-P	5322 263 60062
X 1707	3-P SNG 2.54	5322 265 30392
X 1707	2-P	5322 263 60062
X 1716	2-P SNG 2.54	5322 265 20266
X 1716	2-P	5322 263 60062
X 1801	96-P PIN 2.54	5322 265 61147
X 1802	64-P PIN 2.54MM	5322 265 61146
X 2001	96-P PIN 2.54	5322 265 61147
X 2002	96-P PIN 2.54	5322 265 61147
X 2101	96-P PIN 2.54	5322 265 61147
X 2102	96-P PIN 2.54	5322 265 61147
X 2301	64-P PIN 2.54MM	5322 265 61146
X 2302	64-P PIN 2.54MM	5322 265 61146
X 2501	64-P PIN 2.54MM	5322 265 61146
X 2501	64-P PEN 2.54	5322 265 61025
X 2502	64-P RGHT ANGL	5322 265 61124
X 2513	10-P DBL RGHT	5322 265 40646
X 2514	5-P DBL RGHT	5322 265 30535
X 2516	10-P DBL RGHT	5322 265 40646
X 2601	26-P DBL RGHT	5322 265 51189
X 2602	34-P DBL RGHT	5322 265 61122
X 3001	3-P SNG RT.ANG	5322 265 30433
X 3002	4-P SNG RT.ANG	5322 265 30533
X 3003	10-P DBL RT.ANG	5322 265 51188
X 3004	16-P DBL RT.ANG	5322 265 61119
X 3051	16-P DBL STRGHT	5322 265 61117
X 3304	3-P SNG RT.ANG	5322 265 30433
X 4001	20-P DBL RT.ANG	5322 265 61121
X 4002	20-P DBL STRGHT	5322 265 51129
X 4201	20-P DBL STRGHT	5322 265 51129
X 4202	16-P DBL RT.ANG	5322 265 61119
X 4401	5-P SNG STRGHT	5322 265 30436
X 4402	3-P SNG STRGHT	5322 265 30434
X 4403	50-P DBL STRGHT	5322 265 61123
X 4404	4-P SNG STRGHT	5322 265 30534
X 4406	20-P DBL STRGHT	5322 265 51129
X 4601	3-P SNG STRGHT	5322 265 30434
X 4602	3-P SNG STRGHT	5322 265 30434
X 4603	3-P SNG STRGHT	5322 265 30434
X 4604	64-P BUS 2.54	5322 267 74092
X 4606	50-P DBL STRGHT	5322 265 61123
X 4703	9P DBL SQ 2.54	5322 265 40645
X 5206	34-P DBL STRGHT	5322 265 61069
X 6802	7P DBL SQ 2.54	5322 265 40601
X 6903	9P DBL SQ 2.54	5322 265 40645
X 7014	26-P DBL STRGHT	5322 265 61071
X 7451	7P DBL ST10.2MM	5322 267 50727
X 7452	14-P DBL STRGHT	5322 265 51187
X 7453	9P DBL ST10.2MM	5322 267 50728
X 7454	7P DBL ST10.2MM	5322 267 50727
X 7456	9P DBL ST10.2MM	5322 267 50728
X 7457	7P DBL ST10.2MM	5322 267 50727
X 7461	7-P DBL 2.54	5322 265 40559
X 7462	7P DBL SQ 2.54	5322 265 40601
X 8507	20-P DBL STRGHT	5322 265 51129

MISCELLANEOUS

POSNR	DESCRIPTION		ORDERING CODE
G 1701	LOCO-16M	PEL	5322 216 61456
H 4001	BPW22A-I	PEL	4822 130 41541
H 4002	CQY58A	PEL	5322 130 31643
H 4003	CQY58A	PEL	5322 130 31643
H 4004	BPW22A-I	PEL	4822 130 41541
H 4006	BPW22A-I	PEL	4822 130 41541
H 4007	CQY58A	PEL	5322 130 31643
H 4008	CQY58A	PEL	5322 130 31643
H 4009	BPW22A-I	PEL	4822 130 41541
H 4011	BPW22A-I	PEL	4822 130 41541
H 4012	CQY58A	PEL	5322 130 31643
H 4013	CQY58A	PEL	5322 130 31643
H 4014	BPW22A-I	PEL	4822 130 41541
H 4016	BPW22A-I	PEL	4822 130 41541
H 4017	CQY58A	PEL	5322 130 31643
H 4018	CQY58A	PEL	5322 130 31643
H 4019	BPW22A-I	PEL	4822 130 41541
H 4021	BPW22A-I	PEL	4822 130 41541
H 4022	CQY58A	PEL	5322 130 31643
H 4023	CQY58A	PEL	5322 130 31643
H 4024	BPW22A-I	PEL	4822 130 41541
H 4026	BPW22A-I	PEL	4822 130 41541
H 4027	CQY58A	PEL	5322 130 31643
H 4028	CQY58A	PEL	5322 130 31643
H 4029	BPW22A-I	PEL	4822 130 41541
H 4031	BPW22A-I	PEL	4822 130 41541
H 4032	CQY58A	PEL	5322 130 31643
H 4033	CQY58A	PEL	5322 130 31643
H 4034	BPW22A-I	PEL	4822 130 41541
H 4036	BPW22A-I	PEL	4822 130 41541
H 4037	CQY58A	PEL	5322 130 31643
H 4038	CQY58A	PEL	5322 130 31643
H 4039	BPW22A-I	PEL	4822 130 41541
H 4041	BPW22A-I	PEL	4822 130 41541
H 4042	CQY58A	PEL	5322 130 31643
H 4043	CQY58A	PEL	5322 130 31643
H 4044	BPW22A-I	PEL	4822 130 41541
H 4046	BPW22A-I	PEL	4822 130 41541
H 4047	CQY58A	PEL	5322 130 31643
H 4048	CQY58A	PEL	5322 130 31643
H 4049	BPW22A-I	PEL	4822 130 41541
H 4051	BPW22A-I	PEL	4822 130 41541
H 4052	CQY58A	PEL	5322 130 31643
H 4053	CQY58A	PEL	5322 130 31643
H 4054	BPW22A-I	PEL	4822 130 41541
H 4201	TLHR4613	AEG	5322 130 81522
H 4202	TLHR4613	AEG	5322 130 81522
H 4203	TLHR4613	AEG	5322 130 81522
H 4204	TLHR4613	AEG	5322 130 81522
H 4206	TLHR4613	AEG	5322 130 81522
H 4207	TLHR4613	AEG	5322 130 81522
H 4208	TLHR4613	AEG	5322 130 81522
H 4401	CNX38U	PEL	5322 130 90679
K 6902	RI-23SI		5322 280 20398
K 6903	RI-23SI		5322 280 20398
K 6904	RI-23SI		5322 280 20398
K 6906	RI-23SI		5322 280 20398
S 0001	AAR 70060-007		5322 276 12411
S 0002	2-P MET LED		5322 276 11459
S 0003	2-P MET LED		5322 276 11459
S 0004			5322 276 14338
S 0005			5322 276 14338
S 0006			5322 276 14338
S 0007			5322 276 14338
S 0008			5322 276 14338
S 0009			5322 276 14338
S 0010			5322 276 14338
S 0011			5322 276 14338
S 4216			5322 276 14338
S 4217			5322 276 14338
S 4218			5322 276 14338
S 4219			5322 276 14338
S 4221			5322 276 14338
S 4222			5322 276 14338
S 4223			5322 276 14338
S 4224			5322 276 14338
S 4226			5322 276 14338
S 4227			5322 276 14338
S 4228			5322 276 14338
S 4229			5322 276 14338
S 4231	2-P MET LED		5322 276 11459
S 4232			5322 276 11856
S 4233	2-P MET LED		5322 276 11459
S 4234	2-P MET LED		5322 276 11459
S 4236			5322 276 11856
S 4237	2-P MET LED		5322 276 11459
S 4238	BR		5322 277 10878
S 4239	BR		5322 277 10878
S 4241	BR		5322 277 10878
U 6802	LM339D	SIG	5322 209 70684

CONTENTS

16.0 Accessory information..... 16-1
16.1 Accessories supplied with the instrument..... 16-1
16.1.1 Passive probe with automatic range indication..... 16-1
16.1.2 Blue contrast filter..... 16-1
16.1.2 Front cover..... 16-1
16.2 Optional accessories..... 16-2
16.2.1 IEEE-488/RS232-C bus interface PM8956A 16-2

16.0 ACCESSORY INFORMATION

16.1 ACCESSORIES SUPPLIED WITH THE INSTRUMENT

16.1.1 Passive probe with automatic range indication

For operating or service information refer to the separate booklet, supplied with the probes.

16.1.2 Blue contrast filter

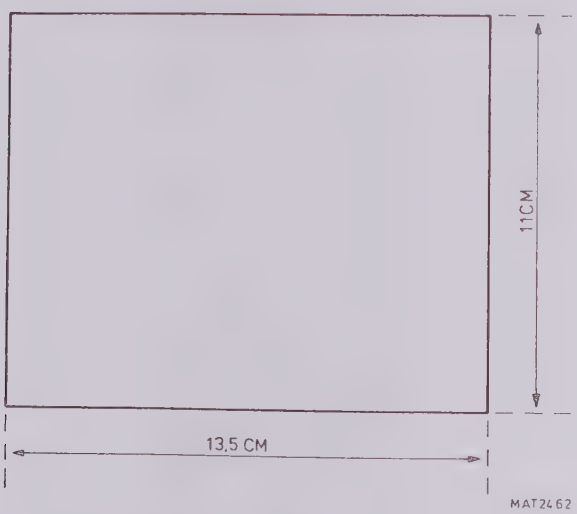


Figure 16.1 Blue contrast filter. (Factory installed !)

16.1.3 Front cover

Figure 16.2 Oscilloscope with front cover.

16.2 OPTIONAL ACCESSORIES

16.2.1 IEEE-488/RS232-C bus interface PM8956A

The interface is a general-purpose bus interface designed according to the IEEE-488/RS232-C standard. This option can be either retrofitted or factory installed. It enables the oscilloscope to be used in a measuring system together with other IEEE-488/RS232-C bus compatible instruments.

For more detailed installation, operating or service information concerning this facility, refer to the separate manual:

IEEE-488/RS232-C BUS INTERFACE PM8956A

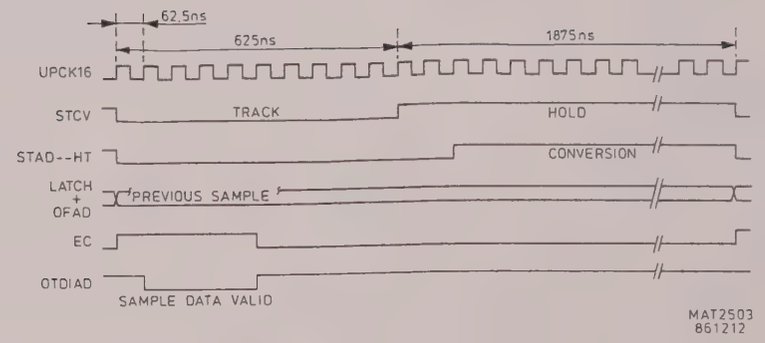


Figure 8.11.1 Timing diagram of the ADC and T&H unit.

NOTE: The STCV signal is derived from the CKCDOC-1 signal on unit A33. The CKCDOC-1 signal is derived from UPCK16 on unit A5. So there is a determined time relationship between the STCV signal and the other control signals on this unit.

8.11.3 Signal name list

UNIT A11

Signal name	Description	Signal source	Signal destination(s)
ADOTØØ...ADOT11	ADC out ØØ...11	A11	A11
ADOT11-1...11-3	ADC out 11-1...11-3	A11	A11
EC	End of conversion	A11	A12-A8
EN250MLT	Enable 250MHz oscillator	A25	-
OFAD	Overflow ADC	A11	A12-A9
OTDIAD	Output disable ADC	A8	-
SADBØØ...11	Sample data bus ØØ...11	A11	A12-A9
STAD--HT	Start ADC	A11	A11
STAD--LT	Start ADC	A11	A11
STCV	Start conversion	A33	-
THINAN	Track & Hold in analogue	A33	-
THOTAN	Track & Hold out analogue	A11	A11
UPCK16	Microprocessor clock 16 MHz	A6	-

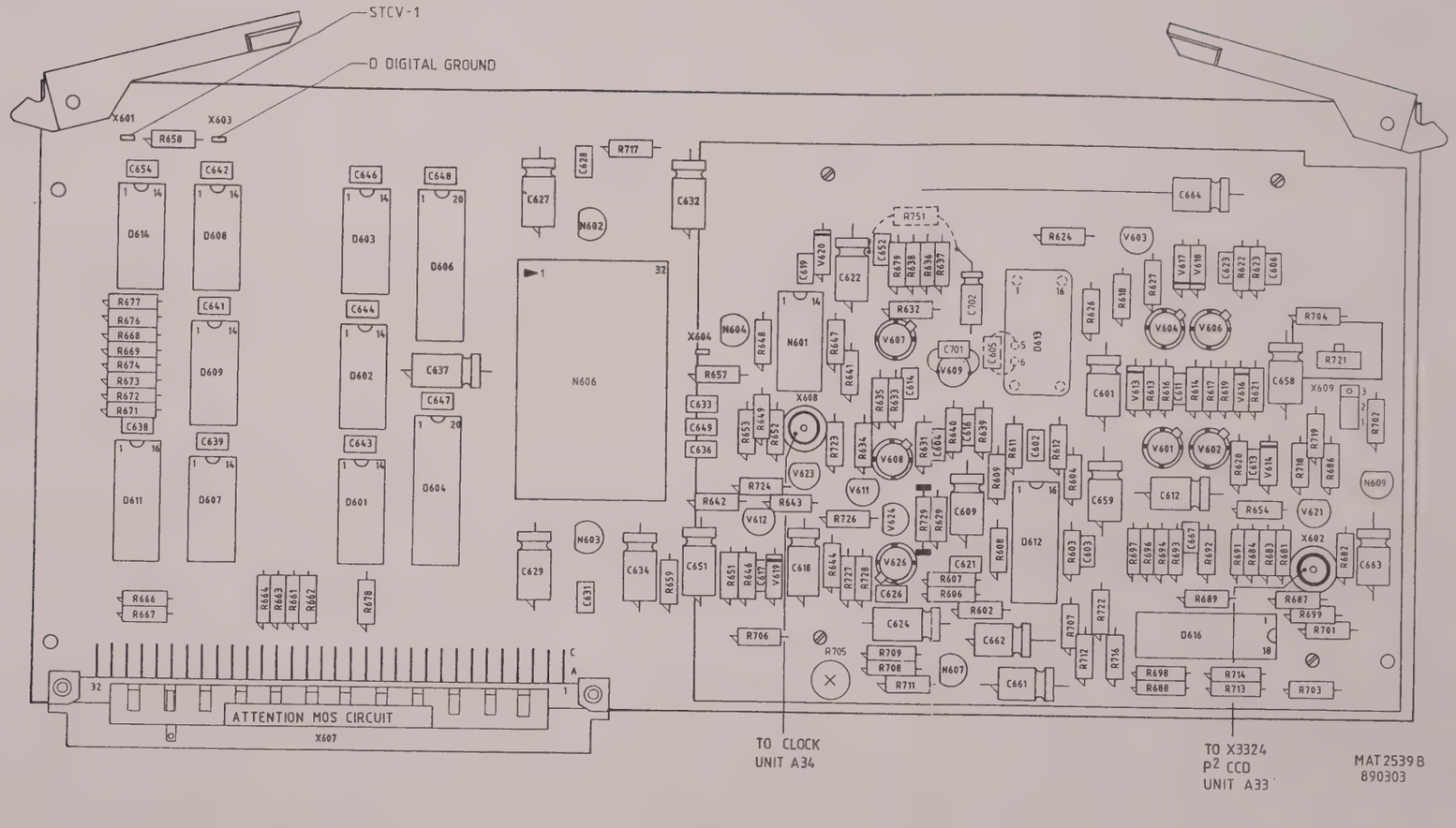


Figure 8.11.2 Unit A11 - ADC + T&H UNIT - p.c.b. lay-out.

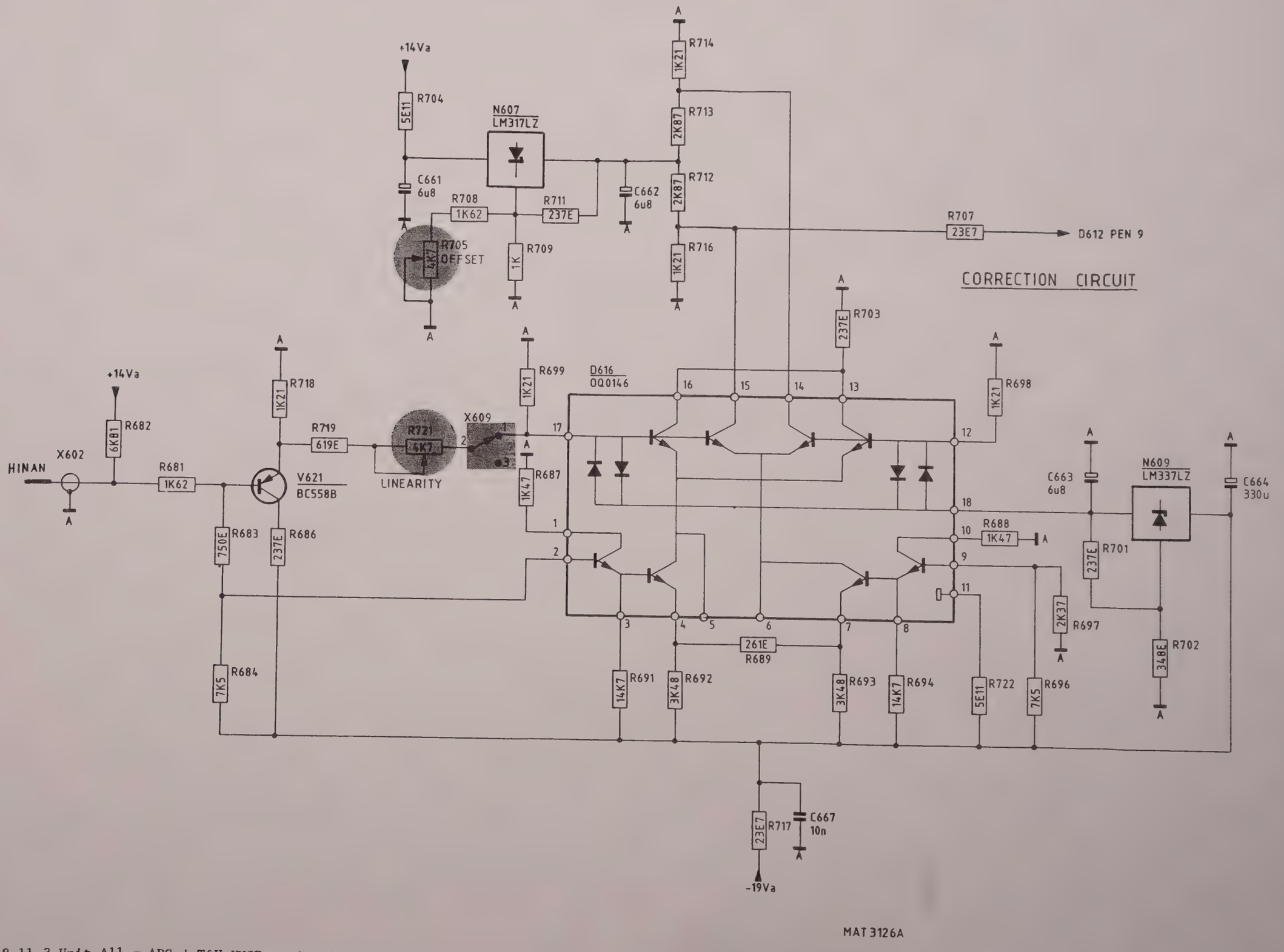


Figure 8.11.3 Unit A11 - ADC + T&H UNIT - circuit diagram.

TRACK & HOLD

ADC

OVERFLOW DETECTION

SAMPLE DATA LATCH

CODE CONVERT

ADC-LOGIC

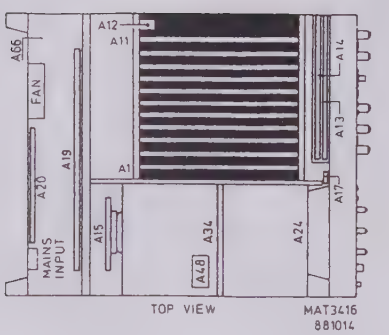
REF NR	TYPE	VCC +5Da	⊥ 0	-7Va
D601, D602, D603	74LS266	14	7	
D604, D606	74HCT374	20	10	
D607	74F08	14	7	
D608, D609	74HCT74	14	7	
D611	74HCT161	16	8	
D612	OQ 8127			5
D614	74HCT04	14	7	
N601	CA3086			12,13,14

D613 BOTTOM VIEW

MAT 25988

Figure 8.11.4 Unit A11 - ADC + T&H UNIT - circuit diagram.

UNIT A12 - MOTHERBOARD



CONTENTS

8.12.1 General information..... 8.12-1
8.12.2 Detailed information..... 8.12-1
8.12.3 Primary bus (CCU-bus)..... 8.12-2
8.12.4 Description of the primary bus signals..... 8.12-3
8.12.5 Secundary bus..... 8.12-4
8.12.6 Additional motherboard connections..... 8.12-14

8.12.1 General information

The function of the motherboard unit is to interconnect the various plug-in units with each other as well as with the rest of the system.

8.12.2 Detailed information

No active components are mounted on this board.

Each plug-in unit is provided with one or two (three row) 96-pole EURO-connectors. One connector is used for the primary or CCU (Central Control Unit) - bus. The other connector is used for the so-called secundary - bus.

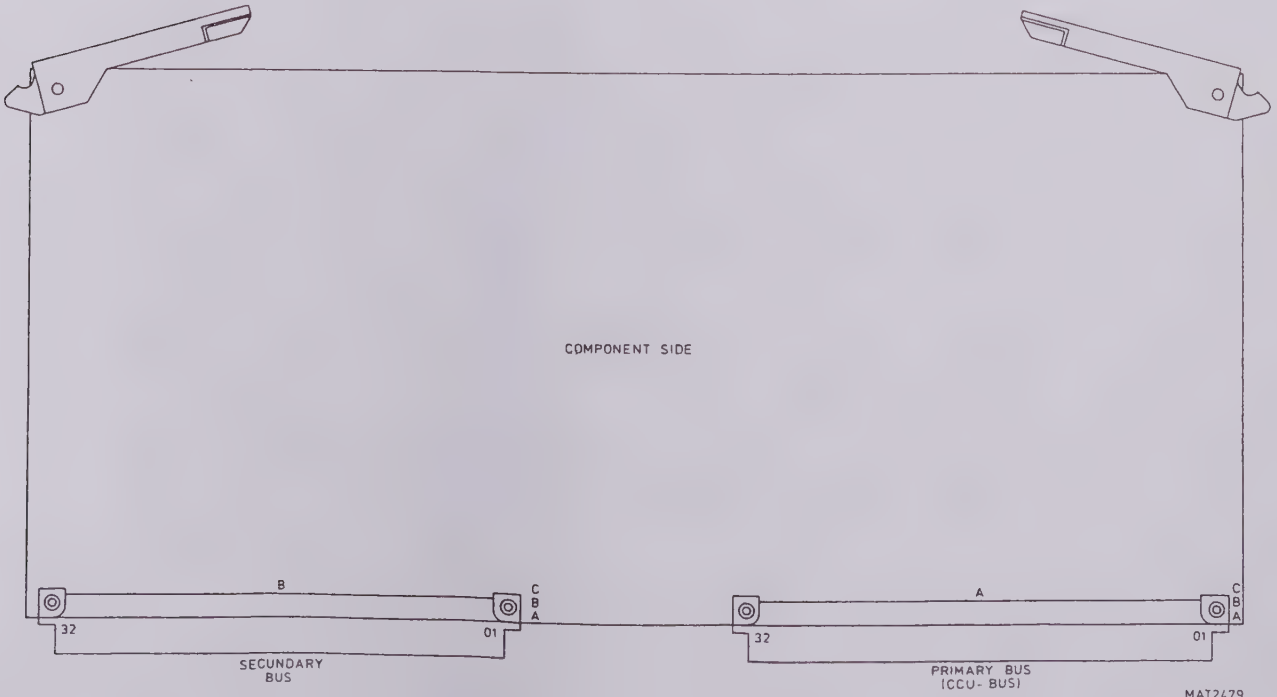


Figure 8.12.1 EURO-connectors.

8.12.3 Primary bus (CCU-bus)

This is a description of the pin lay out for the connectors of the CCU-bus on the motherboard.

```
MOTHERBOARD A12 -----> UNIT
X504 ----------------> A2  - X2301
X507 ----------------> A3  - X2101
X509 ----------------> A4  - X2002
X512 ----------------> A5  - X1801
X513 ----------------> A6  - X1701
X516 ----------------> A7  - X....
X518 ----------------> A8  - X1401
X521 ----------------> A9  - X1201
X523 ----------------> A10- X....
```

ROW A			ROW B			ROW C	
1	+5 D		1	+5 D		1	+5 D	
2	UPCKØ8		2	D		2	UPCK16	
3	D		3	D		3	D	
4	-		4	MYSLØ1LT	* R506/2	4	-	
5	MYSLDWLT		5	MYSLØ2LT	* R506/3	5	-	
6	VBB		6	MYSLØ3LT	* R506/4	6	-	
7	BAVO		7	MYSLØ4LT	* R506/5	7	UPRSOTLT	
8	ABØ1	* R502/2	8	ABØ8	* R506/6	8	DATRAKLT	
9	ABØ2	* R502/3	9	ABØ9	* R506/7	9	DALOSBLT	* R508/2
10	ABØ3	* R502/4	10	AB1Ø	* R506/8	10	DBØØ	* R508/3
11	ABØ4	* R502/5	11	AB11	* R506/9	11	DBØ1	* R508/4
12	ABØ5	* R503/2	12	AB12	* R502/6	12	DBØ2	* R508/5
13	ABØ6	* R503/4	13	AB13	* R503/3	13	DBØ3	* R508/6
14	ABØ7	* R502/7	14	AB14	* R502/8	14	DBØ4	* R508/7
15	IOSLØ3LT	* R503/5	15	AB15	* R502/9	15	DBØ5	* R508/8
16	IOSLØ4LT	* R501/2	16	AB16	* R503/9	16	DBØ6	* R508/9
17	IOSLØ5LT	* R501/4	17	AB17	* R501/3	17	DBØ7	* R503/6
18	IOSLØ6LT	* R504/3	18	AB18	* R504/2	18	DBØ8	* R503/7
19	IOSLØ7LT	* R504/4	19	AB19	* R501/5	19	DBØ9	* R503/8
20	IOSLØ8LT	* R504/6	20	AB2Ø	* R504/5	20	DB1Ø	* R507/2
21	IOSLØ9LT	* R501/6	21	AB21	* R504/7	21	DB11	* R507/3
22	IOSL1ØLT	* R501/7	22	-	* R504/8	22	DB12	* R507/4
23	ILØ1--LT		23	-		23	DB13	* R507/5
24	ILØ2--LT		24	-		24	DB14	* R507/6
25	ILØ3--LT		25	-		25	DB15	* R507/7
26	ILØ4--LT		26	-	* R504/9	26	DAHISBLT	* R507/8
27	ILØ5--LT		27	-	* R501/8	27	UPRD--LT	* R507/9
28	ILØ6--LT		28	WD----LT		28	UPWR--LT	* R501/9
29	ILØ7--LT		29	-		29	Z-MO--XT	
30	A		30	A		30	A	
31	-7 V		31	-7 V		31	-7 V	
32	+7 V		32	+7 V		32	+7 V	

* TERMINATED WITH R.../PINNUMBER

8.12.4 Description of the CCU-bus signals

a1, b1 and c1	: 5 V digital
a3, b2, b3 and c3	: Ground of the digital 5 V
a30, b30 and c30	: Analog earth
a31, b31 and c31	: Analog -7 V
a32, b32 and c32	: Analog 7 V
a2	: 8MHz processor clock
a5	: Memory select down. This line indicates that the chip select of the RAM´s must be disabled on battery back up.
a6	: Voltage for the battery back up RAM´s
a7	: Battery voltage
a8 ... a14	: Lowest 7 address lines
a15 ... a22	: I/O select lines for the selection of the input/output ports
a23 ... a29	: Interrupt level lines. The sequence is as follows: ILØ1--LT --> 40 ms interrupt ILØ2--LT --> DPU interrupt ILØ3--LT --> rotary interrupt ILØ4--LT --> option interrupt ILØ5--LT --> display interrupt ILØ6--LT --> delta-t interrupt ILØ7--LT --> power down interrupt (increasing priority)
b4	: Memory select for the microprocessor RAM
b5	: Memory select for the display memory
b6	: Memory select for the DPU programm memory
b7	: Memory select for the options
b8 ... b21	: Address lines 8 ... 21
b22	: Not used
b23	: Not used
b24	: Not used
b26	: Not used
b27	: Not used
b28	: Watch dog trigger line. Masters can trigger the watchdog via this line.
c2	: 16 MHz clock from the microprocessor unit.
c7	: Microprocessor reset output.
c8	: Data transfer acknowledge. This is an open collector line on which units, which are addressed via MYSLØ1 ... MYSLØ4, can indicate that the data on the data bus is accepted or stable.
C9	: Data lower strobe. With this line active, the lowest 8 data bus lines can be used for read or write actions.
c10 ... c25	: Databus
c27	: Data higher strobe. With this line active, the highest 8 data bus lines can be used for read or write actions.
c28	: Microprocessor read.
c29	: Microprocessor write.
c30	: Z modulation frequency of 200 kHz.

8.12.5 Secundary bus

MOTHERBOARD A12 ---> UNIT A1
X502 ----------> X2501

ROW A		ROW B	ROW C	
1	-	1	1	Z-MO--XT
2	-	2	2	ANCPY-HT
3	-	3	3	ANEPY-HT
4	-	4	4	DPTR--HT
5	-	5	5	DIOS--HT
6	+5D	6	6	Z-BL--HT
7	-	7	7	A
8	-7V	8	8	VREPX2
9	-	9	9	VREPX1
10	+7V	10	10	A
11	A	11	11	X2IN
12	100V	12	12	X1IN
13	A	13	13	A
14	40V	14	14	Y2IN
15	A	15	15	Y1IN
16	+19V	16	16	A
17	A	17	17	-
18	-19V	18	18	-
19	A	19	19	-
20	+14V	20	20	-
21	A	21	21	-
22	-14V	22	22	-
23	-	23	23	-
24	-	24	24	-
25	-	25	25	A
26	-	26	26	A
27	-	27	27	-
28	-	28	28	-
29	-	29	29	SAPL
30	-	30	30	PLZEOT
31	-	31	31	PFPY
32	-	32	32	PU----LT

MOTHERBOARD A12 ---> UNIT A2
X503 ----------> X2302

ROW A		ROW B	ROW C	
1	LEDA--HT	1	1	LEDA--LT
2	WRHOPOLT	2	2	VEDBØ9
3	WRVEPOLT	3	3	VEDBIØ
4	-	4	4	VEDB11
5	DPTR--HT	5	5	VEDB12
6	DIOS--HT	6	6	EPY-ØØ
7	ENTRHOLT	7	7	EPY-Ø1
8	EPX-ØØ	8	8	IVDCDB
9	EPX-Ø1	9	9	ENTXLNLT
10	DCDBØ2	10	10	EPDBØØ
11	DCDBØØ	11	11	EPDBØ1
12	DCDBØ5	12	12	EPDBØ2
13	DCDBØ4	13	13	EPDBØ3
14	DCDBØ3	14	14	EPDBØ4
15	DCDBØ7	15	15	EPDBØ5
16	DCDBØ1	16	16	EPDBØ6
17	DCDBØ8	17	17	EPDBØ7
18	EP12--LT	18	18	EPDBØ8
19	EPH014	19	19	EPDBØ9
20	VREPX2	20	20	EPDBIØ
21	VREPX1	21	21	EPDB11
22	EPX-Ø2	22	22	CKEPVE
23	-	23	23	DCDBØ9
24	Z-OTØ3	24	24	DPRJ
25	DCDBØ6	25	25	-
26	X2IN	26	26	WRHOVRLT
27	X1IN	27	27	DJAC--HT
28	Y2IN	28	28	DPRJDW
29	Y1IN	29	29	SM----LT
30	-7 V	30	30	+7 V
31	-14 V	31	31	+14 V
32	-19 V	32	32	A

MOTHERBOARD A12 ---> UNIT A3
X506 ----------> X2102

	ROW A	ROW B	ROW C
1	OETX--LT	CSTX--LT	WETX--LT
2	RDDM--LT	DITXTR	DAAK--LT
3	LEDA--HT	DRTXTR	DPAB11
4	LEDA--LT	DPABØ9	TXAB13
5	VEDBØ9	WRHOPOLT	DAPBØ8
6	VEDB1Ø	WRVEPOLT	DPAB1Ø
7	VEDB11	ANCPY-HT	OETRØ2LT
8	VEDB12	ANEPY-HT	WETRØ2LT
9	EPY-ØØ	DPTR--HT	DPABØØ
10	EPY-Ø1	DIOS--HT	DPABØ3
11	1VDCDB	ENTRHOLT	DPABØ2
12	ENTXLNLT	EPXØØ	DPABØ1
13	EPDBØØ	EPXØ1	CLUPAB
14	EPDBØ1	Z-BL-HT	DPABØ7
15	EPDBØ2	DPABØ5	DPABØ6
16	EPDBØ3	DAAK--HT	DPABØ4
17	EPDBØ4	WETRØ1LT	CPABØØ n.u.
18	EPDBØ5	OETRØ1LT	MXCPAD
19	EPDBØ6	TRAB13	CKSVLA
20	EPDBØ7	DIDBTX	CLDPAB
21	EPDBØ8	DISVLA	LEDC
22	EPDBØ9	EP12--LT	DCDB15
23	EPDB1Ø	EPHO14	SARYAKLT
24	EPDB11	EPX-Ø2	DCDB14
25	CKEPVE	DCDB11	DCDB13
26	DCDBØ9	-	DCDB12
27	DPRJUPLT	Z-OTØ3	SARY
28	-	WRHOVRLT	DCDB1Ø
29	DJAC--HT	DPRJDWLT	SLTR2LLT
30	SM----LT	SLTR1HLT	SLTR2HLT
31	SAPL	PLZEOT	SLTR1LLT
32	PFPY	PU----LT	SYDP

MOTHERBOARD A12 ---> UNIT A4
X508 ----------> X2001

	ROW A	ROW B	ROW C
1	WETX--LT	CSTX--LT	OETX--LT
2	DAAK--LT	DITXTR	RDDM--LT
3	DPAB11	DRTXTR	TXAB13
4	DPABØ8	DPABØ9	DPAB1Ø
5	OETRØ2LT	WETRØ2LT	SADBØ7
6	SADBØ6	DPABØ3	SADBØ5
7	SADBØ3	DPABØ2	SADBØ4
8	SADBØ1	DPABØ1	SADBØ
9	DPABØØ	CLUPAB	SADBØØ
10	SADBØ9	DPABØ7	OFDP
11	DPABØ6	DPABØ5	SADBØ8
12	DPABØ4	DAAK--HT	TCCPCN
13	CPABØØ n.u.	WETRØ1LT	OETRØ1LT
14	MXCPAD	TRAB13	RLDP
15	RSDU--LT	CKSVLA	CNCPCN
16	DIDBTX	CLDPAB	DUABØ8
17	DUABØ9	DISVLA	DUAB11
18	DCDBØØ	DCDBØ2	DUAB1Ø
19	DCDBØ4	DCDBØ5	LEDC
20	DCDBØ7	DCDBØ3	DUABØØ
21	DCDBØ1	DUABØ2	DUABØ1
22	DCDBØ8	DUABØ4	DUABØ3
23	DUABØ6	SADB13	DUABØ5
24	SADB12	SADB15	DUABØ7
25	SADB14	SARYAKLT	DCDB15
26	DCDB13	DCDB14	DCDBØ9
27	DCDB11	DCDBØ6	DCDB12
28	DCDB1Ø	SARY	ENCPSA
29	SLTR2LLT	OTCM	DAVA
30	SLTR2HLT	SLTR1HLT	DIDCLA n.u.
31	-	SLTR1LLT	LEDP
32	-	-	-

MOTHERBOARD A12 ---> UNIT A5
X511 --------------> X1802

ROW A		ROW B		ROW C	
1	SHIELD	1		1	CK16ØØ
2	CKCDOC	2		2	-
3	SHIELD	3		3	-
4	TKSA	4		4	-
5	-	5		5	SADBØ7
6	SADBØ6	6		6	SADBØ5
7	SADBØ3	7		7	SADBØ4
8	SADBØ1	8		8	SADBØ2
9	OFDP	9		9	SADBØØ
10	SADBØ9	10		10	SADB1Ø
11	SADBØ8	11		11	MMPT
12	MMPTØ1	12		12	CHPT
13	CHPTØ1	13		13	SADB11
14	RLDP	14		14	SHIELD
15	SHIELD	15		15	STCV
16	SWCKØ1	16		16	SHIELD
17	SHIELD	17		17	SCEV--HT
18	SYSWTB	18		18	SHIELD
19	SHIELD	19		19	TCEV--LT
20	RSMN	20		20	SHIELD
21	RSMX	21		21	TRRY
22	SHIELD	22		22	TDLD
23	ETCK	23		23	HDOF--LT
24	ZECH	24		24	STSW
25	CDRD	25		25	RSSW
26	-	26		26	TDUF
27	-14V	27		27	D
28	A -	28		28	-
29	+14V	29		29	DAVA
30	+19V	30		30	-
31	A	31		31	LEDP
32	-19V	32		32	FBRY

MOTHERBOARD A12 ---> UNIT A7
X514 ----------> X....

ROW A		ROW B	ROW C	
1	TKSA	1	1	TKSA
2	-	2	2	-
3	SADBØ6	3	3	SADBØ6
4	-	4	4	-
5	-	5	5	-
6	-	6	6	-
7	-	7	7	-
8	-	8	8	-
9	-	9	9	-
10	-	10	10	-
11	MMPT	11	11	MMPT
12	-	12	12	-
13	TCCPCN	13	13	TCCPCN
14	-	14	14	-
15	CNCPCN	15	15	CNCPCN
16	RSDU--LT	16	16	RSDU--LT
17	-	17	17	-
18	-	18	18	-
19	-	19	19	-
20	-	20	20	-
21	TRRY	21	21	TRRY
22	-	22	22	-
23	-	23	23	-
24	-	24	24	-
25	-	25	25	-
26	D	26	26	-
27	D	27	27	-
28	-	28	28	-
29	-19 V	29	29	+19 V
30	-	30	30	-
31	LEDP	31	31	LEDP
32	-	32	32	A

MOTHERBOARD A12 ---> UNIT A8
X517 ----------> X1402

ROW A		ROW B		ROW C	
1	TKSA	1		1	-
2	-	2		2	EC
3	-	3		3	CKDUR1
4	-	4		4	CDRSMO
5	-	5		5	-
6	-	6		6	-
7	-	7		7	-
8	-	8		8	-
9	OFDP	9		9	-
10	-	10		10	-
11	MMPT	11		11	SFSRØ1
12	CHPT	12		12	SFSRØØ
13	TCCPCN	13		13	CO
14	RLDP	14		14	OTLD
15	CNCPCN	15		15	STRLF
16	RSDU--LT	16		16	DUABØ8
17	DUABØ9	17		17	DUAB11
18	ENOFD	18		18	DUAB1Ø
19	-	19		19	RSDUR-LT
20	TRRY	20		20	DUABØØ
21	DUABØ2	21		21	DUABØ1
22	DUABØ4	22		22	DUABØ3
23	DUABØ6	23		23	DUABØ5
24	CYOT	24		24	DUABØ7
25	LEDUR2	25		25	CKF
26	CKDUR3	26		26	RDDURM
27	CSDURM	27		27	SLOFAD
28	SLAM	28		28	ENCPSA
29	OEDUØØ	29		29	OTDIAD
30	OTCM	30		30	DAVA
31	OEDUØ1	31		31	LEDP
32	SYDP	32		32	FBRY

MOTHERBOARD A12 ---> UNIT A9
X519 ----------> X1202

ROW	A	ROW	B	ROW	C
1	-	1		1	-
2	-	2		2	-
3	-	3		3	-
4	-	4		4	-
5	CKDUR1	5		5	SADBØ7
6	SADBØ6	6		6	SADBØ5
7	SADBØ3	7		7	SADBØ4
8	SADBØ1	8		8	SADBØ2
9	OFDP	9		9	SADBØØ
10	SADBØ9	10		10	SADB1Ø
11	SFSRØ1	11		11	SADBØ8
12	SFSRØØ	12		12	-
13	CO	13		13	SADB11
14	OTLD	14		14	RLDP
15	-	15		15	STRLF
16	-	16		16	DUABØ8
17	DUABØ9	17		17	DUAB11
18	ENOFD	18		18	DUAB1Ø
19	RSDUR-LT	19		19	-
20	-	20		20	DUABØØ
21	DUABØ2	21		21	DUABØ1
22	DUABØ4	22		22	DUABØ3
23	DUABØ6	23		23	DUABØ5
24	CYOT	24		24	DUABØ7
25	CKDUR2LT	25		25	CFK
26	CKDUR3	26		26	RDDURM
27	CSDURM	27		27	SLOFAD
28	SLAM	28		28	-
29	OEDUØØ	29		29	OTDIAD
30	-	30		30	-
31	OEDUØ1	31		31	LEDP
32	FBRY	32		32	OFAD

MOTHERBOARD A12 ---> UNIT A10
X522 ----------> X....

ROW	A	ROW	B	ROW	C
1	-	1		1	-
2	-	2		2	-
3	-	3		3	-
4	-	4		4	-
5	EC	5		5	SADBØ7
6	SADBØ6	6		6	SADBØ5
7	SADBØ3	7		7	SADBØ4
8	SADBØ1	8		8	SADBØ2
9	OFDP	9		9	SADBØØ
10	SADBØ9	10		10	SADB1Ø
11	-	11		11	-
12	-	12		12	-
13	-	13		13	SADB11
14	RLDP	14		14	D
15	-	15		15	-
16	-	16		16	D
17	-	17		17	-
18	-	18		18	-
19	-	19		19	-
20	-	20		20	-
21	-	21		21	-
22	-	22		22	-
23	-	23		23	-
24	-	24		24	-
25	+7 V	25		25	-
26	-7 V	26		26	-
27	-14 V	27		27	-
28	A	28		28	CKADOT
29	+14 V	29		29	OTDIAD
30	+19 V	30		30	LEDP
31	A	31		31	FBRY
32	-19 V	32		32	OFAD

MOTHERBOARD A12 ---> UNIT A11
X524 ----------> X607

ROW A		ROW B	ROW C	
1	-	1	1	-
2	-	2	2	-
3	-	3	3	-
4	-	4	4	CDRSMO
5	EC	5	5	SADBØ7
6	SADBØ6	6	6	SADBØ5
7	SADBØ3	7	7	SADBØ4
8	SADBØ1	8	8	SADBØ2
9	-	9	9	SADBØØ
10	SADBØ9	10	10	SADB1Ø
11	-	11	11	SADBØ8
12	-	12	12	-
13	STCV	13	13	SADB11
14	D	14	14	D
15	-	15	15	UPCK16
16	+5D	16	16	+5D
17	-	17	17	-7 V
18	-	18	18	-
19	-	19	19	-14 V
20	-	20	20	+14 V
21	-	21	21	-19 V
22	-	22	22	+19 V
23	-	23	23	-
24	-	24	24	A
25	-	25	25	A
26	-	26	26	-
27	-	27	27	-
28	-	28	28	-
29	-	29	29	OTDIAD
30	-	30	30	-
31	-	31	31	-
32	-	32	32	OFAD

8.12.6 Additional connections

MOTHERBOARD A12 ---> UNIT A14
X526 --> (CABLE)---> X4001

1	ABØ1
2	+5 D
3	ABØ2
4	DBØØ
5	ABØ3
6	DBØ1
7	ABØ4
8	DBØ2
9	DBØ3
10	DBØ4
11	DBØ5
12	DBØ6
13	IOSLØ4LT
14	DBØ7
15	ILØ3--LT
16	UPRD--LT
17	UPWR--LT
18	D
19	D
20	-7 V

MOTHERBOARD A12 ---> UNIT A19
X527 -->(CABLE) ---> X4406

1	A
2	A
3	-5 D
4	BAVO
5	CON
6	+100 V
7	+7 V
8	+7 V
9	-7 V
10	-7 V
11	-14 V
12	-14 V
13	+14 V
14	+14 V
15	-19 V
16	-19 V
17	+19 V
18	+19 V
19	+40 V
20	+40 V

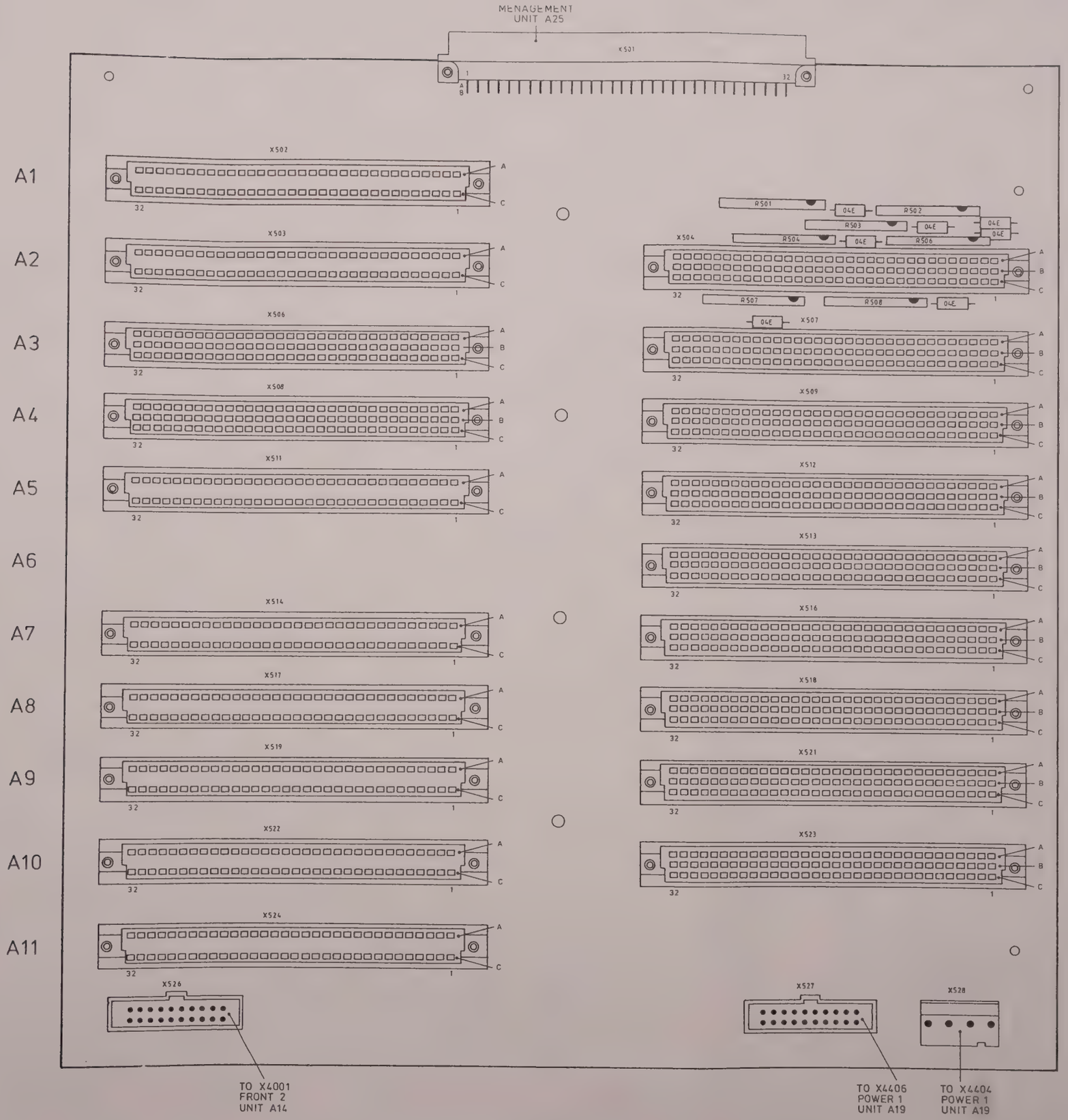


Figure 8.12.2 Unit A12 - MOTHERBOARD - p.c.b. lay-out.

MAT2540
870116

MOTHERBOARD A12 ---> UNIT A25
X501 --> (CABLE)---> X2502

ROW A		ROW B		ROW C
1	ZECH	1	CDRD	1
2	SHIELD	2	ETCK	2
3	RSMN	3	RSMX	3
4	SYSWTB	4	SHIELD	4
5	SWCKØ1	5	SHIELD	5
6	CHPTØ1	6	SHIELD	6
7	SHIELD	7	MMPTØ1	7
8	SHIELD	8	CKCDOC	8
9	-	9	CK16ØØ	9
10	-	10	-	10
11	STCV	11	SHIELD	11
12	SCEV--HT	12	SHIELD	12
13	TCEV--LT	13	SHIELD	13
14	TDLD	14	SHIELD	14
15	STSW	15	HDOF--LT	15
16	TDUF	16	RSSW	16
17	UPWR--LT	17	ILØ6--LT	17
18	DB15 * R507/7	18	UPRD--LT	18
19	DB13 * R507/5	19	DB14 * R507/6	19
20	DB11 * R507/3	20	DB12 * R507/4	20
21	IOSLØ7LT	21	DB1Ø* R507/2	21
22	IOSLØ6LT	22	DBØ9* R503/8	22
23	DBØ7* R503/6	23	DBØ8* R503/7	23
24	DBØ5* R508/7	24	DBØ6* R508/9	24
25	DBØ3* R508/6	25	DBØ4* R508/7	25
26	DBØ2* R508/5	26	ABØ5* -	26
27	DBØ1* R508/4	27	ABØ4* R502/5	27
28	DBØØ* R508/3	28	ABØ3* R502/4	28
29	ABØ1* R502/2	29	ABØ2* R503/3	29
30	D	30	D	30
31	+5 D	31	D	31
32	+5 D	32	+5 D	32

* TERMINATED WITH R.../PINNUMBER

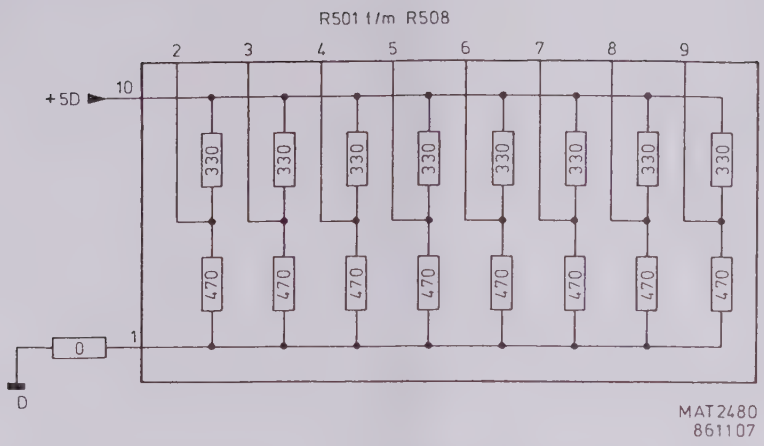
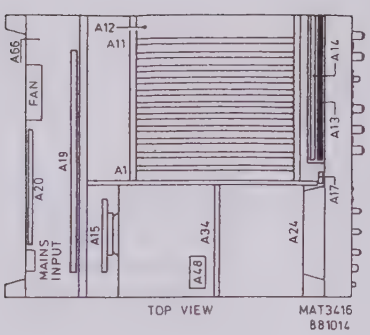


Figure 8.12.3 Unit A12 - MOTHERBOARD - circuit diagram.

UNIT A13 - FRONT 1



CONTENTS

8.13.1 General information..... 8.13-1
8.13.2 Pilot lamps..... 8.13-1
8.13.3 Front-switches..... 8.13-2
8.13.4 Address decoding table..... 8.13-2
8.13.5 Signal name list..... 8.13-2

8.13.1 General information

This front unit contains the front-panel pilot lamps, soft-switches and soft-switches with built-in pilot lamps.

8.13.2 Pilot lamps

The front panel pilot lamps are controlled by the microprocessor via the data bus lines DBØØ ... DBØ7 and latches D4206 and D4207.
Each latch can be activated by an output signal from the decoder D4204. This decoder decodes the three microprocessor address bits ABØ1, ABØ2 and ABØ3 and is enabled by the signals ABØ4, UPWR--LT and IOSLØ4LT.
This is done when the microprocessor generates the front unit addresses and the UPWR--LT signals for the control of the pilot lamps.
Latch D4206 controls the pilot lamps DOTS, SMOOTH, NEGATIVE SLOPE, EXT CLOCK, ALIASED, REP ONLY and NOT TRIG'D.
Latch D4207 controls the pilot lamps UNCAL A, UNCAL B, REMOTE, X-EXPAND UNCAL, LOCK and WRITE.

8.13.3 Front-switches

The settings of all the front-switches are periodically read by the microprocessor system.
The front-switches are therefore placed in a matrix structure.
Eight switches at a time can offer their settings to the inputs of data buffer D4203.
Each row of eight switches can be activated by one of the output signals CNØØ ... CNØ6 from the address decoder D4201. These signals are on a -0,7 V level because of the -0,7 V level on input 3 of D4201. In this way the 0,7 V accross the diodes is compensated and the signals RWØØ ... RWØ7 are brought on a 0 V level.
This decoder decodes the three microprocessor address bits ABØ1, ABØ2 and ABØ3 and is enabled by the signal combination ABØ4, UPRD--LT and IOSLØ4LT.
This combination resulting in signal ENFTSWLT is generated when the microprocessor generates the front unit addresses and the UPRD--LT signals for the reading of the soft-switch settings.
When signal ENFTSWLT is active, front switch buffer D4203 will place the matrix data RWØØ ... RWØ7 on the data bus lines DBØØ ... DBØ7.
The matrix is scanned by the microprocessor, every 40ms.

8.13.4 Address decoding table

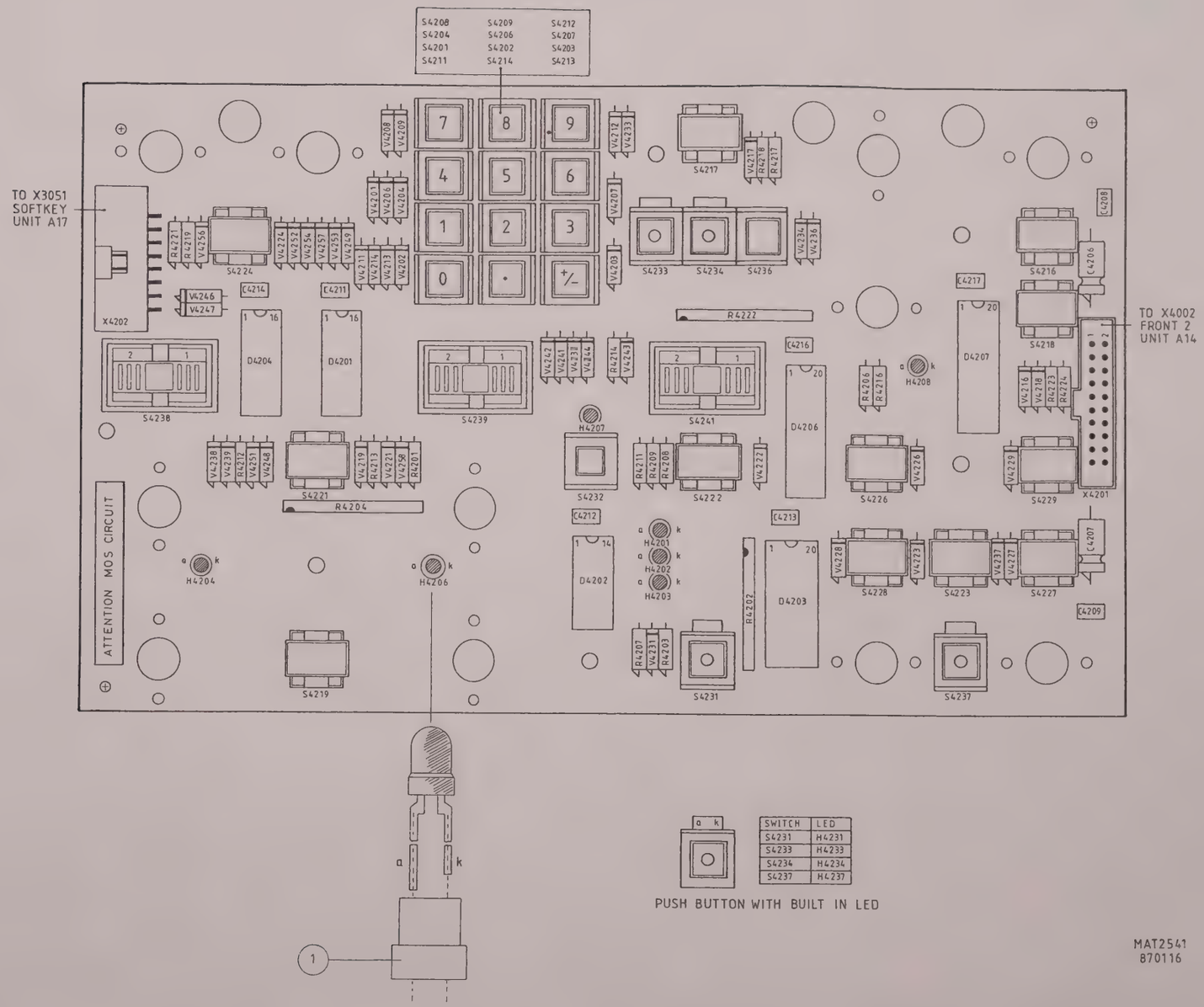
The addresses which are generated by the microprocessor are decoded by address decoders D4204 and D4201 according to the following table.

IOSLØ4LT	ABØ4	ABØ3	ABØ2	ABØ1	Function WR	RD
0	0	0	0	0	Leds (4206)	CNØØ
0	0	0	0	1	Leds (4207)	CNØ1
0	0	0	1	0		CNØ2
0	0	0	1	1		CNØ3
0	0	1	0	0		CNØ4
0	0	1	0	1		CNØ5
0	0	1	1	0		CNØ6

8.13.5 Signal name list

UNIT A13

Signal name	Description	Signal source	Signal destination(s)
ABØ1...Ø4	Address bus	A6+option	-
CNØØ...Ø6	Count ØØ...Ø6	A13	A13
COMMON1	Common line 1	A13	A18
COMMON2	Common line 2	A13	A17
DBØØ...Ø7	Data bus ØØ...Ø7	A6+option	-
ENFTSWLT	Enter front switch	A13	A13
IOSLØ4LT	I/O select Ø4	A6	-
RWØ...Ø7	Row ØØ...Ø7	A13	A13
UPRD--LT	Microprocessor read	A6	-

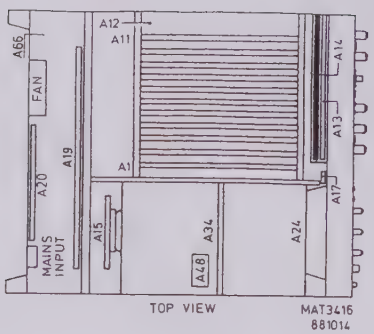


SWITCH	LED
S4231	H4231
S4233	H4233
S4234	H4234
S4237	H4237

PUSH BUTTON WITH BUILT IN LED

MAT2541
870116

Figure 8.13.1 Unit A13 - FRONT 1 - p.c.b. lay-out.



CONTENTS

8.14.1 General information..... 8.14-1
8.14.2 Optical switches..... 8.14-2
8.14.3 Address decoding table..... 8.14-3
8.14.4 Signal-name list..... 8.14-3

8.14.1 General information

This front unit contains all the front-panel optical switches and their photo-sensitive transistors.
There are ten identical optical switches for the following functions:

X-POSITION
X-EXPAND
VARIABLE-B
Y-POSITION
SHIFT-A
VARIABLE-A
SHIFT-B
1st CURSOR
2nd CURSOR
LEVEL

8.14.2 Optical switches

The rotation of an optical switch is detected by the two internal photo-transistors. If the control is turned from one position to another, light from the infra-red LED's falls in the photo-transistors, pulsed via the holes in a perforated disc. As a result, the photo-transistors conduct for some time and their collectors are low.

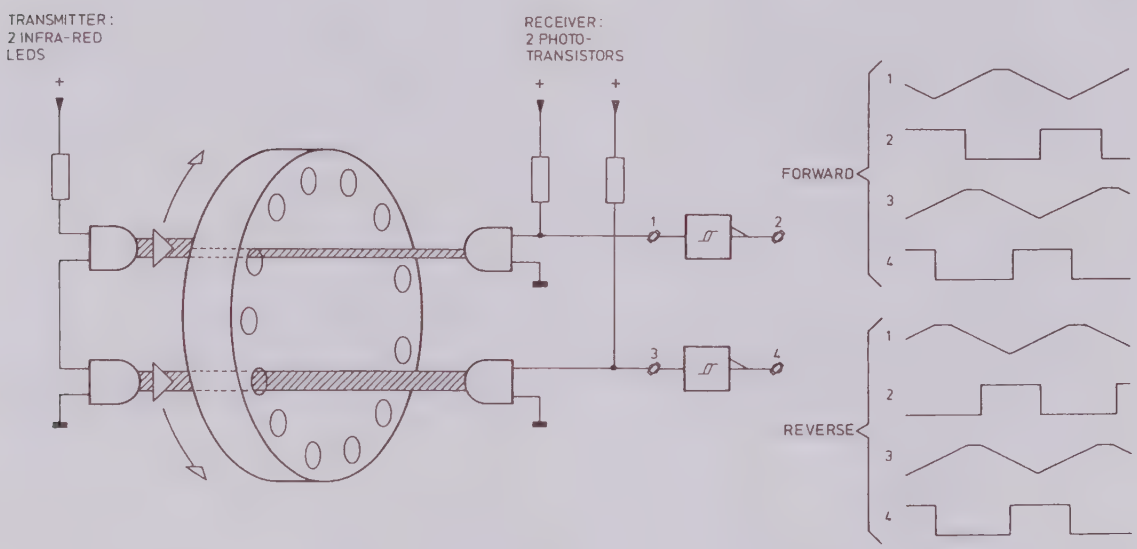


Figure 8.14.1 Optical switches MAT 2481

The collector signals of the photo-transistors are applied to three 3-state registers D4012, D4011, and D4009 as rotate forward signals RTFWØ1 ... RTFW12 and rotate backward signals RTBWØ1 ... RTBW12. This is done via SCHMITT-trigger inverters for good pulse definition.

If one of the optical switches is operated, the relevant RTFW.. pulse is used for the generation of an interrupt level pulse ILØ3PU on output point 9 of NAND D4014 on each positive or negative going signal edge.
This pulse is used as clockpulse for the D-type flip flop D4016, resulting in an interrupt level signal ILØ3--LT which interrupts the microprocessor. This is done to realize a very quick reaction by the microprocessor when an optical switch is operated.

The flip flop output signal ILØ3--HT is used to clock the actual photo-transistor output levels in the three 3-state registers via the databus lines DBØØ ... DBØ7 for further processing.
In this way the microprocessor knows which switch is operated and in which direction.
The microprocessor will be interrupted by signal ILØ3--LT and generates in turn three different addresses and the UPRD--LT signals in order to read the contents of the 3-state registers.
If a front unit address is generated, the IO select signal IOSLØ4LT for the front unit will be active.

ROTARY ENCODER

OPTICAL SWITCHES

X-POSITION

X-EXPAND

VARIABLE-B

Y-POSITION

SHIFT-A

VARIABLE-A

SHIFT-B

1st CURSOR

2nd CURSOR

LEVEL

HOLD-OFF

ONLY IN GHz VERSION

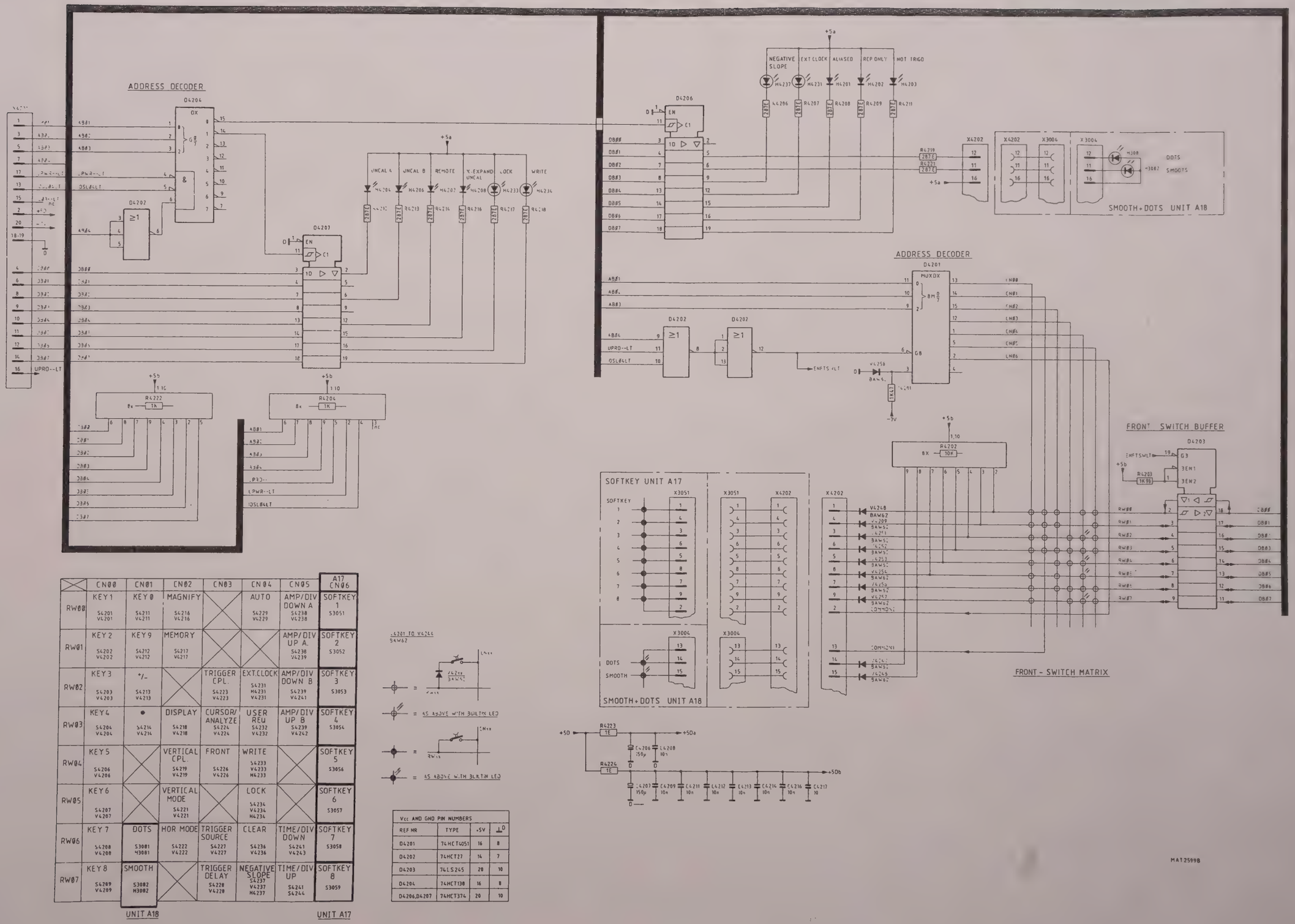
3-STATE REGISTER

ADDRESS DECODER

REF NR	TYPE	Vcc AND GND PIN NUMBERS +5t	+5r	⊥ G
D4001 D4002 D4008 D4012	HEF40106		14	7
D4003 D4004 D4007	HEF4070		14	7
D4006	HEF4082		14	7
D4009 D4011 D4012	74HCT374	20		10
D4013	74HCT138	16		8
D4014	HEF4073		14	7
D4016	HEF4013		14	7

MAT 26008

Figure 8.14.3 Unit A14 - FRONT 2 - circuit diagram.



	CN00	CN01	CN02	CN03	CN04	CN05	A17 CN06
RW00	KEY 1 S4201 V4201	KEY 0 S4211 V4211	MAGNIFY S4216 V4216		AUTO S4229 V4229	AMP/DIV DOWN A S4238 V4238	SOFTKEY 1 S3051
RW01	KEY 2 S4202 V4202	KEY 9 S4212 V4212	MEMORY S4217 V4217			AMP/DIV UP A. S4238 V4239	SOFTKEY 2 S3052
RW02	KEY 3 S4203 V4203	+/- S4213 V4213		TRIGGER CPL. S4223 V4223	EXT.CLOCK S4231 H4231 V4231	AMP/DIV DOWN B S4239 V4241	SOFTKEY 3 S3053
RW03	KEY 4 S4204 V4204	• S4214 V4214	DISPLAY S4218 V4218	CURSOR/ ANALYZE S4224 V4224	USER REV S4232 V4232	AMP/DIV UP B S4239 V4242	SOFTKEY 4 S3054
RW04	KEY 5 S4206 V4206		VERTICAL CPL. S4219 V4219	FRONT S4226 V4226	WRITE S4233 V4233 H4233		SOFTKEY 5 S3056
RW05	KEY 6 S4207 V4207		VERTICAL MODE S4221 V4221		LOCK S4234 V4234 H4234		SOFTKEY 6 S3057
RW06	KEY 7 S4208 V4208	DOTS S3081 H3081	HOR MODE S4222 V4222	TRIGGER SOURCE S4227 V4227	CLEAR S4236 V4236	TIME/DIV DOWN S4241 V4243	SOFTKEY 7 S3058
RW07	KEY 8 S4209 V4209	SMOOTH S3082 H3082		TRIGGER DELAY S4228 V4228	NEGATIVE SLOPE S4237 V4237 H4237	TIME/DIV UP S4241 S4244	SOFTKEY 8 S3059

UNIT A18 — UNIT A17

Vcc AND GND PIN NUMBERS			
REF NR	TYPE	+5V	⊥
D4201	74HCT4051	16	8
D4202	74HCT27	14	7
D4203	74LS245	20	10
D4204	74HCT138	16	8
D4206,D4207	74HCT374	20	10

Figure 8.13.2 Unit A13 - FRONT 1 - circuit diagram.

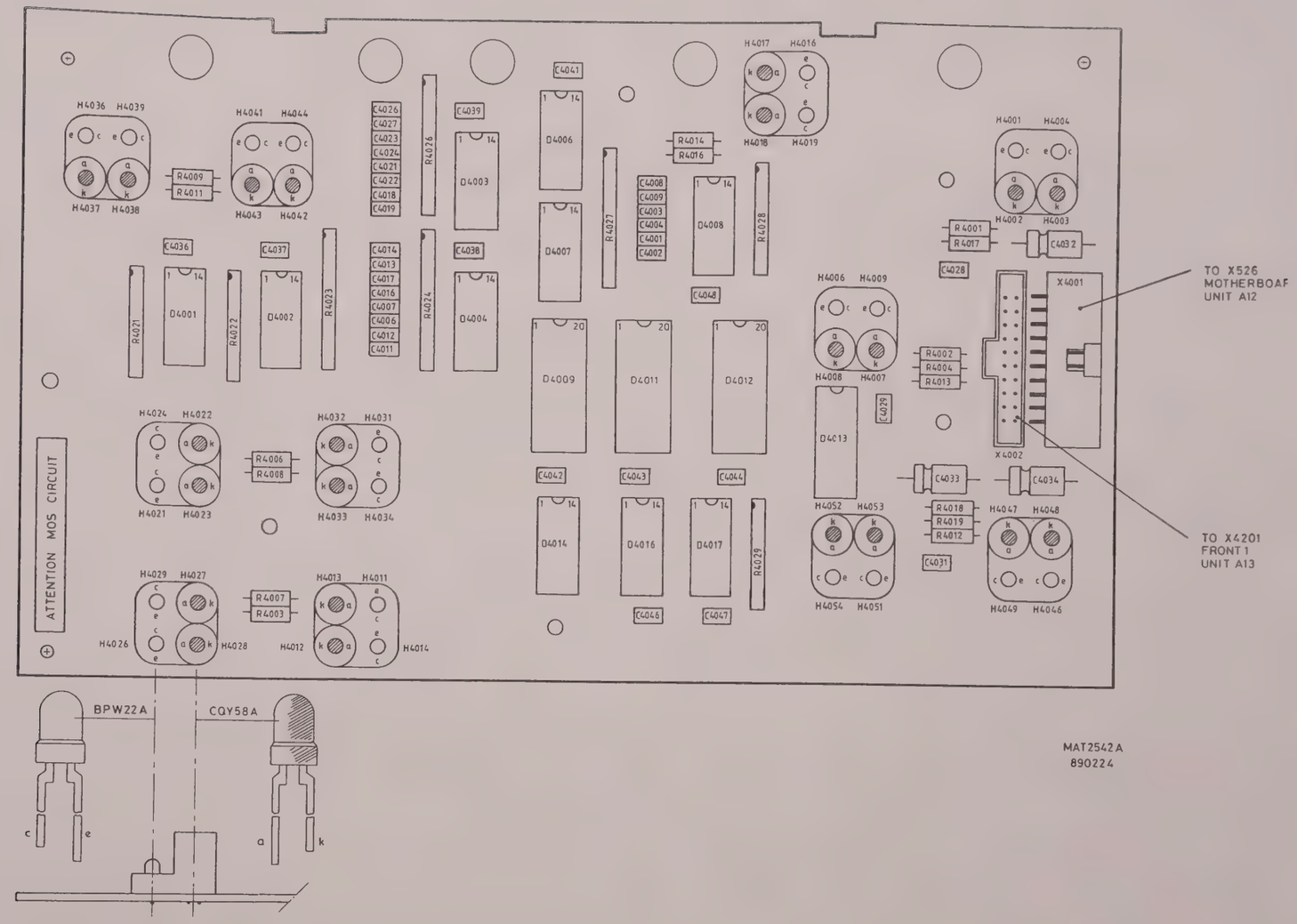


Figure 8.14.2 Unit A14 - FRONT 2 - p.c.b. lay out.

Selection of one of the 3-state registers is achieved then by decoder D4013, which decodes the three microprocessor address lines ABØ1, ABØ2 and ABØ3. This results then in one active low decoder output line (enable rotate) ENRTØ1, ENRTØ2 or ENRTØ3. This are the output enable signals for the three 3-state registers and the one which is enabled places its data on the microprocessor data bus lines DBØØ... DBØ7.
During the read cycle, flip flop D4016 will be set to its zero state again by signal ENRTØ1.

8.14.3 Address decoding table

The addresses which are generated by the microprocessor are decoded by address decoder D4013 according to the following table.

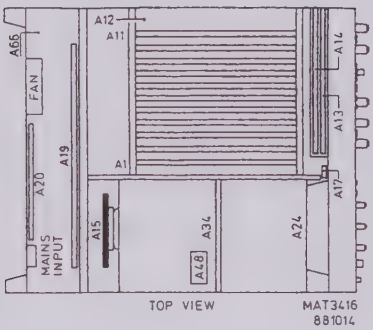
IOSLØ4LT	ABØ4	ABØ3	ABØ2	ABØ1	Function
0	1	0	0	0	ENRTØ1
0	1	0	0	1	ENRTØ2
0	1	0	1	0	ENRTØ3

8.14.4 Signal name list

UNIT A14

Signal name	Description	Signal source	Signal destination(s)
ABØ1...Ø4	Address bus Ø1...Ø4	A6+option	-
DBØØ...Ø7	Data bus ØØ...Ø7	A6+option	-
ENRTØ1	Enable rotate Ø1	A14	-
ENRTØ2	Enable rotate Ø2	A14	-
ENRTØ3	Enable rotate Ø3	A14	-
ILØ3--LT	Interrupt level Ø3	A14	A6
ILØ3--HT	Interrupt level Ø3	A14	-
ILØ3PU	Interrupt pulse	A14	-
IOSLØ4LT	I/O select Ø4	A6	-
RTBWØ1...12	Rotate backward Ø1...12	A14	-
RTFWØ1...12	Rotate forward Ø1...12	A14	-
UPRD--LT	Microprocessor read	A6	-
UPWR--LT	Microprocessor write	A6	-

UNIT A15 - Z AMPLIFIER UNIT



CONTENTS

8.15.1 General information..... 8.15-1
8.15.2 Final Z-stage..... 8.15-1
8.15.3 Final focus stage..... 8.15-1
8.15.4 Signal name list..... 8.15-2

8.15.1 General information

This unit basically comprises a Z-demodulator circuit, a final Z-stage and a final focus stage.

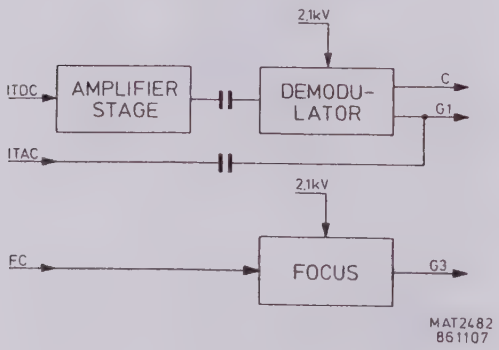


Figure 8.15.1 Blockdiagram final Z-stage.

8.15.2 Final Z-stage

The high frequency component ITAC of the Z-signal is fed via a high voltage capacitor C2806 to the high voltage part of the circuit.
The modulated low frequency component ITDC of the Z-signal is fed via a high voltage capacitor C2803 to a demodulator circuit in the high voltage part of the circuit.
The resulting demodulated signal is then combined with the high frequency component from C2806 and applied to the intensity grid G1 of the C.R.T.

8.15.3 Final focus stage

The focus signal FC is applied to the final focus stage brought on a correct level and applied to the focus grid G3 of the C.R.T.

8.15.4 Signal name list

Signal name	Description	Signal source	Signal destination(s)
f1	Filament 1	A20	-
f2	Filament 2	A20	-
FC	Focus	A1	-
ITAC	Intens a.c. component	A1	-
ITDC	Intens d.c. component	A1	-
X1	X1 input for C.R.T.	A1	-
X2	X2 input for C.R.T.	A1	-
Y1	Y1 input for C.R.T.	A1	-
Y2	Y2 input for C.R.T.	A1	-
-2,1 kV	-2,1 kV C.R.T.	A20	-

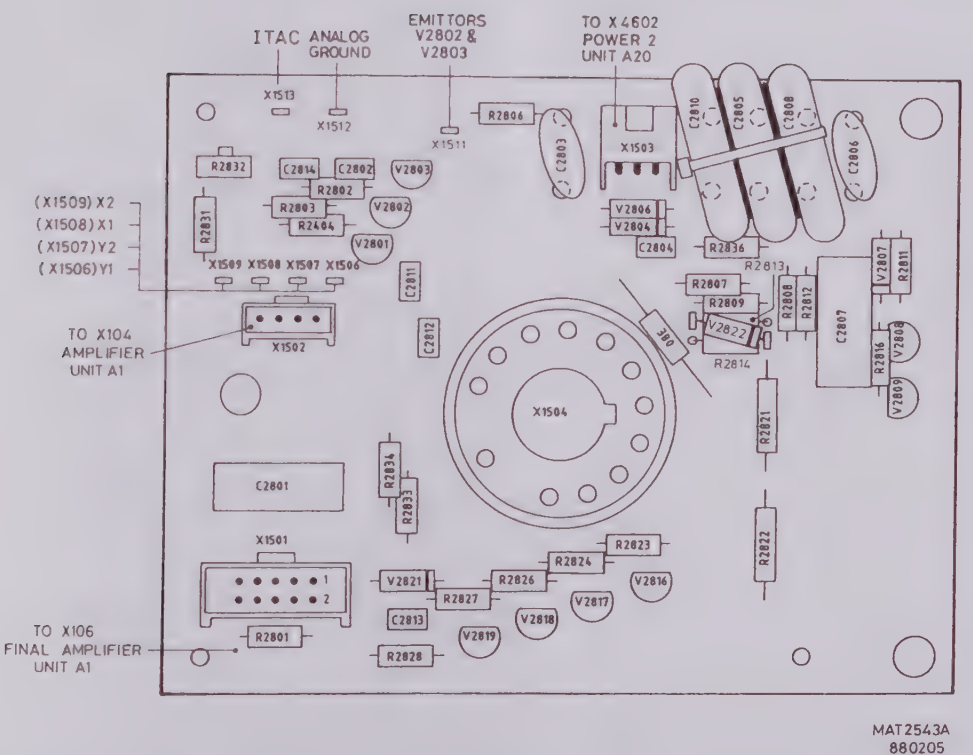


Figure 8.15.2 Unit A15 - Z-AMPLIFIER - p.c.b. lay-out.

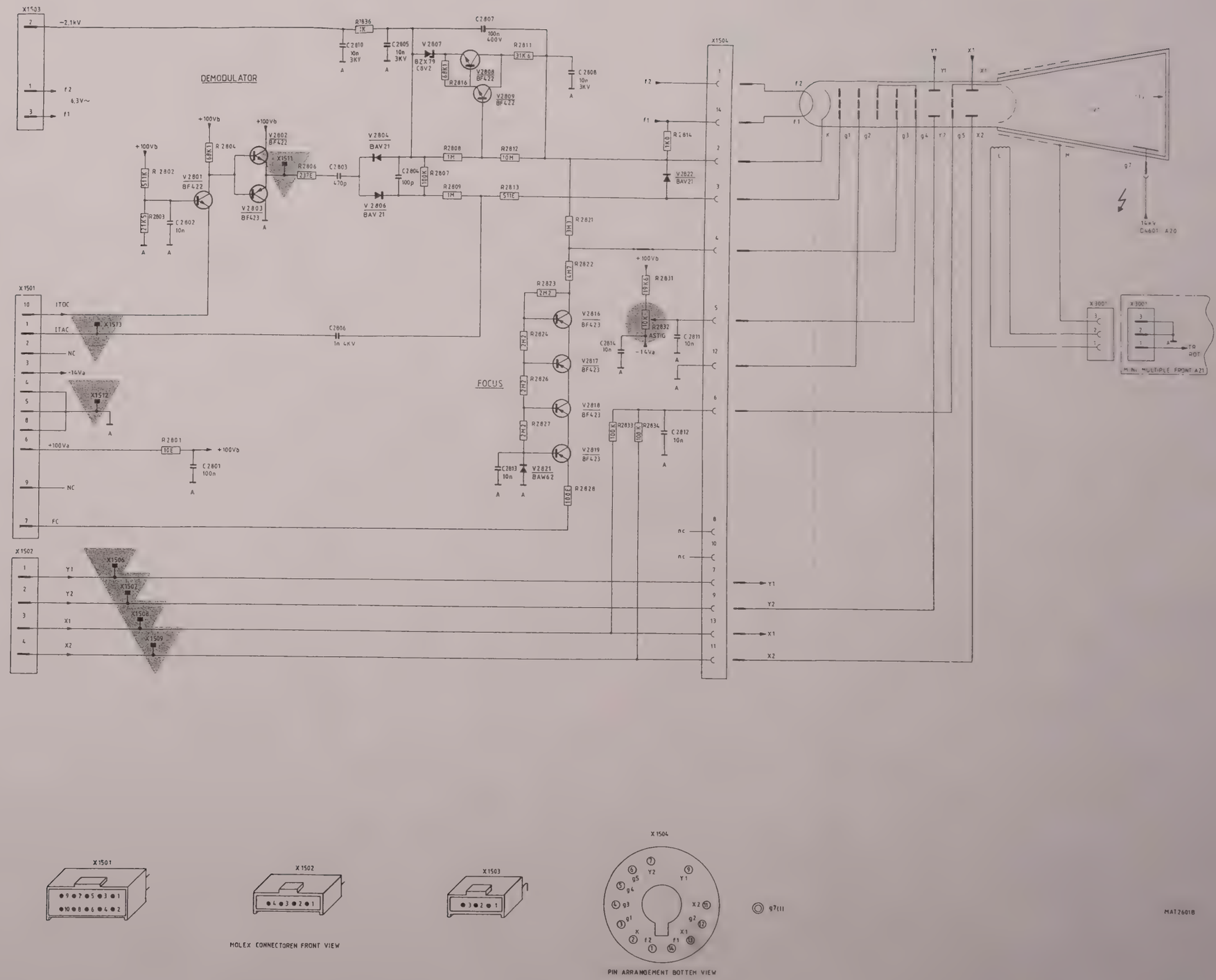
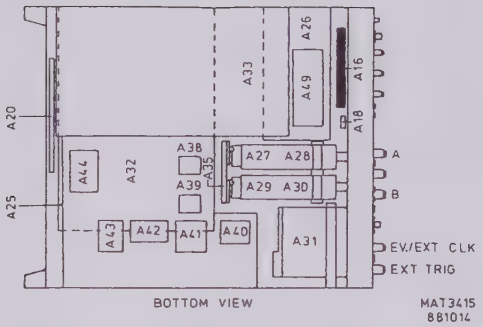


Figure 8.15.3 Unit A15 - Z-AMPLIFIER - circuit diagram.

UNIT A16 - C.R.T CONTROL UNIT



CONTENTS

8.16.1 General information..... 8.16-1
8.16.2 Signal name list..... 8.16-2

8.16.1 General information

The C.R.T. CONTROL unit, which is located below the C.R.T., contains the frontpanel C.R.T. controls:

- FOCUS
- INTENS TRACE
- INTENS TEXT
- ILLUM
- TRACE ROT

The FOCUS level FCIN is applied to the focus circuit on unit A1.

The INTENSITY levels ITTR and ITTX are applied to unit A1 and depending on the current display block (trace or text) one of these two (trace or text) levels will be selected and applied to the Z-amplifier.

8.16.2 Signal name list

Signal name	Description	Signal source	Signal destination(s)
FCIN	Focus input	A16	A1
ITTR	Intensity trace	A16	A1
ITTX	Intensity text	A16	A1
TRRT	Trace rotation	A16	C.R.T.

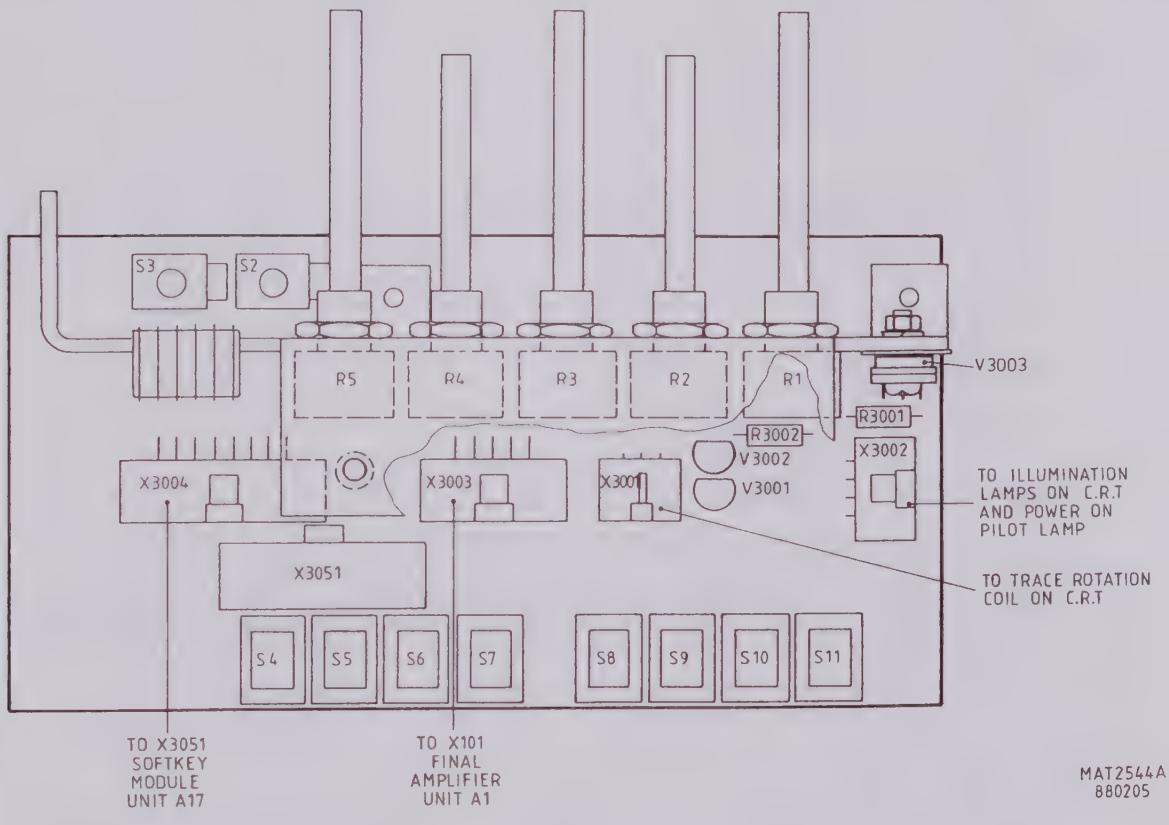


Figure 8.16.1 Unit A16 - C.R.T. CONTROL - p.c.b. lay out.

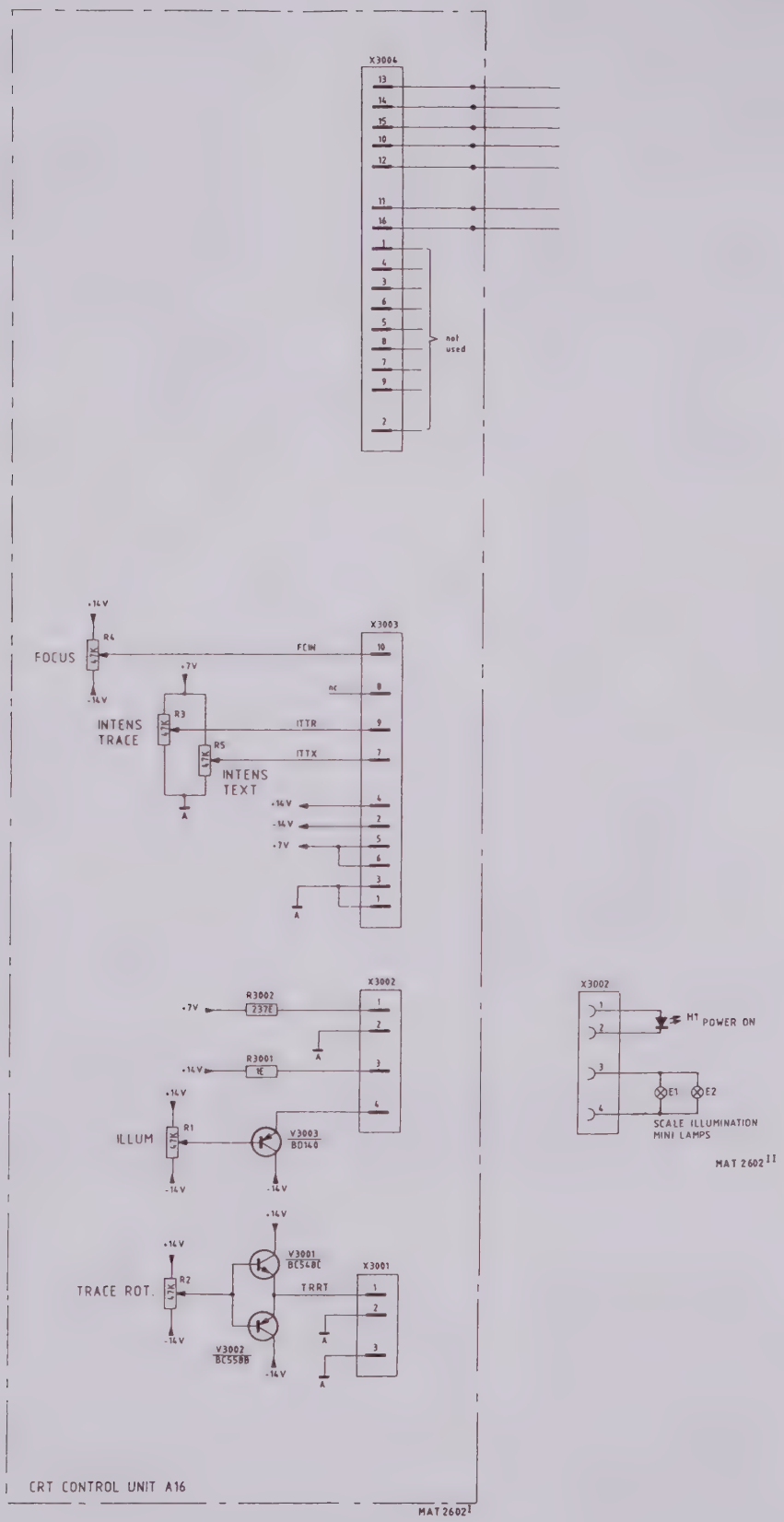
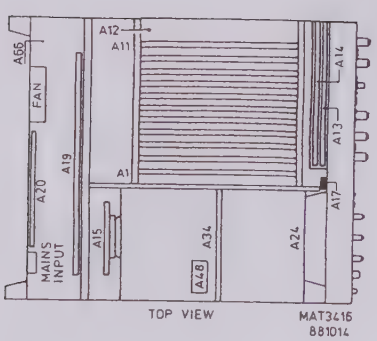


Figure 8.16.2 Unit A16 - C.R.T. CONTROL - circuit diagram.

UNIT A17 - SOFTKEY UNIT



CONTENTS

8.17.1 General information..... 8.17-1

8.17.1 General information

The SOFTKEY unit, which is located on the right side of the C.R.T., contains the row of eight frontpanel softkey switches.

See also section 8.13 FRONT 1.

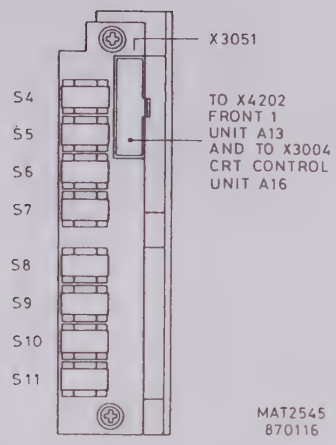


Figure 8.17.1 Unit A17 - SOFTKEY UNIT - p.c.b. lay-out.

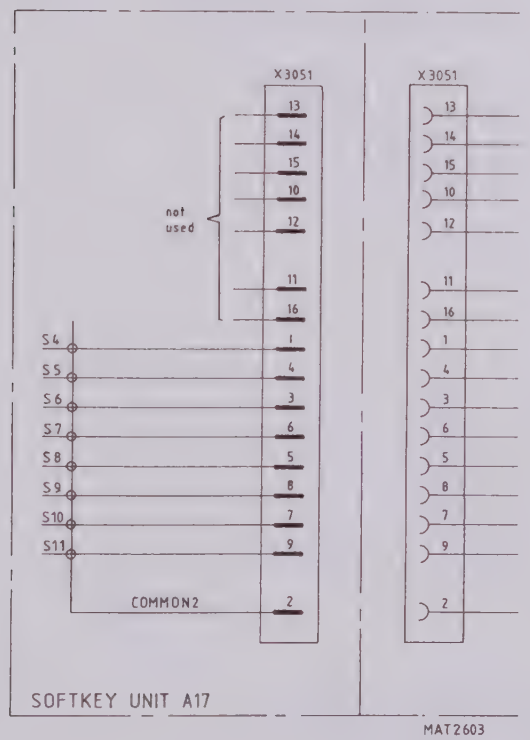
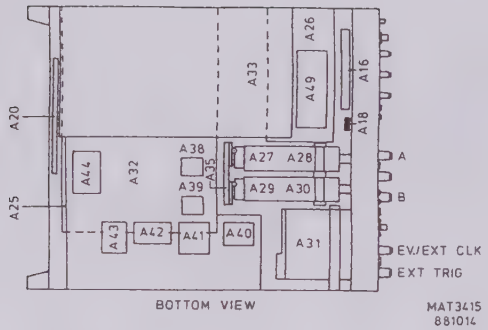


Figure 8.17.2 Unit A17 - SOFTKEY UNIT - circuit diagram.

UNIT A18 - SMOOTH + DOTS UNIT



CONTENTS

8.18.1 General information..... 8.18-1

8.18.1 General information

The SMOOTH + DOTS unit, which is located below the C.R.T., contains the switches DOTS and SMOOTH including the leds.

See also section 8.13 FRONT 1.

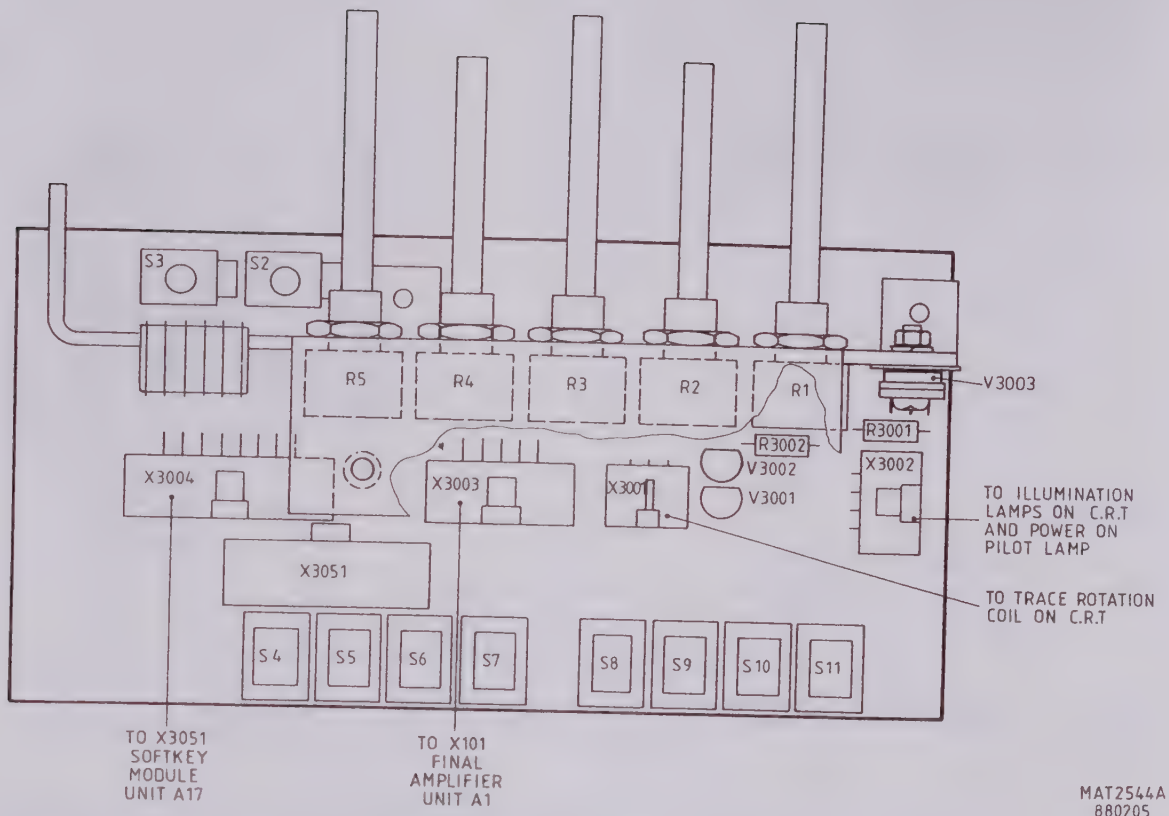


Figure 8.18.1 Unit A18 - SMOOTH + DOTS UNIT - p.c.b. lay-out.

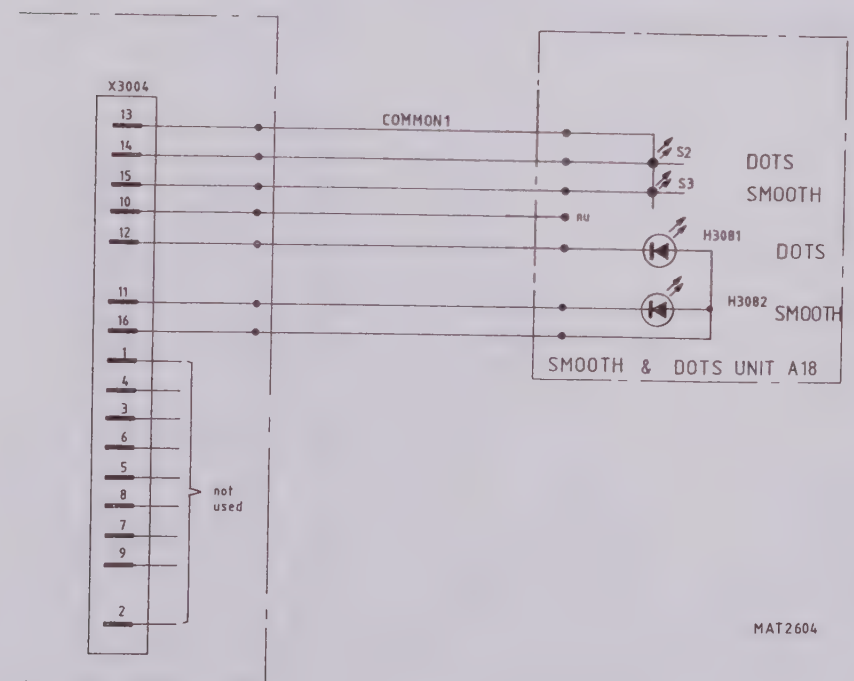
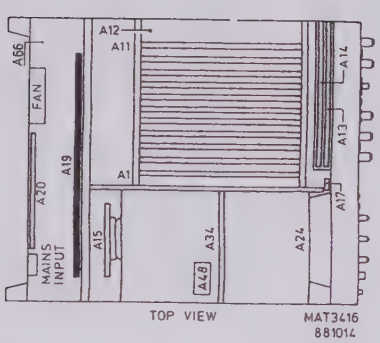


Figure 8.18.2 Unit A18 - SMOOTH + DOTS UNIT - circuit diagram.

UNIT A19 - POWER 1



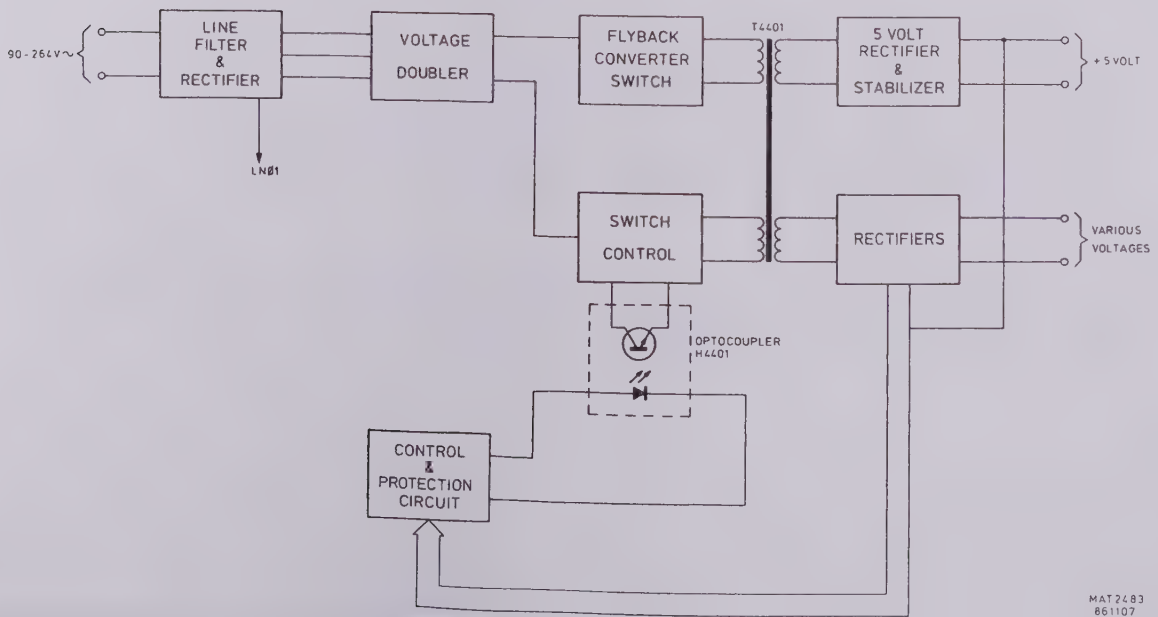
CONTENTS

8.19.1 General information..... 8.19-1
8.19.2 The mains filter and rectifier..... 8.19-2
8.19.3 The voltage doubler..... 8.19-2
8.19.4 The flyback converter switch..... 8.19-3
8.19.5 The switch control..... 8.19-3
8.19.6 The control circuit..... 8.19-5
8.19.7 The protection circuit..... 8.19-6
8.19.8 The +5 Volt stabiliser..... 8.19-6
8.19.9 The rectifiers..... 8.19-7
8.19.10 Signal name list..... 8.19-7

8.19.1 General Information

WARNING: The complete circuit is at mains potential up to transformer T4401 and opto-coupler H4401. To avoid any electrical shock, it is strongly recommended to read section 10.1 first.

The block diagram below shows the parts of this unit.



The line voltage is applied via a line filter and a rectifier to a voltage doubler. The voltage is only doubled if the line voltage is below 140 V.
The output voltage of the voltage doubler is applied to transformer T4401 via a flyback converter, which consists of a flyback converter switch and a switch control circuit.
The switch control is influenced by the control and protection circuit via opto-coupler H4401. The latter and transformer T4401 perform a galvanic separation of the instrument from the line voltage.
The various output voltages of transformer T4401 are controlled by the control & protection circuit, which gives protection against over- and undervoltage and a too high temperature.
The +5 V for the digital circuitry has a separate stabilizer.
When the power is on, the POWER ON led on the front panel lights. This led is connected to +7 V on the CRT control unit A16.

8.19.2 The Mains filter and rectifier

The mains input (90 V...264 Vac) is filtered by a mains filter, consisting of C4401 and L4401 and fed into a full bridge rectifier (V4401...4404).
Resistors R4402 and R4403 have a surge current limiting function.
A capacitive network C4402...C4407 across the input serves to reduce interference, the centre-point being coupled to earth to provide electromagnetic compatibility. C4403 and R4401 provide a trigger pick-off point LNØ1 for LINE triggering.

8.19.3 The voltage doubler

To avoid the flyback converter switching high currents a voltage doubler has been provided. This doubler is switched off at high input voltages.
The principle of the voltage doubler is given in figure 8.19.2.

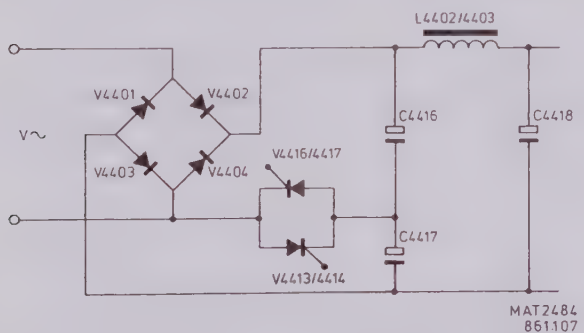


Figure 8.19.2 Simplified diagram of the voltage doubler.

The thyristors are turned on if the output voltage of the doubler is below 200 V approx. (double output voltage).
They are turned off if the output voltage rises above 400 V approx.

If the thyristors are off, the ac-voltage charges the series connection of C4416 and C4417 to the peak value. The voltage on both capacitors is smoothed by L4402/4403 and C4418.

If the thyristors are on, the positive phase of the ac-voltage charges C4416 via V4402 and V4416/17 to the peak value.
The negative phase charges C4417 via V4401 and V4413/4414 to the peak value.
The voltage on the series connection of C4416 and C4417, which is twice the peak voltage of Vac, is smoothed by L4402/4403 and C4418.

The thyristors are switched on and off by a schmitt-trigger circuit consisting of V4406/4408, V4407 and their associated components.

8.19.4 The flyback converter switch (see also figure 8.19.3)

The switch consists of a power transistor V4429, connected in series with diode V4419. The transistor is switched by 2 MOSFETS V4424/V4426, which are controlled by the switch control. By regulating the on and off periods of the switch, the output voltages of T4401 are controlled. The other components of the switch serve as a dV/dt limiter to decrease the switching dissipation, to reduce interference and to protect the switching transistors against overvoltages.

8.19.5 The switch control

The switch control is a rather complicated circuit, which will be explained by the simplified circuit diagram of figure 8.19.3.
After power on, a current via R4434/4436 and the b-c diode of V4433 charges C4423 until the treshold voltage of the FET is reached, after which the converter switch turns on. The current through winding 1-2 of T4401 and R4448...R4452 increases linearly and charges T4401.
This causes a linearly increasing voltage on winding 3-4, which turns the converter switch further on.
This is the forward stroke.

If the voltage over R4448...R4452 rises above 1,2 V the cathode-gate voltage of thyristor V4441 rises above 0,6 V and it will be fired.
The NTC resistor R4444 provides temperature compensation for the firing point of the thyristor.
Now the converter switch is blocked and the flyback stroke starts, during which the secondary windings of T4401 discharge via the rectifiers into the smoothing capacitors.
In this situation winding 3-4 of the transformer gives a negative voltage, which charges C4423 as indicated. The output voltage of V4433 will be zero, so the thyristor extinghuishes.

If the transformer is discharged, the output voltage of winding 3-4 drops to zero and C4423 supplies a positive voltage to V4433, which will turn the converter switch on. The forward stroke starts again and so on.

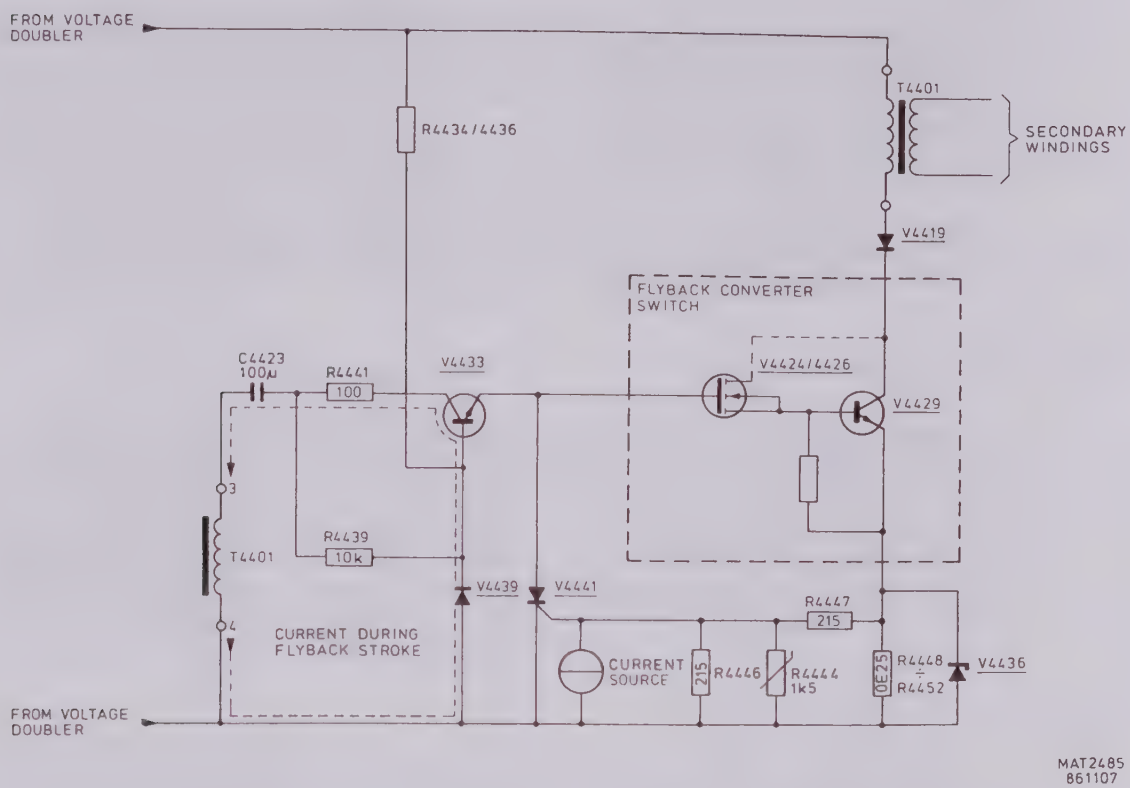


Figure 8.19.3 Simplified diagram of the flyback converter switch.

V4433, R4439 and V4439 form a voltage stabilizer circuit during the forward stroke, which limits the voltage on the gates of the MOSFETS to 15 V. The switching frequency varies from 20 kHz to 40 kHz, depending on the input voltage.

By inserting a current in R4446 with a current source, the on/off time of the converter switch (duty cycle) can be influenced. This is used to control the output voltages of T4401.
The current source is realised with opto-coupler H4401, which is supplied by C4424. This capacitor is charged during the forward stroke via V4438.
The opto coupler is controlled by the control and protection circuit.

If one or more of the transistors of the converter switch are blown, the zenerdiode V4436 prevents the burning out of R4448...R4452 and the whole switch control circuit, because it blows itself and makes a short circuit over R4448...R4452.
Afterwards, the mains fuse will blow.
If, after having replaced the converter switch transistors and the mains fuse, the power is turned on again, the thyristor V4441 can't be fired due to the short circuit of V4436. In consequence the converter switch won't be turned off and the TRANSISTORS and MAINS FUSE will BLOW AGAIN.

WARNING: Replace always zenerdiode V4436 after having replaced one or more converter switch transistors (V4424, V4426 and V4429) and the mains fuse.

8.19.7 The protection circuit

The protection circuit gives the protection against:

- overvoltage on +5D
- overvoltage on +14 V
- too high temperature
- undervoltage on -7 V

The signal C-ON serves as a power supply for this circuit.
Overvoltage on +5D or on +14 V makes V4476 conducting. A too high temperature (e.g. caused by a failure of the fan) also makes V4476 conducting, due to the effect of PTC R4469.
V4476 makes V4474 conducting and via R4459 both transistors keep themselves conducting.
Now V4474 supplies a high current into the opto-coupler, which makes the forward stroke very short and eliminates the overvoltage.

If there is a short circuit in one of the voltage on the secondary side of the transformer all voltages will drop, the -7 V inclusive. This causes V4473 to conduct, due to a voltage rise on the node V4471, R4461, V4472. Next V4471 conducts, which makes the forward stroke very short. No components will be overcharged in this way, in spite of the short circuit.
To prevent the undervoltage protection being active immediate after power on, a delay circuit consisting of R4461 and C4461 is provided. After an over- or undervoltage detection C4461 is discharged fastly by the mains switch, which has a contact connected to connector X4402, when the oscilloscope is switched off.

8.19.8 The +5 volt stabilizer

The output voltage of winding 10-20 of transformer T4401 depends on the load of the +14 V, because this voltage is regulated by the control unit by means of the flyback stroke.
To get a stable +5 V power supply for the digital circuits (+5D) a stabilizer is provided, which works during the forward stroke (forward converter).
During the positive phase of winding 10-20 (the forward stroke), C4429 is charged via L4408, V4449 and L4409. The voltage on C4429 is smoothed by L4411/4412 and C4431.
During the negative phase (the flyback stroke), V4451 acts as a flywheel diode for L4409.
There also flows a current from +5D through V4486, and V4484 in the reverse direction through choke L4408. This demagnetises the core of L4408 or even magnetises it in the reverse direction, depending on the value of the reverse current.
During the forward stroke, the core of L4408 has to be magnetised again. The more the core has to be magnetised, the higher the self inductance will be and the lower the voltage on C4429 and C4431 will be.
A lower voltage on +5D causes the operational amplifier N4401 to give a higher output voltage. The transistor V4486 conducts less, the reverse current through choke L4408 and so the self inductance decrease and so the voltage on C4429 and C4431 rises.
RV10 serves as a reference voltage.

Figure 8.19.4 shows some wave-forms in the flyback converter.

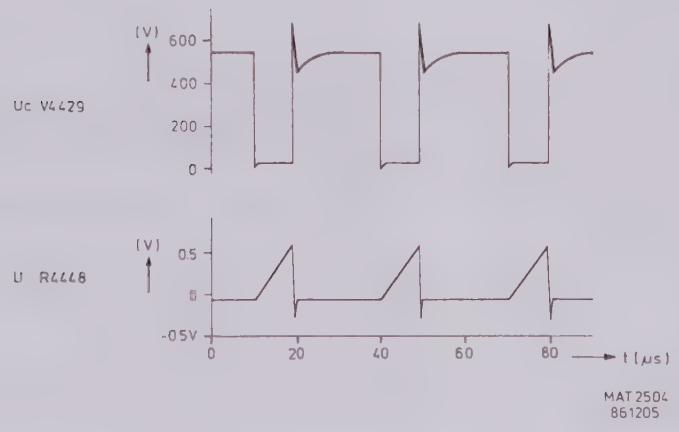


Figure 8.19.4 Voltage waveforms in the flyback converter.

8.19.6 The control circuit

This circuit consists of an operational amplifier (N4401) with some associated components.
The rectified and smoothed +14 V is fed back to the op-amp and compared with the 10 V reference voltage, RV10, which comes from unit A20.
If the +14 V is too high, the op-amp supplies more current into the opto coupler. Next, the opto coupler supplies more current into R4446, which causes the thyristor V4441 to be fired earlier. This shortens the forward stroke, so transformer T4401 is charged less. Next the flyback stroke will be shorter and the smoothing capacitors will be charged less and the output voltages, +14 V inclusive, decrease. So only the +14 V is regulated. All the other voltages are not regulated, except the +5 volt (+5D).
Because the output voltages depend on the length of the flyback stroke, the flyback stroke is regulated by the control circuit.
The +5D has a separate stabilizer, which works during the forward stroke (see 8.19.8)

Resumed:

- If the load on +14 V varies, the forward and the flyback stroke vary. The duty cycle remains constant; the frequency varies.
- If the input voltage varies, only the forward stroke varies; the flyback stroke remains constant. A higher input voltage results in a shorter forward stroke.
- The load on the +5D influences only the waveform of primary current through transformer T4401 during the forward stroke. The frequency and the duty cycle remain constant.

VOLTAGE DOUBLER

FLYBACK CONVERTER SWITCH

5V STABILIZER

MAINS VOLTAGE 90-264V~

WARNING
THE CIRCUIT IS UP TO T4401 AND H4401 AT MAINS VOLTAGE LEVEL

SWITCH CONTROL

PROTECTION CIRCUIT

CONTROL CIRCUIT

RECTIFIERS

ASSY FRAME REAR A66

MAT 26058

Figure 8.19.6 Unit A19 - POWER 1 - circuit diagram.

8.19.9 The rectifiers

The rectifiers consist of standard rectifying circuits with smoothing filters.

8.19.10 Signal name list

UNIT A19

Signal name	Description	Signal source	Signal destination(s)
BAVO	Battery voltage	A66	-
C-ON	Converter on	A19	A19,A20
FRUVP	Fast reset under voltage protection	A19	A66
ILØ7--LT	Interrupt level Ø7	A20	-
LNØ1	Line Ø1	A19	A20
M1	Mains 1	A66	-
M2	Mains 2	A66	-
PE	Protective earth	A66	-
RVG	Reference voltage ground	A20	-
RV1Ø	Reference voltage 1Ø V	A20	-
A	Analogue ground	A19	General
D	Digital ground	A19	General
+5D	+5 Volt digital	A19	General
-5D	-5 Volt digital	A19	General
+7V	+7 Volt	A19	General
-7V	-7 Volt	A19	General
+14V	+14 Volt	A19	General
-14V	-14 Volt	A19	General
+19V	+19 Volt	A19	General
-19V	-19 Volt	A19	General
+40V	+40 Volt	A19	General
+100V	+100 Volt	A19	General

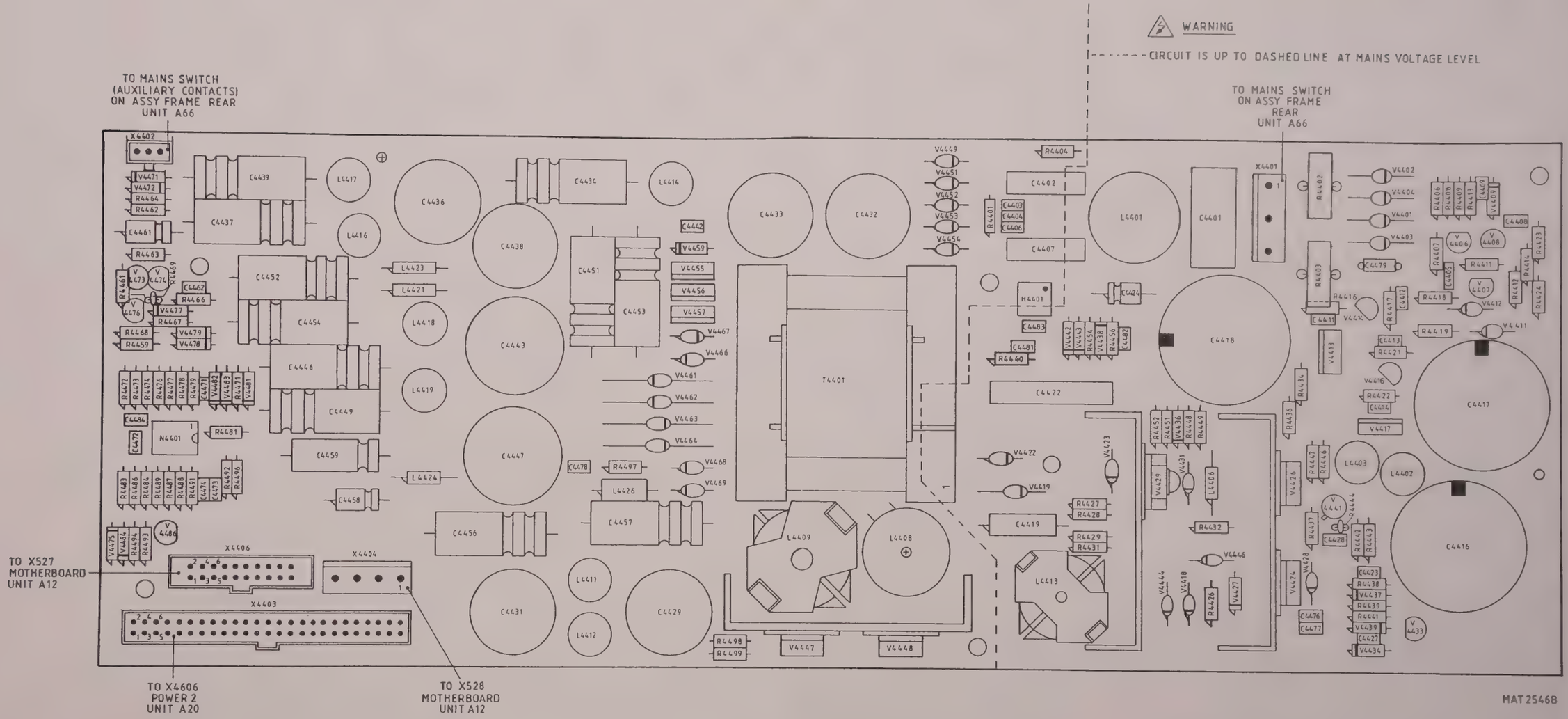
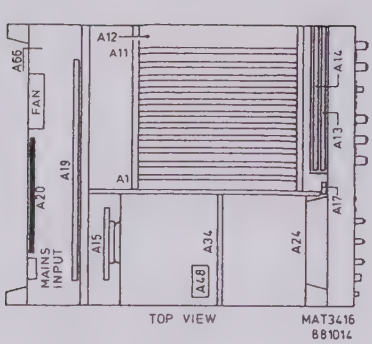


Figure 8.19.5 Unit A19 - POWER 1 - p.c.b. lay-out.



CONTENTS

8.20.1 General information..... 8.20-1
8.20.2 The reference voltage source..... 8.20-1
8.20.3 The line trigger circuit..... 8.20-2
8.20.4 The power down/up detection circuit..... 8.20-2
8.20.5 The EHT converter..... 8.20-3
8.20.6 The fan control circuit..... 8.20-4
8.20.7 Signal name list..... 8.20-4

8.20.1 General information

This unit consists of several circuits:

- a reference voltage source
- a line trigger circuit
- a power down/up detection circuit
- an EHT converter
- a fan-control circuit

WARNING: To avoid any electrical shock, it is strongly recommended to read section 10.1 first.

8.20.2 The reference voltage source

The voltage source consists of an operational amplifier N4601 with the associated components.
The zenerdiode V4601 (6,5 V) serves as the reference voltage source for the op-amp.
Via diode V4602 the node R4601, R4602, V4602 is kept at a stable voltage of 9,4 V to achieve a stable current through zenerdiode V4601.
The output voltage RV10 can be adjusted with R4607.

8.20.3 The line trigger circuit

The LNØ1 input from POWER UNIT 1 (A19) is a mains-voltage related signal. To ensure that the line trigger signal has a constant amplitude, this circuit provides automatic gain control. The LNØ1 input is fed to a feedback operational amplifier N4601 with a gain of 1000 (R4636/R4637). The output LN on pin 14 is fed to a comparator input N4601-10. The other input carries a reference voltage. This stage operates as a top detector. The output on pin 8 is a rectangular waveform (+14 V ... -14 V) with a very short duty cycle. The long negative stroke of this voltage charges C4618. The short positive stroke, which width is dependent on the amplitude of the sinewave on N4601-10, discharges C4618 a bit. The voltage on C4618 serves as a control voltage on the gate of the FET V4617. This FET conducts to regulate the amplitude of the signal on N4601-12.If, for instance, the mains voltage increases, LNØ1 also increases.
Then output N4601-14 increases. As a result the pulse width of the square wave signal on N4601-8 will get wider and C4618 will be charged less negative. FET V4617 will conduct more, which decreases the sine wave signal on N4601-12. This results in a direct correction of the output sinewave on N4601-14. The output provides the constant LN signal (sine wave 10 Vpp), which is routed to the external trigger unit (A31).

8.20.4 The power down/up detection circuit

The circuit consists of two comparators (N4602) with their associated components.
After power on, the signal C-ON goes high (> 20 V). After a time delay of 0.1 sec, determined by R4644 and C4622, the ILØ7--LT goes high. This signal, which is routed to the microprocessor unit A6, tells the microprocessor that the power is on and it can start.
In case of a converter failure, the C-ON-signal goes immediately low, which causes the signal ILØ7--LT to go low with a very short time delay, because C4622 is discharged fast via R4643 and N4602. The microprocessor will stop.

NOTE: C4622 can't be charged via R4643, because N4602 has open collector outputs.

8.20.5 The EHT converter

Transformer T4601 forms with the various capacitive loads an LC resonance circuit, with an own frequency of approx. 60 kHz.
The circuit is every period charged by a thyristor circuit, consisting of transistors V4608 and V4612 (switched parallel resonance converter).
The thyristor circuit is fired on the negative peak of T4601-9 (see figure 8.20.1). On the negative peak of T4601 - 9, the capacitor C4609 is charged via V4603, R4616, R4618, the b-e junction of V4608 and diode V4607. This fires the thyristor circuit.
Now V4611 charges the LC resonance circuit as soon as T4601 - 9 becomes positive, and V4608 discharges V4608.
When V4608 is discharged the thyristor circuit turns off, because the current from V4603 is below the treshold current of the thyristor circuit. Now C4608 is charged again via V4603.
A higher voltage at the base of V4603 results in a higher charge of C4608 and causes the thyristor circuit to be turned off later, so there will be supplied more energy to the resonance circuit, in this case the output transformer.
During the off-time of the thyristor circuit C4608 is discharged via R4616.

One output voltage (-2,1 kV) is fed back into op-amp N4601 to perform voltage stabilisation.
If the output voltage rises (i.e. -2,1 kV goes more negative) then N4601-3, N4601-1 and the emitter of V4603 go more negative. The on-time of the thyristor circuit will be shorter; the energy supplied to the transformer will decrease and therefore the output voltages will also decrease.

The output voltage F1/F2 (6,3 V) supplies the filament.
The output voltage of T4601-6 is rectified by V4613 and gives the -2,1 kV cathode voltage for the CRT and the feedback to N4601.
The output voltage of T4601-11 is converted to 14 kV in the HT-multiplier D4001 to supply the post acceleration anode of the CRT.
For security reasons the EHT ground is separated from the analogue ground on connector X4604 (1A, 1C, 2A, 2C) when the unit is removed.
The EHT is not available now (see also section 10.4).

The following figure gives some voltages in the circuit.

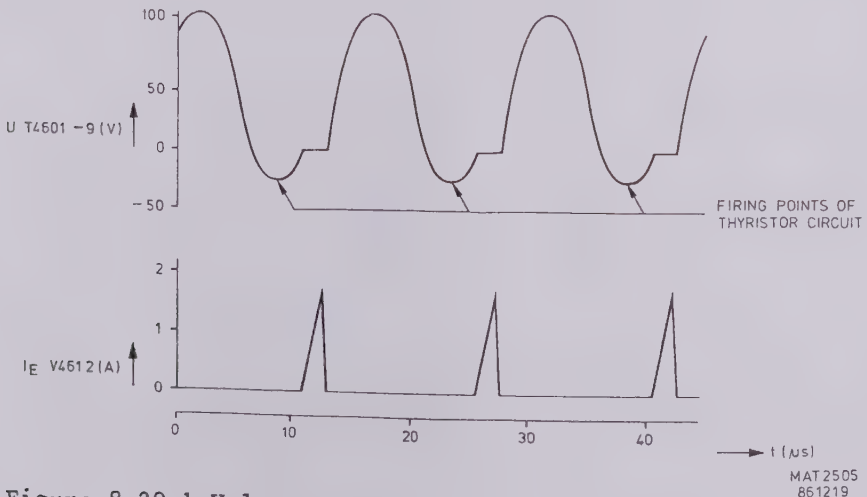


Figure 8.20.1 Voltage waveforms in the EHT converter.

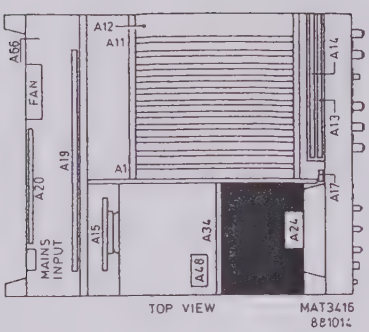
8.20.6 The fan control circuit

In this circuit, a triangle wave voltage of 70 kHz is generated by comparator N4602. Resistor R4652 loads the open collector output. This triangle voltage is on N4602-5 compared with a voltage on N4602-4, which is influenced by a NTC resistor R4656 on this board.
The output voltage on N4602-2 is a square-wave signal, whose duty cycle depends on the temperature of the NTC. This square-wave switches via V4621 and V4622 a converter, consisting of L4601, V4619 and C4624, which gives a maximum voltage of 28 V. The output voltage is supplied to the fan and fed back to N4602-4 via V4618 to achieve an overvoltage protection for the fan.
If V4622 doesn't switch for some reason, the fan runs on 14 V via L4601, V4619 and L4602, which is mostly sufficient to keep the oscilloscope running.

8.20.7 Signal name list

UNIT A20

Signal name	Description	Signal source	Signal destination(s)
BAVO	Battery voltage	A66	-
C-ON	Converter on	A19	-
EG	EHT ground	A20	A25
FS	Fan supply	A20	A66
f1	Filament 1	A20	A15-C.R.T.
f2	Filament 2	A20	A15-C.R.T.
ILØ7--LT	Interrupt level Ø7	A20	A19-A12-A6
LNØ1	Line Ø1	A19	-
LN	Line trigger	A20	A25-A31
RVG	Reference voltage ground	A20	A20,A19
RV1Ø	Reference voltage 1Ø V	A20	A20,A19
-2,1 kV	-2,1 kV C.R.T.	A20	A20,A15-C.R.T.
14 kV	14 kV EHT C.R.T.	A20	C.R.T.



CONTENTS

8.24.1 Circuit description..... 8.24-1
8.24.2 Signal name list..... 8.24-2

8.24.1 Circuit description

The DRIVER UNIT buffers the sample and transport clock signals from the ACE, IC D6001 on the CCD LOGIC unit A26. The output signals drive the P^2CCDs on the P^2CCD unit A33.

As channels A and B are identical, only channel A is described.

The TRANSPORT CLOCK DRIVER A accepts the signals TCODA-HE and TCEVA-HE from the ACE.
The circuit around transistors V9401...V9404 splits both signals in 2 equal signals.
One set of these signals (TCOD2AHX and TCEV2AHX) is led via a 1 ns coaxial delay line (length approx. 22 cm) to a driver stage. The driver stage consists of the circuitry around transistors V9451...V9454, V9456 and V9457. It buffers the delayed signals TCODDAHX and TCEVDAHX.
The output signals TCODDALX and TCEVDALX are applied to the P^2CCDs.
The other set of signals (TCOD1AHX and TCEV1AHX) is applied directly to a similar driver stage, which consists of the circuitry around transistors V9551...V9554, V9556 and V9557.
The output signals TCODA-LX and TCEVA-LX are applied to the P^2CCDs.

The SAMPLE CLOCK DRIVER A buffers the sample clock signals SCODA-LE and SCEVA-LE from the ACE. It consists of the circuitry around transistors V9501...V9504, V9506 and V9507, which is similar to the transport clock driver stages.
The average DC level of the even sample clock is influenced by the signal SCOCA from the P^2CCD unit A33, to achieve an equal average DC level of the odd and even sample clocks.
The output signals SCODA-HX and SCEVA-HX are applied to the P^2CCDs via 75 ohm coax cables.

Note: A number of transistors are mounted topside down, which is marked with a dot at their emitters in the p.c.b. layout (see figure 8.24.1).

8.24.2 Signal name list

UNIT A24

Signal name	Description	Signal source	Signal destination(s)
SCEVA-HX	Sample Clock Even A	A24	A33
SCEVB-HX	Sample Clock Even B	A24	A33
SCEVA-LE	Sample Clock Even A	A26	-
SCEVB-LE	Sample Clock Even B	A26	-
SCOCA	Sample Clock Output Control A	A33	-
SCOCB	Sample Clock Output Control B	A33	-
SCODA-HX	Sample Clock Odd A	A24	A33
SCODB-HX	Sample Clock Odd B	A24	A33
SCODA-LE	Sample Clock Odd A	A26	-
SCODB-LE	Sample Clock Odd B	A26	-
TCEVA-HE	Transport Clock Even A	A26	-
TCEVB-HE	Transport Clock Even B	A26	-
TCEVA-LX	Transport Clock Even A	A24	A33
TCEVB-LX	Transport Clock Even B	A24	A33
TCEV1AHX	Transport Clock Even 1 A	A24	A24
TCEV2AHX	Transport Clock Even 2 A	A24	A24
TCEV1BHX	Transport Clock Even 1 B	A24	A24
TCEV2BHX	Transport Clock Even 2 B	A24	A24
TCEVDAHX	Transport Clock Even Delayed A	A24	A24
TCEVDALX	Transport Clock Even Delayed A	A24	A33
TCEVDBHX	Transport Clock Even Delayed B	A24	A24
TCEVDBLX	Transport Clock Even Delayed B	A24	A33
TCODA-HE	Transport Clock Odd A	A26	-
TCODB-HE	Transport Clock Odd B	A26	-
TCODA-LX	Transport Clock Odd A	A24	A33
TCODB-LX	Transport Clock Odd B	A24	A33
TCOD1AHX	Transport Clock Odd 1 A	A24	A24
TCOD2AHX	Transport Clock Odd 2 A	A24	A24
TCOD1BHX	Transport Clock Odd 1 B	A24	A24
TCOD2BHX	Transport Clock Odd 2 B	A24	A24
TCODDAHX	Transport Clock Odd Delayed A	A24	A24
TCODDALX	Transport Clock Odd Delayed A	A24	A33
TCODDBHX	Transport Clock Odd Delayed B	A24	A24
TCODDBLX	Transport Clock Odd Delayed B	A24	A33

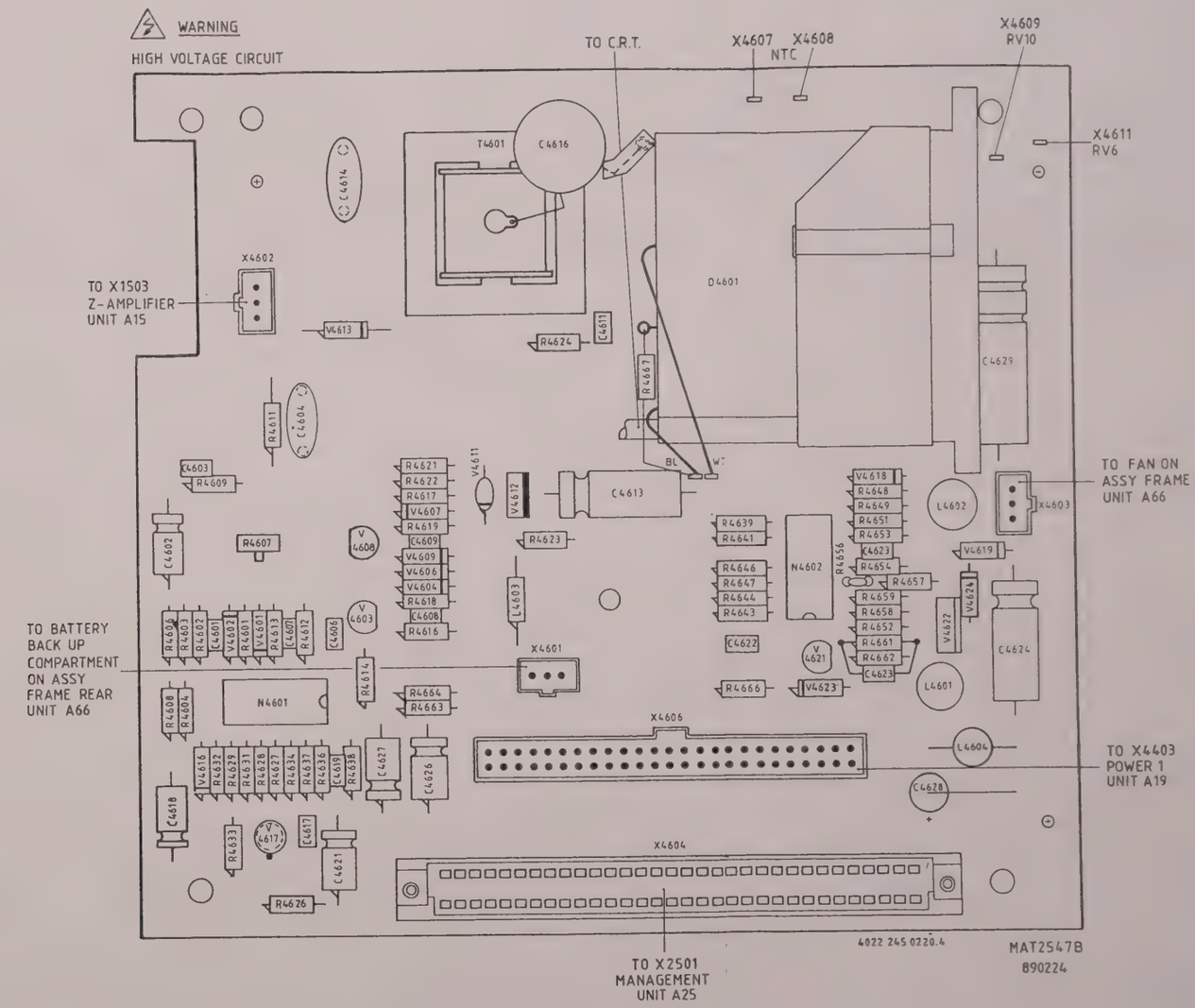


Figure 8.20.2 Unit A20 - POWER 2 - p.c.b. lay-out.

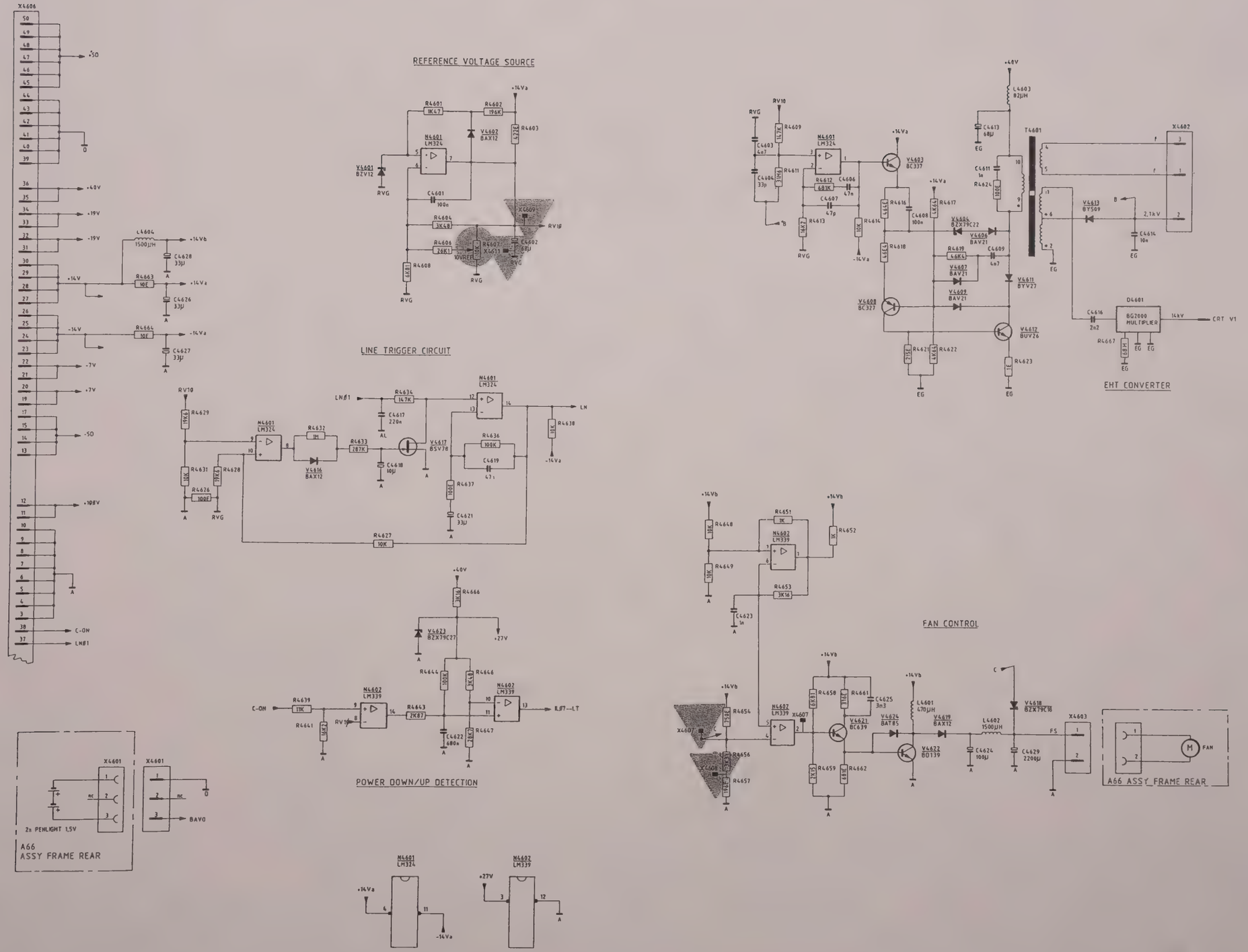
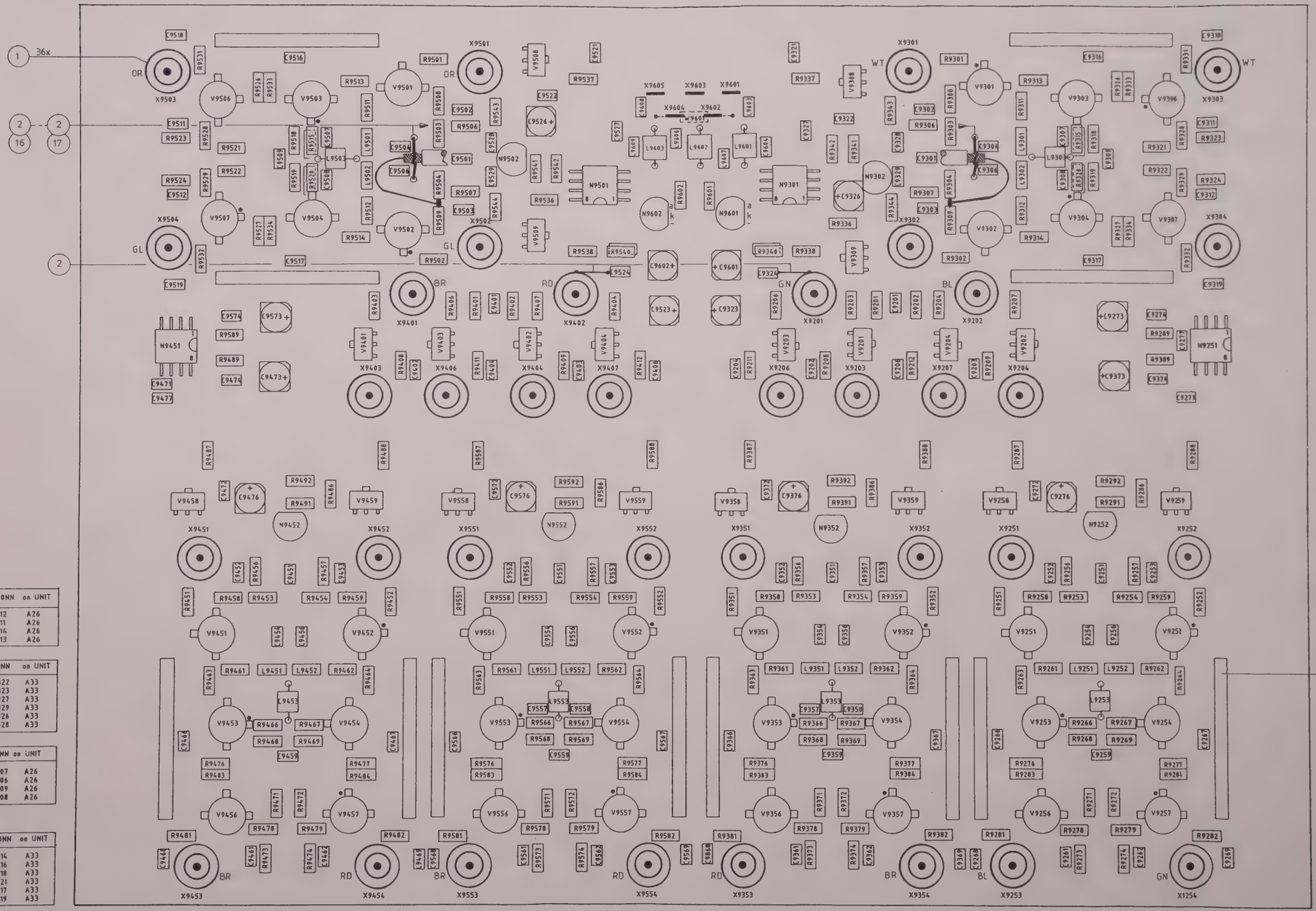


Figure 8.20.3 Unit A20 - POWER 2 - circuit diagram.



CONN	to CONN	on UNIT
X9201	X2612	A26
X9202	X2611	A26
X9301	X2614	A26
X9302	X2613	A26

CONN	to CONN	on UNIT
X9303	X3322	A33
X9304	X3323	A33
X9253	X3327	A33
X9254	X3329	A33
X9353	X3326	A33
X9354	X3328	A33

CONN	to CONN	on UNIT
X9401	X2607	A26
X9402	X2606	A26
X9501	X2609	A26
X9502	X2608	A26

CONN	to CONN	on UNIT
X9503	X3314	A33
X9504	X3316	A33
X9453	X3318	A33
X9454	X3321	A33
X9553	X3317	A33
X9554	X3319	A33

ON BOARD CONNECTIONS				
X9203	DELAYLINE	X9251	X9206 ----	X9351
X9204	DELAYLINE	X9252	X9207 ----	X9352
X9403	DELAYLINE	X9451	X9406 ----	X9551
X9404	DELAYLINE	X9452	X9407 ----	X9552

CABLE to CONN on UNIT
GREY ---- X7653 A52
VIOLET -- X7657 A52

Figure 8.24.1 Unit A24 - DRIVER UNIT - p.c.b. lay-out.

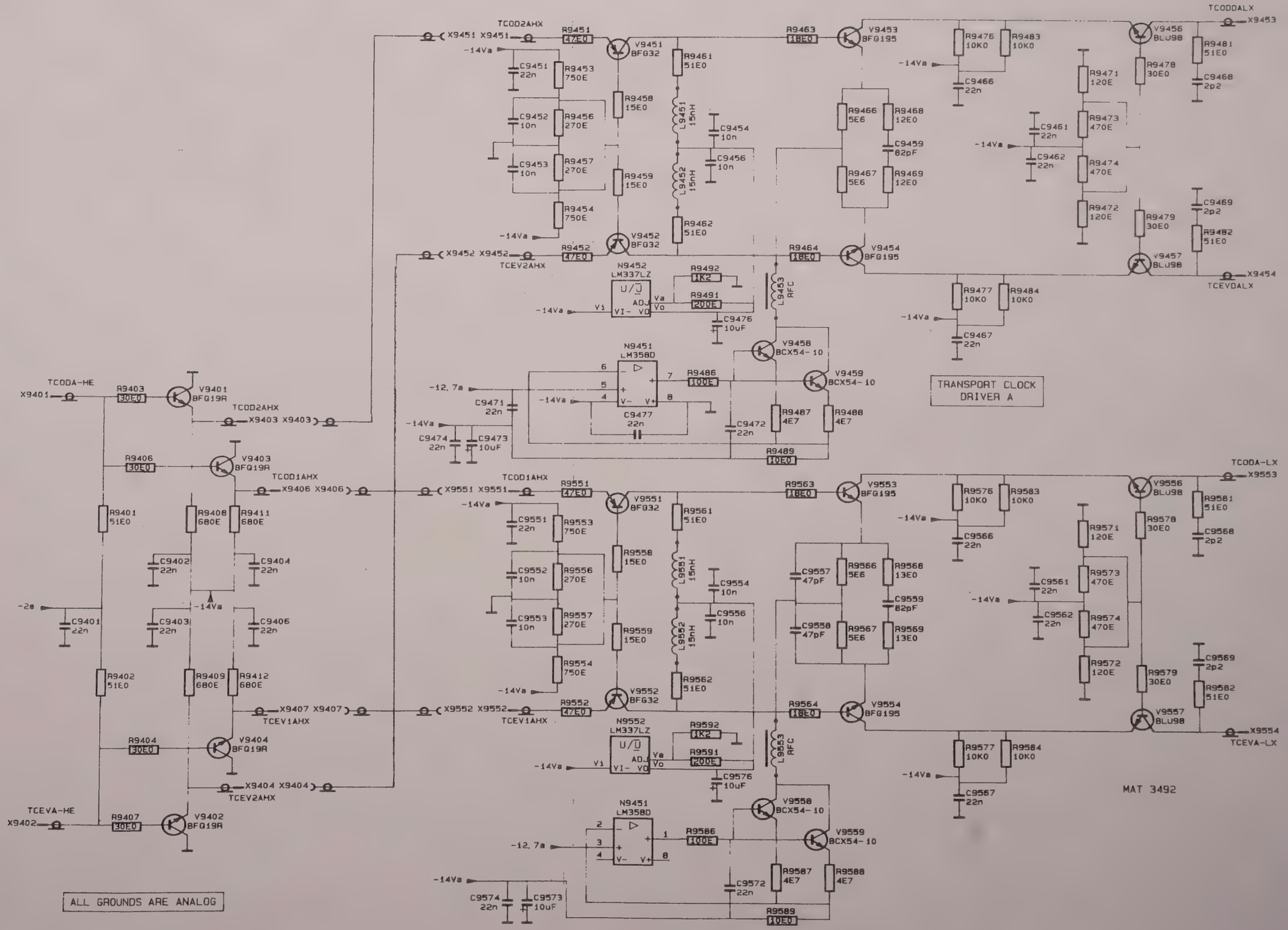


Figure 8.24.2 Unit A24 - DRIVER UNIT - circuit diagram.

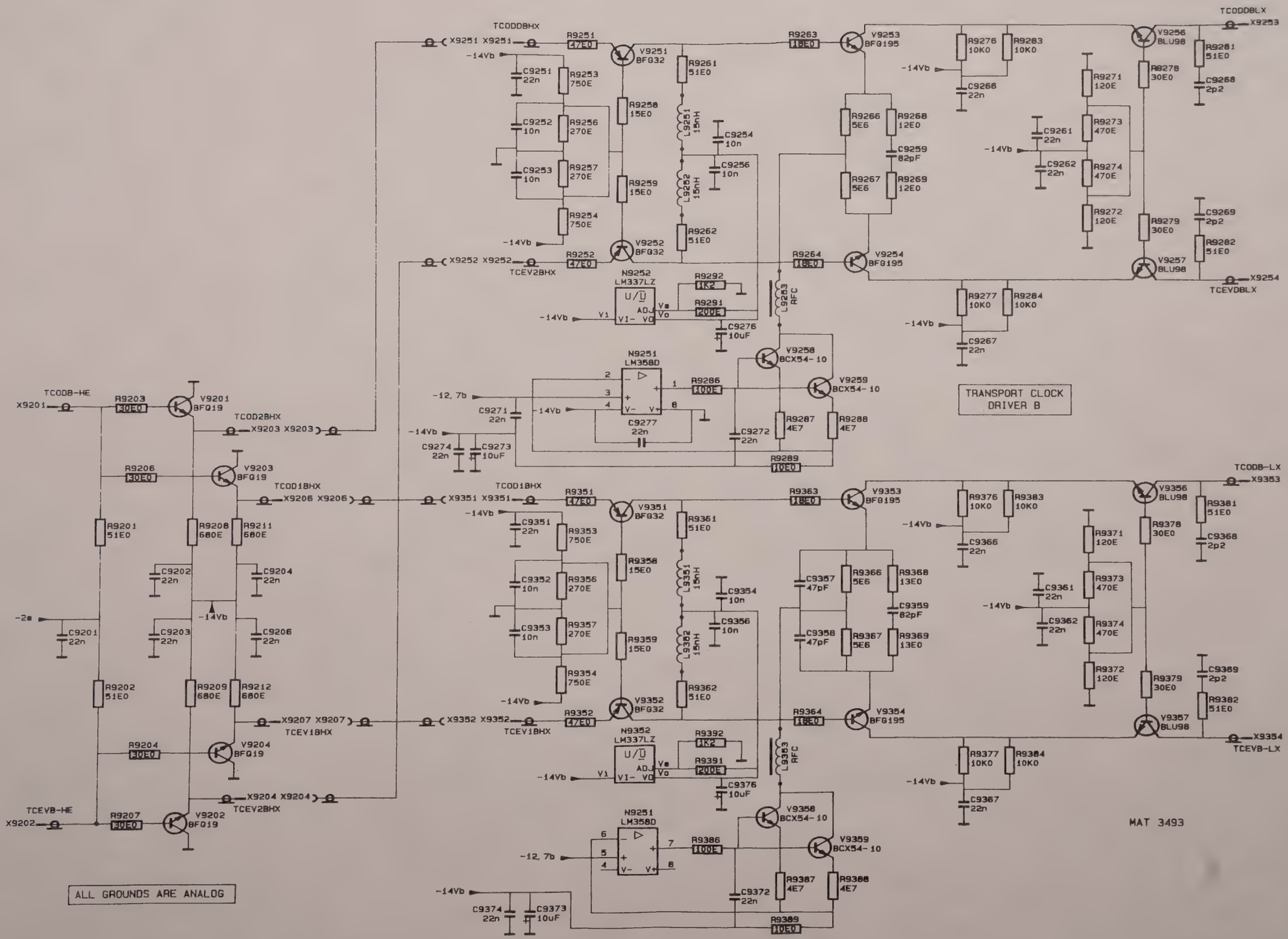


Figure 8.24.3 Unit A24 - DRIVER UNIT - circuit diagram.

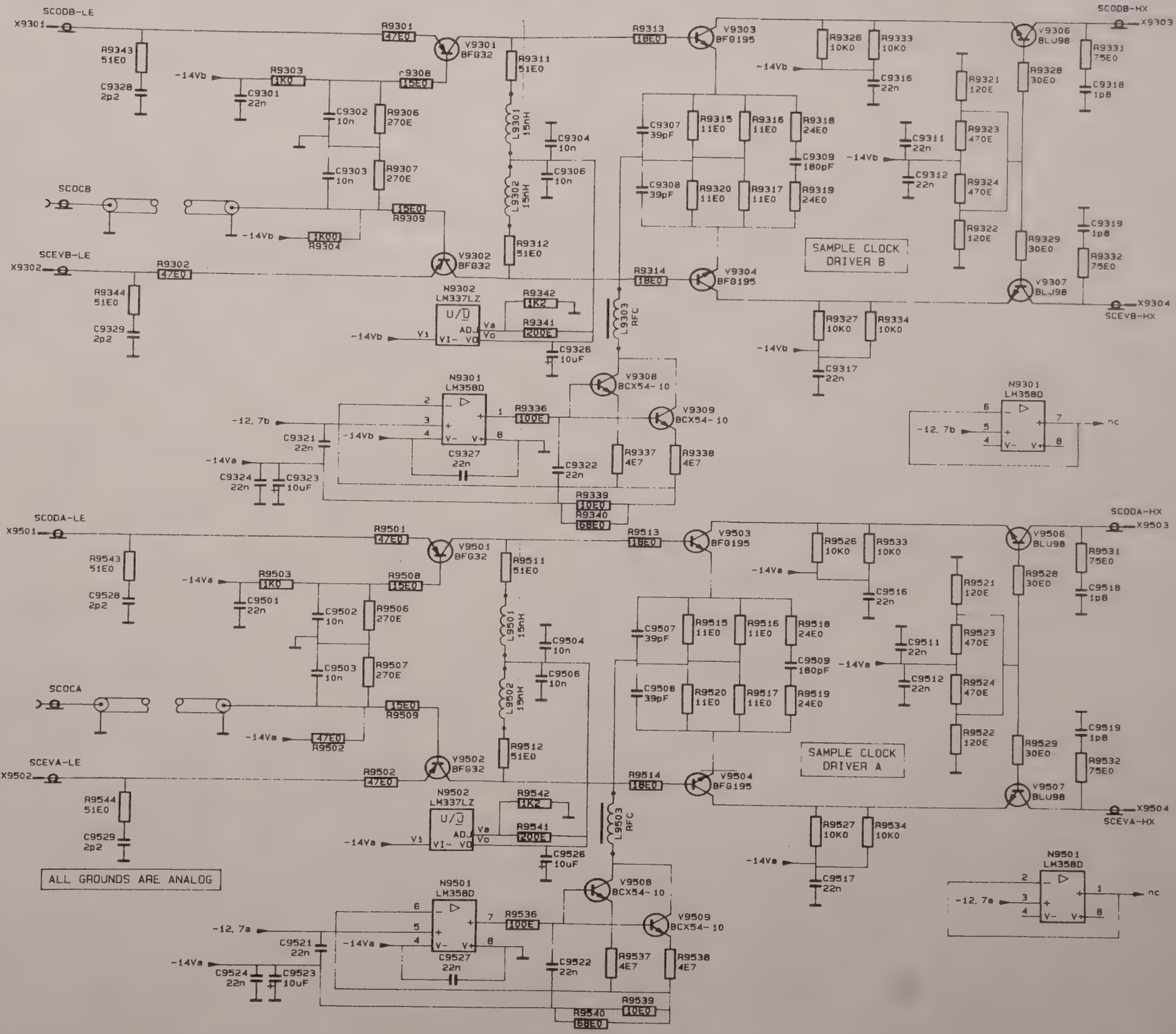


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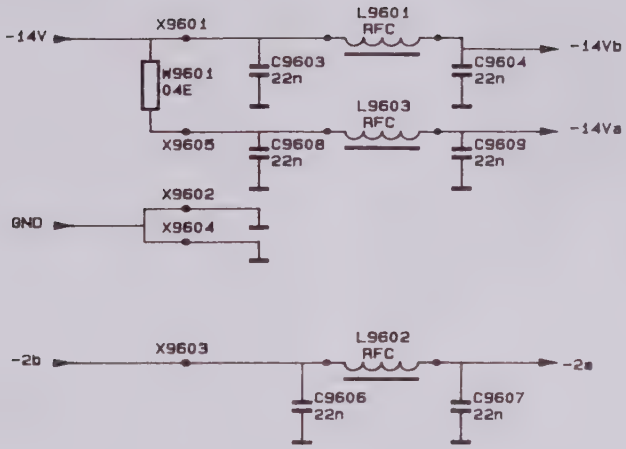
Figure 8.24.4 Unit A24 - DRIVER UNIT - circuit diagram.



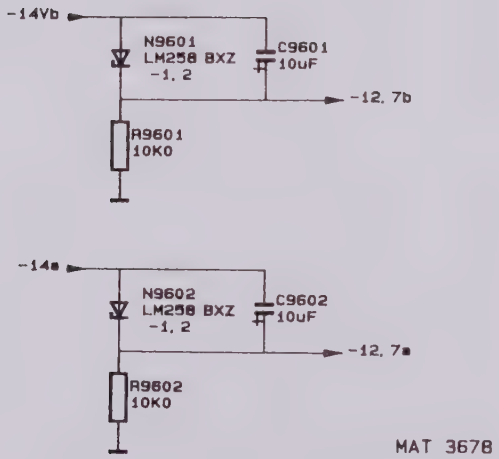
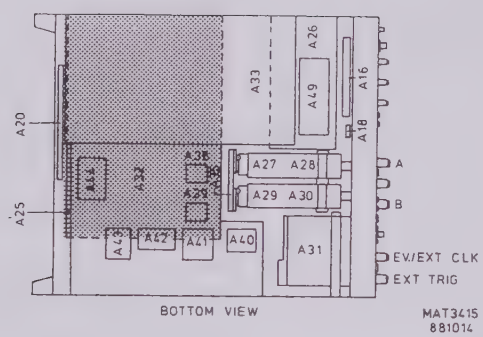


Figure 8.24.5 Unit A24 - DRIVER UNIT - circuit diagram.

UNIT A25 - MANAGEMENT UNIT



CONTENTS

8.25.1	General information	8.25-2
8.25.2	Microprocessor control - and data buffers and address decoder	8.25-2
8.25.3	Attenuator control latches	8.25-4
8.25.4	Vertical signal - and signal switch latch	8.25-5
8.25.5	Probe information ADC and 50 Ohm protection buffer	8.25-5
8.25.6	Trigger latches	8.25-6
8.25.7	Delta-t serial-parallel converter and the delta-t control latch	8.25-7
8.25.8	Shift and variable control circuits	8.25-8
8.25.9	Auto offset level DAC	8.25-10
8.25.10	Offset and trigger level DACs	8.25-11
8.25.11	ACL buffer, P^2CCD output control circuit and P^2CCD buffer	8.25-12
8.25.12	Signal name list	8.25-13

8.25.1 General information

On the management unit the following main functions are present:

1. - Decoupling of power supply voltages which are routed via this unit to units A32, A33 and A27...A30.
   - Interconnection of different power supply voltages which are routed to unit A34, A31 and A26.

2. - Interconnection for several control signal lines between different units e.g. via connectors X2516-X2502-X2503-X2513-X2514
   - Signal buffering of control signals e.g. via D434, D404 etc.

3. Interface between microprocessor and the following units:

Vertical signal unit	A32
P^{2}CCD unit	A33
Attenuators A and B	A27...A30
Clock unit	A34
External trigger unit	A31
CCD logic	A26

8.25.2 Microprocessor control- and data buffers and address decoder (D401, D402, D403, D406, D407)

The bi-directional 16-bits data information is fed from the microprocessor via data buffers D401 and D402 to unit A25 and A26 (via X2504).
The data buffers D401 and D402 are enabled by the control signal ENBS derived from D414-D416-6 which on its turn are controlled by the control signals IOSLØ6LT and IOSLØ7LT.
The control signal RDDABS (read data buffers) which is derived from the signals UPRD-1LT and IOSLØ7LT changes the direction of data transport.
If this RDDABS signal is low the contents of the data buffers is read by the microprocessor and if it is high, the buffers will receive data from the microprocessor.

The address signals ABØ1...ABØ4 and the control signals UPRD--LT and I/O select Ø6 and Ø7 are controlling the functions on this unit via the address-control buffer D403.
The signal IOSLDL enables the buffer D403 and freezes ABØ1...ABØ4, I/O select Ø6 and Ø7 and UPRD--LT after a fixed I/O select delay time which is determined by D408-13-12-11-10.

This delay time of 50 ns is necessary to prevent interference on the address and control signals coming from the data bus when the data bus switches.

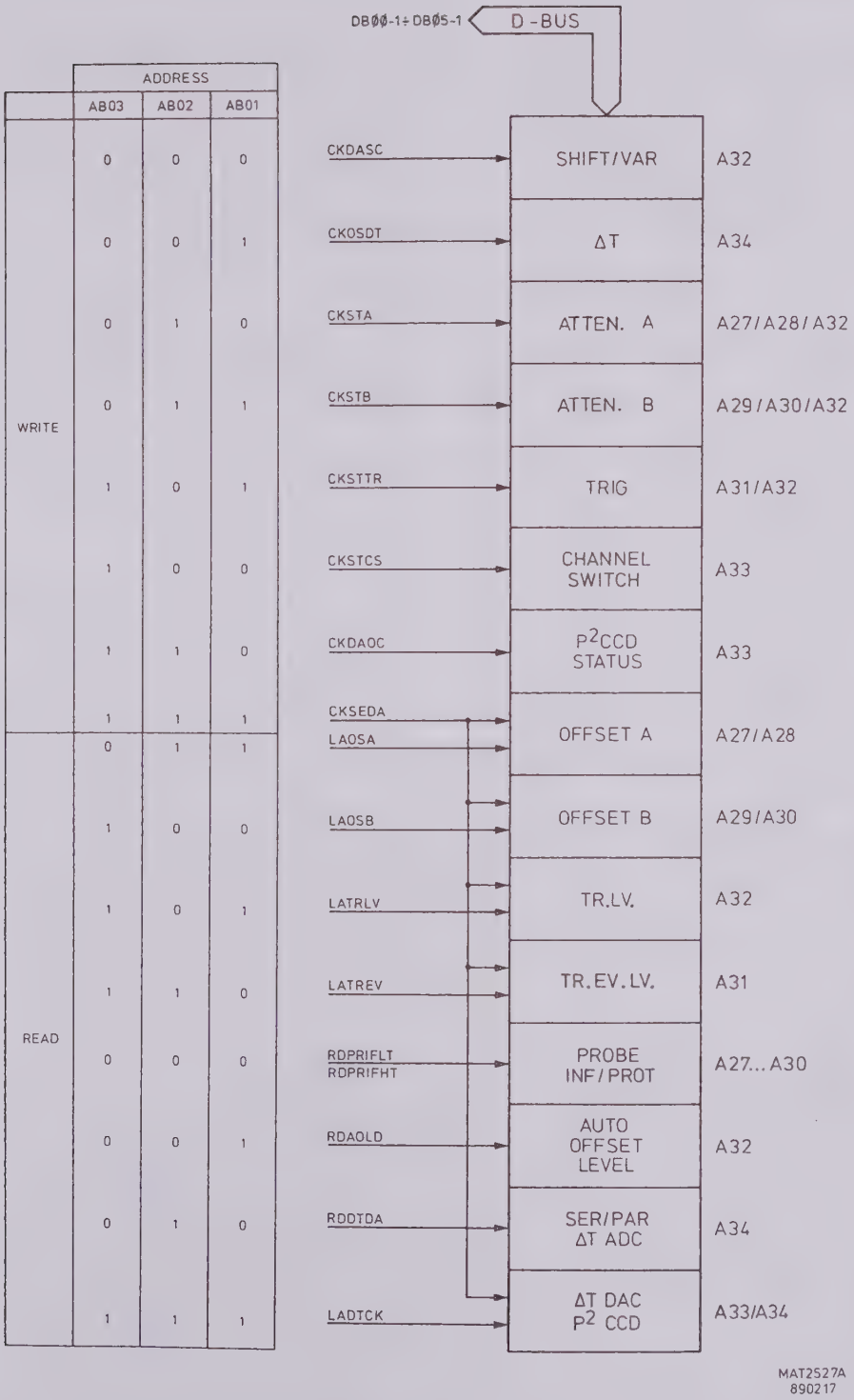


Figure 8.25.1 Address decoder control signals.

The control signals LAOSA, LAOSB, LATRLV, LATREV and LADTCK select the 14-bits serial DACs respectively N403, N404, N407, N406 and X2506-7.

8.25.3 Attenuator control latches (D409, D411, D412, D413)

In the truth tables below, the several control signal levels are indicated for the vertical attenuation control on the attenuator units and on the vertical signal unit.
The latches for channel A (D409 and D411) are selected by CKSTA and for channel B by CKSTB (see below). The drivers D414 and D416 are level adapters to adapt the TTL level to a 0-10 V level.
The control signals OSA+/- and OSB+/- are routed to D423 pins 13 and 5 to control the polarity of the offset of channels A and B.

	VERTICAL SIGNAL UNIT A32					ATTENUATOR A28		
ATTENUATOR SETTING	PA/1A	PA/2A	PA/4A	PA2.5 XAHT	PA2.5 XALT	AT100A	AT10A	AT1A
5 mV/div	1	0	0	0	1	0	0	1
10 mV/div	0	1	0	0	1	0	0	1
20 mV/div	0	0	1	0	1	0	0	1
50 mV/div	1	0	0	0	1	0	1	0
100 mV/div	0	1	0	0	1	0	1	0
200 mV/div	0	0	1	0	1	0	1	0
0,5 V/div	1	0	0	0	1	1	0	0
1 V/div	0	1	0	0	1	1	0	0
2 V/div	0	0	1	0	1	1	0	0
5 V/div	0	0	1	1	0	1	0	0

INPUT COUPLING A	AC DC A
AC	0
DC	1

ZERO	ZEA
CH. A	
ON	1
OFF	0

50 Ohm PROTECT CH. A	TM50A
ON	1
OFF	0

TRIG SOURCE CH. A	TRSOA
ON	1
OFF	0

MODE	NOA	IVA
NORMAL	1	0
INVERT	0	1

For channel B the logic levels are exactly the same as for channel A only the addresses are different:

CKSTB and the latches for channel B are D412 and D413.

8.25.4 Vertical signal switch latch

This latch is controlled by the clock signal CKSTCS (pin 11).
This latch (D417) is used for control signals (PDSWØ...PDSW2) for the signal switch (unit A33) and for control of the bandwidth limiter and ADD circuit on the vertical signal unit A32.

VERTICAL SIGNAL CONTROL

BWL	BWL---LT	BWL---HT
ON	0	1
OFF	1	0

ADD	A+B---LT	A+B---HT
ON	0	1
OFF	1	0

SIGNAL SWITCH CONTROL

TIME BASE	MODE	PDSW2	PDSW1	PDSW0
NORMAL	≥0,5 ms	0	1	0
	≤0,2 ms	0	0	0
MIN/MAX	≥2 ms	1	1	1
	≤1 ms	0	1	1

8

8.25.5 Probe information ADC and 50 Ohm protection buffer (D437 and D419)

The selection of this detection IC D437 is done by RDPRIFHT coming from D407.
The detection of the attenuation factor of the connected probe is done via the current signal PRIFA-XA for ch. A and with PRIFB-XA for ch. B.
These signals from the attenuator units A28 (A) and A30 (B) are applied to pins 3 and 16 of D437.
This results in the following output signals from D437:

PROBE INDICATION

PROBE	CHANNEL A DB 00-1	DB 01-1	DB 02-1	DB 03-1	CHANNEL B DB 04-1	DB 05-1	DB 06-1	DB 07-1
1:1 (1 MOhm)	1	1	1	1	1	1	1	1
1:100 (1 MOhm)	1	1	0	1	1	1	0	1
1:10 (1 MOhm)	1	0	0	0	1	0	0	0
1:100 (50 Ohm)	1	1	0	0	1	1	0	0
1:10 (50 Ohm)	1	0	0	1	1	0	0	1
CURRENT PROBE								
HV ISOLATION PROBE	1	1	1	0	1	1	1	0

The selection of the 50 Ohm protection buffer is done by the signal RDPRIFLT.
This buffer latches 2 signals from the vertical attenuator units A28 and A30 (PT50A-LT and PT50B-LT), the aliasing status signal ALID and trigger status signal TRID.

These input signals are generating the following output data:

50 OHM PROBE PROTECTION

50 OHM PROBE PROTECTION CH A	PT50A--LT DB08-1
50 Ohm REED RELAY OFF	0
50 Ohm REED RELAY NOT OFF	1
50 OHM PROBE PROTECTION CH B	PT50B--LT DB09-1
50 Ohm REED RELAY OFF	0
50 Ohm REED RELAY NOT OFF	1

TRIGGER INDICATION

NOT TRIG'D	DB11-1 TRID
TRIGGERED	1
NOT TRIGGERED	0
ALIASED	DB10-1 ALID
ALIASED DETECT	1
NO ALIASING (NORMAL)	0

8.25.6 Trigger latches (D421 and D422)

The trigger and trigger events modes are controlled by signals coming from the trigger latches D421 and D422.
These trigger latches are addressed by the control signal CKSTTR applied to the inputs D421-11 and D422-11.
The output control signals TRDUMO and TREV+/- are routed to respectively the trigger level DAC and the trigger event level DAC.
The trigger latches generate the following output control signals:

TRIGGER INPUT AND TRIGGER EVENTS INPUT

TRIGGER COUPLING	ACTRCO	DCTRCO	HFTRCO
DC	0	1	0
DC/LF	0	1	1
AC	1	0	0
AC/LF	1	0	1
AC/HF	0	0	0

TRIGGER SOURCE	ETTR	ETTR/5	ETTR/50
EXT	0	0	1
EXT:10	0	1	0

EXTERNAL TRIGGER COUPLING	TRACDC	
AC	0	
DC	1	
TRIG.MODE	TRDUMO	TRTVMO
NORMAL	1	1
DUAL	0	1
TV	1	0
AUTO LEVEL	AULV	
ON	0	
OFF	1	
TRIG SLOPE	TRSP	
+	1	
-	0	
TRIG EVENT SLOPE	TREVSP	
+	1	
-	0	
LINE TRIG	LNTR	
ON	1	
OFF	0	
EVENT/5	TREV/1	
ON	0	
OFF	NOT USED	
EVENT/50	TREV/10	
ON	NOT USED	
OFF	1	

8

8.25.7 Delta-t serial parallel converter (D424, D426, D428) and the delta-t control latch (D427)

In the serial parallel converter consisting of two shift registers D424 and D426, the serial data DTADDA coming from the delta-t ADC on the clock unit A34 is converted into parallel data signals DB00-1...DB09-1 which are applied to the databus.
The clock signal which is controlling this conversion is DTADCK, coming from clock unit A34.
If all data are latched, the status signal, DTADST applied to D428-12, becomes active.
This status signal makes IL06--LT (D428-2) active (low).

Now the microprocessor will read the data by enabling the delta-t serial parallel converter via the RDDTTA signal. This signal also resets IL06--LT.

The signals DB15-1, CKSEDA and LADTCK are applied to the clock unit A34, where they are used for the delta-t ADC.

The delta-t control latch D427 is controlled by the clocksignal CKOSDT. The output signals behave as follows:

EN200MLT is 0 in time-base settings:
0,2 ms/div...0,5us/div
50 ns/div... 5ns/div
EN200MLT is 1 in all other time-base settings.

EN250MLT is 0 in time-base settings 200 ns/div and 100 ns/div.
EN250MLT is 1 in all other time-base settings.

CDOGC1 is 0 in the following settings:
360 s/div...200 ns/div, single channel, min/max off
0,2 ms/div...200 ns/div, dual channel, min/max off
CDOGC1 is 1 in all other settings.

CDSGC1 is 0 in the following settings:
360 s/div...5 ns/div, single channel, min/max off
0,2 ms/div...5 ns/div, dual channel, min/max off
CDSGC1 is 1 in all other settings.

CDOGC2 is 1 in time-base settings 200 ns/div and 100 ns/div.
CDOGC2 is 0 in all other time-base settings.

CDSGC2 is 0 in time-base setting 100 ns/div.
CDSGC2 is 1 in all other time-base settings.

8.25.8 Shift and variable control circuits

The shift and var-control circuits consist of the following parts:

* The shift-var latches
* The shift-var DAC
* The shift-var timer
* The shift-var decoder
* The sample and hold circuits.

* The shift-var latches (D429 and D431)

The latches D429 and D431 are controlled by the clock signal CKDASC from D406.
The output signals of the latches SCDBØØ...SCDB11 are the data for the shift-var DAC N401 (12 bits).

* The shift-var DAC (N401)

The 5V reference voltage for this DAC, coming from opamp N417-6 (adjustable with R462), is applied to N401-17. The setting time of the DAC circuit and N408, N409 is 1 ms.

The output voltage levels of the DAC circuits are as follows:

	INPUT DATA											OUTPUT
SCDBØØ	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7	Ø8	Ø9	10	11	
0	0	1	1	1	1	1	1	1	1	1	1	+5 V
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
0	0	1	0	0	0	0	0	0	0	0	1	+5 mV
0	0	0	0	0	0	0	0	0	0	0	1	0 V
0	0	1	1	1	1	1	1	1	1	1	0	-5 mV
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
0	0	0	0	0	0	0	0	0	0	0	0	-5 V

The dc output level of the DAC circuit is applied to the inputs of four sample and hold circuits N412...N416.

* The shift-var timer (D432)

This timer is necessary to determine the settling time for the DAC and the acquisition time for the sample and hold circuits.

These two delay times are determined by two separate timers:

1. D432-2-4 delay time ≃1 ms (settling time DAC-circuit)
2. D432-10-2 delay time ≃100 us (acquisition time S&H)

The first timer D432-2-4 is started by the clock signal CKDASC.
The delay time is determined by R458 and C492 (≃1 ms).
This time is necessary for the settling time of the DAC circuit. The second timer D432-10-12 is started ≃1 ms after the first one. The delay in this second timer is determined by R459 and C493 (≃100 us).
This time is necessary for the acquisition time of the sample and hold circuits.
The ≃1 ms delayed clock signal CKDASC is applied to the shift-var decoder (D433).

* The shift-var decoder (D433)

The decoder selects one of the four sample and hold circuits. The input signals SCDB12-1 and SCDB13-1 are decoded on receipt of a pulse coming from the second timer D432 into one of the four control signals:

Control signal	To sample and hold	SCDB12-1	SCDB13-1
TSSHA	N412	0	0
TSVGA	N413	1	0
TSSHB	N414	0	1
TSVGB	N416	1	1

* The sample and hold circuits (N412...N416)

The function of the sample and hold circuit is to take a sample from the DAC-output and to hold the sample (dc voltage) up to the moment that it will be refreshed by its control signal coming from the decoder D433.

TSSHA: Take sample for shift channel A
TSSHB: Take sample for shift channel B
TSVGA: Take sample for variable gain channel A
TSVGB: Take sample for variable gain channel B

If one of these control signals is active the stored dc value of the selected sample and hold circuit is given on its output.
The refresh rate of each sample and hold circuits is 20 ms (4x5 ms) see figure 8.25.2.

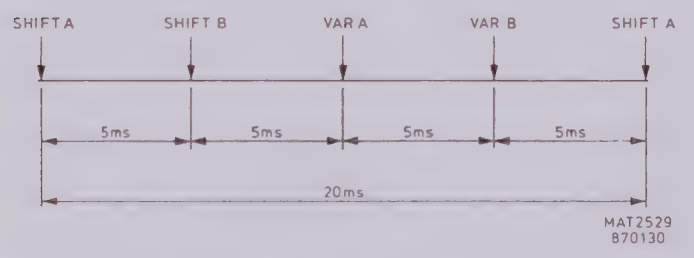


Figure 8.25.2 Refresh rate of each sample and hold (20 ms) and wait time (5 ms) before the next S&H is accessed.

8.25.9 Auto offset level ADC (N402)

The function of this ADC is to convert the average DC level of the input signal into digital data information to perform the auto offset function. This ADC (N402) is selected with the signal RDAOLD coming from D407.
The analog input signal, coming from vertical signal unit A32, is AOLD.
The reference voltage for the ADC is adjustable with R462 and stabilized by N417 and N411.
The signal conversion in the ADC is started by a low pulse RDAOLD (active low). The conversion time of the ADC is 20 us.
Next RDAOLD goes low again and the data is read by the microprocessor.

The following analog input levels result in:

INPUT ADC	OUTPUT ADC							
	DBØØ-1	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7
+5 V	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
+39 mV	1	0	0	0	0	0	0	1
0 V	1	0	0	0	0	0	0	0
-39 mV	0	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
-5 V	0	0	0	0	0	0	0	0

8.25.10 Offset and trigger level DACs (N403...N407)

The function of this part of the unit is to convert the digital offset and trigger level information into analog signals.

* Offset DAC A (N403)

This 14 bits serial DAC is controlled by the clock signal CKSEDA and the control signal LAOSA coming from respectively D406 and D407. The input serial-data DB15-1 is applied to pin 1.

The polarity of the OSA signal is determined by the OSA +/- signal, which determines if opamp N423 inverts or not.

From this 14 bits DAC, 10 bits are used.
The four LSB´s are always zero.

The offset is controlled as follows:

BINARY CODE															ANALOG OUTPUT
OSA+/-	MSB													LSB	
0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	+5 V
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 V
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	-5 V

The analog output level AOSA is via a coaxial wire applied to the offset adaption unit A50.

* Offset DAC B (N404).

This circuit is almost identical to the offset DAC A circuits, as described before.

The DAC is controlled by the CKSEDA and LAOSB signals.

The polarity of the output signal is determined by the OSB+/- signal.

The analog output level AOSB is via a coaxial wire applied to the offset adaption unit A50.

* Trigger event level DAC (N406)

This circuit is almost identical to the Offset DAC A circuit, as described before.

The DAC is controlled by the CKSEDA and LATREV signals.

The polarity of the output signal is determined by the TREV+/- signal.

The analog output level TREVLV is applied to the external trigger input A31.

* Trigger level DAC (N407)

This circuit is almost identical to the offset channel A circuit, as described before.

The DAC is controlled by the CKSEDA and LATRLV signals.

The analog output voltage is split up into two signal pathes:

TRDULV (level in dual trigger mode) and TRLV (trigger level in normal mode).
The polarity cannot be changed (output range 0...+5 V).
The analog signal TRLV can be switched off via D423-11-10, which is determined by TRDUMO.

TRDUMO

0 TRLV is switched off
1 TRLV is switched on

The analog output signals TRDULV and TRLV are applied to the vertical signal unit A32.

8.25.11 ACL buffer (D434), P^2CCD output control (D436) and P^2CCD buffer (D404)

* ACL buffer (D434)

The input signals of this buffer are coming from the P^2CCD unit A33 (via X2516) and the CCD logic A26 (via X2503).
The buffered output control signals are applied to the MRAM unit A5 via X2502.

* P^2CCD output control (D436)

This latch is selected by the clock signal CKDAOC.
The output signals are control signals for the P^2CCD unit A33.

Details of the control signals on the output of this latch are given in section 8.33.

* P^2CCD buffer (D404)

The two input clock signals CKCDOC and CK16ØØ are coming from the MRAM unit A5.
The buffered output clock signals are fed to the P^2CCD unit A33.
Details of these clock signals can be found in the sections 8.5 and 8.33.

8.25.12 Signal name list

UNIT A25

Signal name	Description	Signal source	Signal destination(s)
A-	Channel A	A25	A33
ABØ1...Ø4	Address bus Ø1...Ø4	A6+option	-
ABØ1-1...Ø4-1	Address bus Ø1-1...Ø4-1	A25	A25,A26
ACDCA	AC-DC input coupling A	A25	A50-A35-A28
ACDCB	AC-DC input coupling B	A25	A35-A30
ACTRCO	AC trigger coupling	A25	A32
ALID	Aliasing indication	A49	-
AOLD	Auto offset level detection	A32	-
AOSA	Analog offset A	A25	A50
AOSB	Analog offset B	A25	A50
AT1A	Attenuation x1 A	A25	A50-A35-A28
AT1B	Attenuation x1 B	A25	A35-A30
AT1ØA	Attenuation x1Ø A	A25	A50-A35-A28
AT1ØB	Attenuation x1Ø B	A25	A35-A30
AT1ØØA	Attenuation x1ØØ A	A25	A50-A35-A28
AT1ØØB	Attenuation x1ØØ B	A25	A35-A30
AULV	Auto Level	A25	A32
A+B---HT	Add mode	A25	A32
A+B---LT	Add mode	A25	A32
A+B—1HT	Add mode 1	A25	A33
BWL---HT	Bandwidth limiter	A25	A32
BWL---LT	Bandwidth limiter	A25	A32
CD	P^2CCD	A25	A33
CDOCØØ	P^2CCD output control ØØ	A25	A33
CDOCØ1	P^2CCD output control Ø1	A25	A33
CDOCØ2	P^2CCD output control Ø2	A25	A33
CDOCØ3	P^2CCD output control Ø3	A25	A33
CDOGC1	P^2CCD output gain control 1	A25	A33
CDOGC2	P^2CCD output gain control 2	A25	A33
CDRD	P^2CCD read	A25	A12-A5
CDRD-2	P^2CCD read-2	A26	-
CDSGC1	P^2CCD sample gate control 1	A25	A33
CDSGC2	P^2CCD sample gate control 2	A25	A26, A33
CHPTØ1	Channel pointer Ø1	A33	-
CKCDOC	Clock P^2CCD output control	A5	-
CKCDOC-1	Clock P^2CCD output control-1	A25	A33
CKDAOC	Clock data output control	A25	A25
CKDASC	Clock data sample control	A25	A25

8

Signal name	Description	Signal source	Signal destination(s)
CKOSDT	Clock offset delta-t	A25	A25
CKSEDA	Clock serial data	A25	A34
CKSTA	Clock setting A	A25	A25
CKSTB	Clock setting B	A25	A25
CKSTCS	Clock setting channel switch	A25	A25
CKSTTR	Clock setting triggering	A25	A25
CKØ1ØØ	Clock Ø1ØØ	A33	-
CK16ØØ	Clock 16ØØ	A5	-
CK16ØØ-1	Clock 16ØØ-1	A25	A33
DBØØ...15	Data bus ØØ...15	A6+option	-
DBØØ-1...14-1	Data bus ØØ-1...14-1	A25	A25,A26
DB15-1	Data bus 15-1	A25	A25,A26,A34
DCTRCO	DC trigger coupling	A25	A32
DTADCK	Delta-t ADC clock	A34	-
DTADCK-1	Delta-t ADC clock-1	A25	A25
DTADDA	Delta-t ADC Data	A34	-
DTADST	Delta-t ADC status	A34	-
EG	EHT ground	A20	-
EN2ØØMLT	Enable 2ØØ MHz oscillator	A25	A34
EN25ØMLT	Enable 25Ø MHz oscillator	A25	A34,A34-A11
ENBS	Enable buffers	A25	A25
ETCK	External clock	A25	A12-A5
ETCK-2	External clock-2	A26	-
ETTR	External triggering	A25	A32
ETTR/5	External triggering /5	A25	A31
ETTR/5Ø	External triggering /5Ø	A25	A31
GTBS	Gate bus	A25	A25
HDOF	Hold off	A5	-
HFTRCO	HF trigger control	A25	A32
ILØ6--LT	Interrupt level Ø6	A25	A12-A6
IOSLDL	I/O select delay	A25	A25
IOSLØ6LT	I/O select Ø6	A6	-
IOSLØ7LT	I/O select Ø7	A6	-
IOSLØ6L1	I/O select Ø6	A25	A25
IOSLØ7L1	I/O select Ø7	A25	A25
IVA	Invert A	A25	A32
IVB	Invert B	A25	A32
LADTCK	Latch delta-t clock	A25	A34
LAOSA	Latch offset A	A25	A25
LAOSB	Latch offset B	A25	A25
LATREV	Latch trigger event	A25	A25
LATRLV	Latch trigger level	A25	A25
LNTR	Line triggering	A25	A31
MM	Min-Max mode	A25	A33
MMPTØ1	Min-Max pointer Ø1	A33	-
NOA	Normal A	A25	A32
NOB	Normal B	A25	A32
OSA+/-	Offset A +/-	A25	A25
OSB+/-	Offset B +/-	A25	A25

Signal name	Description	Signal source	Signal destination(s)
PA/1A	Pre-amplifier /1 A	A25	A32
PA/1B	Pre-amplifier /1 B	A25	A32
PA/2A	Pre-amplifier /2 A	A25	A32
PA/2B	Pre-amplifier /2 B	A25	A32
PA/4A	Pre-amplifier /4 A	A25	A32
PA/4B	Pre-amplifier /4 B	A25	A32
PA25AHT	Pre-amplifier x2,5 A	A25	A32
PA25ALT	Pre-amplifier x2,5 A	A25	A32
PA25BHT	Pre-amplifier x2,5 B	A25	A32
PA25BLT	Pre-amplifier x2,5 B	A25	A32
PDSWØ	Peak detector switch Ø	A25	A33
PDSW1	Peak detector switch 1	A25	A33
PDSW2	Peak detector switch 2	A25	A33
PRIFA-XA	Probe information A	A28+A27	-
PRIFB-XA	Probe Information B	A30+A29	-
PT5ØA-LT	50 Ohm protection A	A27	-
PT5ØB-LT	50 Ohm protection B	A29	-
RDAOLD	Read auto offset level detection	A25	A25
RDDABS	Read data buffers	A25	A25
RDDTDA	Read delta-t data	A25	A25
RDPRIF--HT	Read probe information	A25	A25
RDPRIF--LT	Read probe information	A25	A25
RSMN	Reset min	A5	-
RSMX	Reset max	A5	-
RSSW	Reset slow	A5	-
SHA	Shift A	A25	A32
SHB	Shift B	A25	A32
SCEV--HT	Sample clock even	A25	A12-A5
SCEV-1HT	Sample clock even	A33	-
SCEV-2HT	Sample clock even	A26	-
SOSA	Shield offset A	A25	A50
SOSB	Shield offset B	A25	A50
STCV	Start conversion	A33	-
STSW	Set slow	A5	-
SWCK	Slow clock	A33	-
SWCKØ1	Slow clock Ø1	A25	A12-A5
SYSWTB	Synchronized slow time base	A5	-
TCEV--LT	Transport clock even	A25	A12-A5
TCEV-1LT	Transport clock even	A33	-
TCEV-2LT	Transport clock even	A26	-
TDLD	Delay trigger load	A5	-
TDUF	Trigger delay underflow	A25	A12-A5
TDUF-2	Trigger delay underflow -2	A26	-
TM5ØA	Termination 5Ø Ohm A	A25	A50-A35-A28
TM5ØB	Termination 5Ø Ohm B	A25	A35-A30
TRACDC	Trigger AC or DC	A25	A31
TRDULV	Trigger dual level	A25	A32
TRDUMO	Trigger dual mode	A25	A32
TREVLV	Trigger event level	A25	A31
TREVSP	Trigger event slope	A25	A32
TREV+/-	Trigger event +/-	A25	A25
TREV /5	Trigger event /5	A25	A31
TREV /5Ø	Trigger event /5Ø	A25	A31

Signal name	Description	Signal source	Signal destination(s)
TRID	Trigger indication	A26	-
TRLV	Trigger level	A25	A32
TRSOA	Trigger source A	A25	A32
TRSOB	Trigger source B	A25	A32
TRSP	Trigger slope	A25	A32
TRTVMO	Trigger TV mode	A25	A32
TSSHA	Take sample shift A	A25	A25
TSSHB	Take sample shift B	A25	A25
TSVGA	Take sample variable gain A	A25	A25
TSVGB	Take sample variable gain B	A25	A25
UPRD-1LT	Microprocessor read 1	A25	A25
VGA	Variable gain A	A25	A32
VGB	Variable gain B	A25	A32
ZEA-HX	Zero A	A25	A35-A27
ZEB-HX	Zero B	A25	A35-A29
ZECH	Zero channel	A5	-

DATA BUFFERS

ADDRESS-CONTROL BUFFER

I/O SELECT DELAY

ADDRESS DECODER

ATTENUATOR CONTROL LATCHES

VERTICAL SIGNAL-P²CCD LATCH

PROBE INFORMATION ADC

50Ω PROTECTION ADC

SAME RESISTORS ON MORE LOCATIONS

Figure 8.25.4 Unit A25 - MANAGEMENT UNIT - circuit diagram.

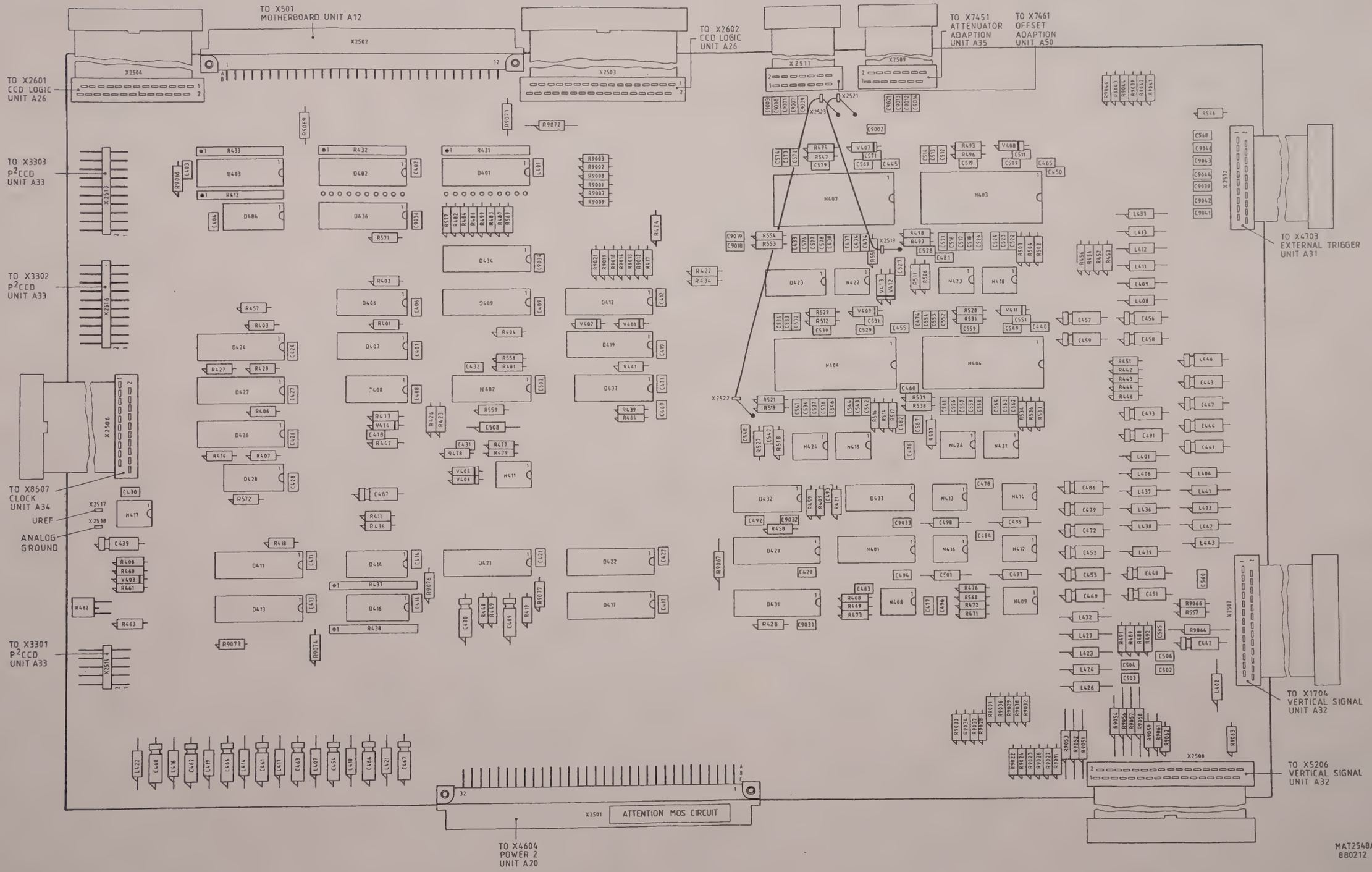
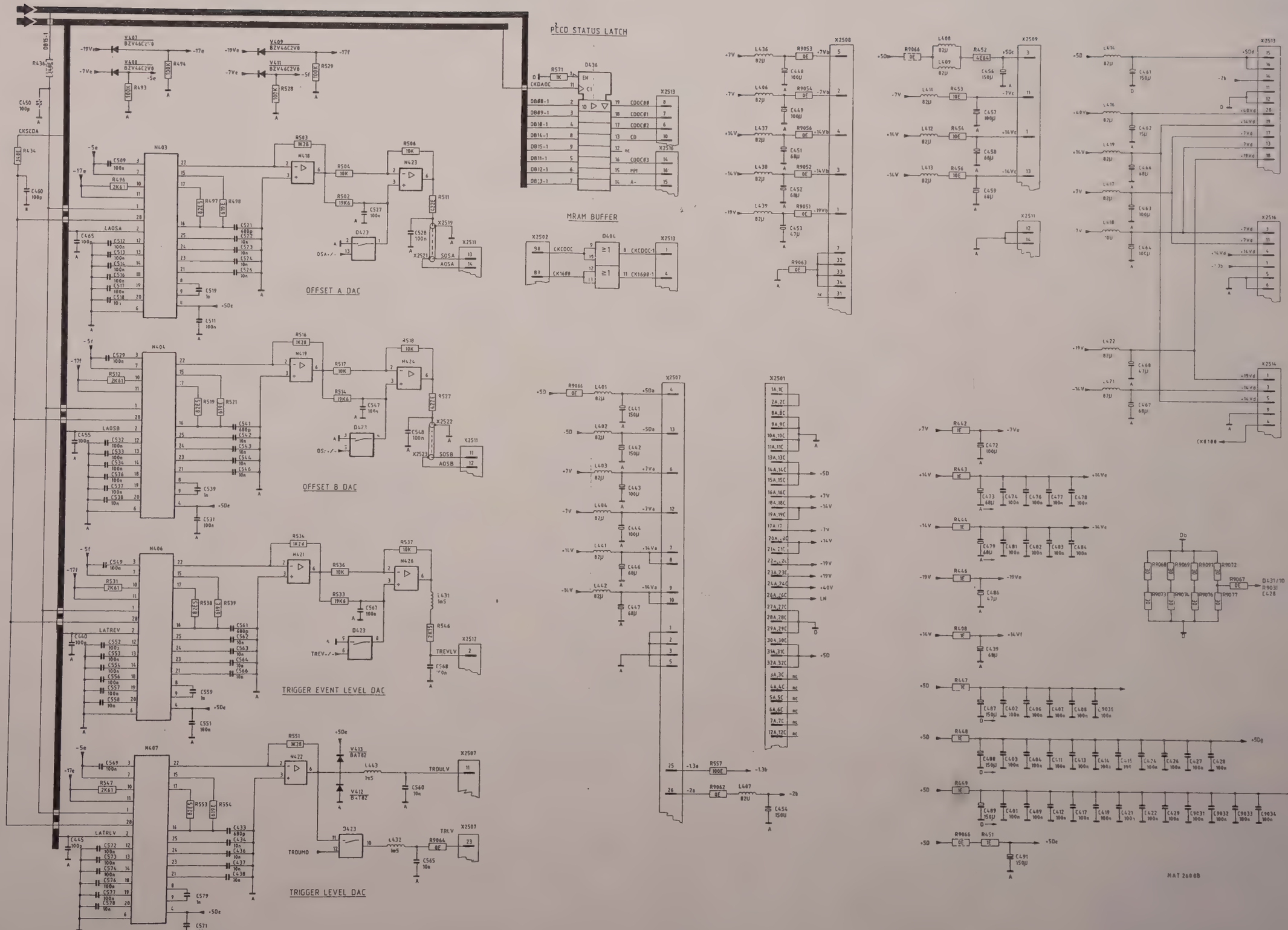


Figure 8.25.3 Unit A25 - MANAGEMENT UNIT - p.c.b. lay-out.

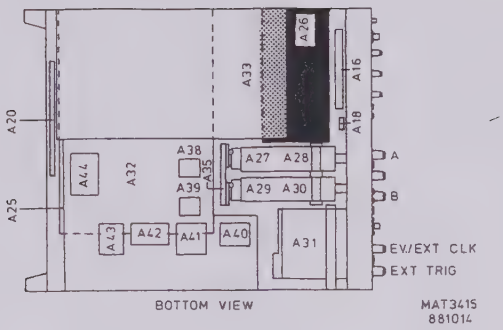

P²CD STATUS LATCH
MRAM BUFFER
OFFSET A DAC
OFFSET B DAC
TRIGGER EVENT LEVEL DAC
TRIGGER LEVEL DAC
CKSEDA
LAOSA
LAOSB
LATREV
LATRLV
OSA
OSB
SOSA
AOSA
SOSB
AOSB
TREVLV
TRLV
TROULV
TROUMO
CKCDOC
CK16Ø
CKCDOC-1
CK16Ø-1
CDOC#Ø
CDOC#1
CDOC#2
CD
CDOC#3
MM
A-
DB8Ø-1
DB81-1
DB10-1
DB15-1
DB11-1
DB12-1
DB13-1
MAT 26008

REF.NR	TYPE	Vcc	PIN	Vee	PIN	GND	PIN
D401	74LS 245	+5Dg	20			D	10
D402	74LS 245	+5Df	20			D	10
D403	74HCT573	+5Dg	20			D	10
D404	74F32	+5Df	14			D	7
D406	74HCT138	+5Df	16			D	8
D407	74HCT238	+5Df	16			D	8
D408	74HCT14	+5Df	14			D	7
D414,416	7407	+5Dg	14			D	7
D423	74HCT4066	+5De	14			A	7
D411,413,427	74HCT574	+5Dg	20			D	10
D409,412,417,421	74HCT574	+5Dh	20			D	10
D422,429,431	74HCT574	+5Dh	20			D	10
D433	74HCT238	+5Dh	16			D	8
D424,426	74HCT299	+5Dg	20			D	10
D428	74HCT107	+5Dg	14			D	7
D432	74HCT123	+5Dh	16			D	8
D419,434	74HCT541	+5Dh	20			D	10
D436	74HCT574	+5Df	20			D	10
D437	DQ0044	+5Dh	4	-14Ve	18	D	1
N403,404,406,407	TDA1540D	+5De	4			D/A	6
N402	AD7541AJN	+5Dg	1			D/A	18/5
N401	AD7541AJN	-14Ve	16			A	3/2
N408,409,411	UA714TC	-14Ve	7	-14Ve	4	A	4
N417	UA714TC	-14Ve	7			A	4
N412,413,414,416	LF398N	-14Ve	1	-14Ve	4	A	7
N418,419,421,422	UA714TC	-14Ve	7	-14Ve	4		
N423,424,426	UA714TC	-14Ve	7	-14Ve	4		

SAME COMPONENTS ON MORE LOCATIONS

Figure 8.25.5 Unit A25 - MANAGEMENT UNIT - circuit diagram.

UNIT A26 - CCD LOGIC UNIT



CONTENTS

8.26.1 General information..... 8.26-1
8.26.2 Circuit description..... 8.26-1
8.26.3 Signal name list..... 8.26-3

8.26.1 General information

The CCD logic unit contains the logic which is used for controlling the P^2CCDs on unit A33. A part of the logic is fitted on the MINI CCD LOGIC unit (A49) which is fitted on this unit.

8.26.2 Circuit description

The AUTO TRIGGER logic causes the generation of the TDUF-2 signals when no triggers appear. The TDUF-2 signal is a derived trigger signal for the ACL.
The auto trigger logic is active when the AUTB signal is high, which will be assumed in the following description.
When HDOF at X2637 goes down, this is the sign of the ACL to start a new acquisition. Now pin 4 of D6008 gives a low pulse of 25 ms.
When TRSGØ1LT stays high, because no triggers appear, flip flop D6009 (the auto flip flop) receives a clock at the end of the 25 ms pulse at pin 11. The ENAURSLT signal goes low. Because it is fed back to pin 13 of D6007 further clock signals are blocked; the auto flip flop stays in this state.
The ENAURSLT signal sets flip flop D6009 via pin 4. The TRID signal, goes low, which is read by the microprocessor. This will light the NOT TRIG´D pilot lamp on the front panel.
In this situation pin 8 of D6009 is high and HDOF is low. Now EVUF goes high via R6402, D6011, D6007 and D6012. This generates on unit A49 the ENTDCNLE signal after one or two FSTB--HE pulses, depending on the DTPUSL signal. ENTDCNLE enables the trigger delay counter. Because ENAURSLT makes pin 3 of D6012 high, only the fast part of the trigger delay counter (the part in IC D6001 and IC D6022) counts down to generate TDUF-2 (see also the description of the trigger delay counter next).
The ENAURSLT signal enables RSAUFF on unit A49 to go high when a trigger occurs. This sets the auto flip flop D6009 at pin 10 via D6008, D6007 and D6011. Now ENAURSLT goes high, which is the starting situation.
When no triggers appear ENAURSLT stays low, which results in the generation of TDUF-2, every time when HDOF goes down.

When AUTB is low only flip flop D6009, which generates TRID, is enabled. TRID is set low by a clock from TDLD at pin 3.
If a trigger appears, TRSGØ1LT goes low, which resets the flip flop via pin 1; TRID goes high. If no trigger appears, TRID stays low. The microprocessor reads the status of TRID to control the status of the pilot lamp NOT TRIG´D.

The STAL signal is generated when HDOF is high and RSSW is low. (see also section 8.49.2 aliasing detection circuit).

The CCD LOGIC + FAST TIME BASE DIVIDER is integrated in an ACE (Advanced Customised ECL), IC D6001. It contains various fast dividers to generate the sample and transport clock from the FSCK signal in the P^2CCD mode and the Random Sampling mode.
It also contains the logic for the change over to the slow clock (SWCK) for the read out stroke in the P^2CCD mode and the random sampling mode. In the Direct (special) mode and in the Roll mode the sample and transport clocks are also derived from SWCK.
The DC-level of FSCK--XA controls the duty-cycle of the signals inside the ACE.

The TRIGGER DELAY COUNTER consists of a 25 bit counter. The first 5 bits are in the ACE (for speed reasons), the next 4 bits are in a fast Schottky TTL counter (D6022), the remaining bits are in 4 CMOS counters (D6026...D6029). Transistors V6008 and V6009 are a buffer. Each counter can be preset with a value which is stored by the microprocessor in the latches D6033...D6037. The latches for the counter stage in the ACE are integrated in the ACE.
When the slower part of the trigger delay counter (D6022 andD6026...D6029) has counted down the TDTC---LT is generated. This is inside the ACE combined with the status of the high speed counter stage. As soon as this stage has counted down, the TDUF-2 signal goes high.

The EVENTS COUNTER consists of a 16 bits counter (D6016...D6019). It can be preset with a value, which is stored by the microprocessor in the latches D6031 and D6032. The EVSG--HE signal represents the events signal that can be connected to the EVENTS/EXT CLK BNC input on the frontpanel. It is converted to TTL level by the circuitry around transistor V6001...V6004. The output
signal of this circuit (ETCK-2) clocks the events counter and is also applied to the acquisition control logic (unit A5). This path is only effective when an external clock is selected.
The counting down of the events counter is enabled by the ENEVCNLT signal. When the events counter has counted down the EVUF signal is generated.
Both the events counter and the trigger delay counter are preset by the TDLD-1LT signal.
During the signal acquisition stroke in P^2CCD-mode the trigger delay counter counts down after a preset caused by the going low of TDLD (pin 33 of X2602).
During the zero acquisition stroke in P^2CCD-mode the trigger delay counter counts down after a preset caused by the going low of RSSW (pin 28 of X2602).
Interference caused by the trigger delay counter will be eliminated during the digital substraction for leakage correction in the DPU (see also section 8.33).

The CONTROL LATCH latches various control signals from the microprocessor for this unit and unit A49.

The ADDRESS DECODER decodes various addresses which are used to clock the information from the microprocessor in the right latches.

8.26.3 Signal name list

UNIT A26

Signal name	Description	Signal source	Signal destination(s)
ABØ1-1...Ø4-1	Address bus Ø1-1...Ø4-1	A25	-
ALID	Aliasing indication	A49	-
AUTB	Auto time base	A26	A26
CDRD-2	P^2CCD read	A26	A25, A25-A33
CDSGC2	P^2CCD sample gate control 2	A25	-
CKØ1ØØ	Clock 1ØØ kHz	A33	-
DBØØ-1...DB15-1	Data bus ØØ-1...15-1	A25	-
DB-1	Data bus 1	A26	A26
DR	Direct / Roll mode	A26	A49
DTPUSL	Delta-t pulse select	A26	A49
ENAURSLT	Enable auto reset	A26	A26, A49
ENEV--LT	Enable events	A26	A49
ENEVCNLT	Enable events counter	A49	-
ENTDCNLE	Enable trigger delay counter	A49	-
ETCK-2	External clock 2	A26	A25
EVPSØØ...15	Events preset ØØ...15	A26	A26
EVSG--HE	Events signal	A32	-
EVUF	Events underflow	A26	A49
EVUF-1	Events underflow 1	A26	A26
FSCK	Fast sample clock	A34	-
FSCK--HE	Fast sample clock	A26	A26
FSCK--LE	Fast sample clock	A26	A26
FSCK--XA	Fast sample clock	A26	A26
FSTB--HE	Fast time base	A26	A49
HDOF	Hold off	A26	A26
HDOF--LT	Hold off	A5	-
IOSLØ6LT	I/O Select Ø6	A6	-
MMSLØØ	Min/max select ØØ	A26	A49
MMSLØ1	Min/max select Ø1	A26	A49
MNDLIN	Min delay in	A26	A49
MNDLOT	Min delay out	A49	-
MXDLIN	Max delay in	A26	A49
MXDLOT	Max delay out	A49	-
PSEG	Preset enable ground	A26	A26
RSALIDLT	Reset aliasing indication	A26	A49
RSAUFF	Reset auto flip flop	A49	-
RSMN	Reset min	A5	-
RSMNPD	Reset min peak detector	A49	-
RSMX	Reset max	A5	-

Signal name	Description	Signal source	Signal destination(s)
SCEV	Sample clock even	A26	A49
SCEV-2HT	Sample clock even 2	A26	A25-A33
SCEVA-LE	Sample clock even A	A26	A24
SCEVB-LE	Sample clock even B	A26	A24
SCOD	Sample clock odd	A26	A49
SCODA-LE	Sample clock odd A	A26	A24
SCODB-LE	Sample clock odd B	A26	A24
SPDTSWHE	Stop delta-t sweep	A49	-
SPDTSWLE	Stop delta-t sweep	A49	-
STAL	Start aliasing detection	A26	A49
STDTSWHE	Start delta-t sweep	A49	-
STDTSWLE	Start delta-t sweep	A49	-
STSW	Set slow	A5	-
STTDCNLE	Start trigger delay counter	A26	A49
SWCK	Slow clock	A33	
SYSWTB	Synchronised slow time base	A5	-
SYSWTBHE	Synchronized slow time base	A49	-
TCEV-2LT	Transport clock even 2	A26	A25-A33
TCEVA-HE	Transport clock even A	A26	A24
TCEVB-HE	Transport clock even B	A26	A24
TCODA-HE	Transport clock odd A	A26	A24
TCODB-HE	Transport clock odd B	A26	A24
TDCNCK	Trigger delay counter clock	A26	A26
TDLD	Trigger delay load	A5	-
TDLD-1LT	Trigger delay load 1	A26	A26
TDPSØØ...TDPS15	Trigger delay preset ØØ...15	A26	A26
TDTC--LT	Trigger delay terminal count	A26	A26
TDUF-2	Trigger delay underflow 2	A26	A25, A49
TRID	Trigger indication	A26	A25
TRSG	Trigger signal	A32	-
TRSGØ1LT	Trigger signal Ø1	A49	-
WRØ6ØØ... WRØ6ØA	Write Ø6ØØ...Ø6ØA	A26	A26

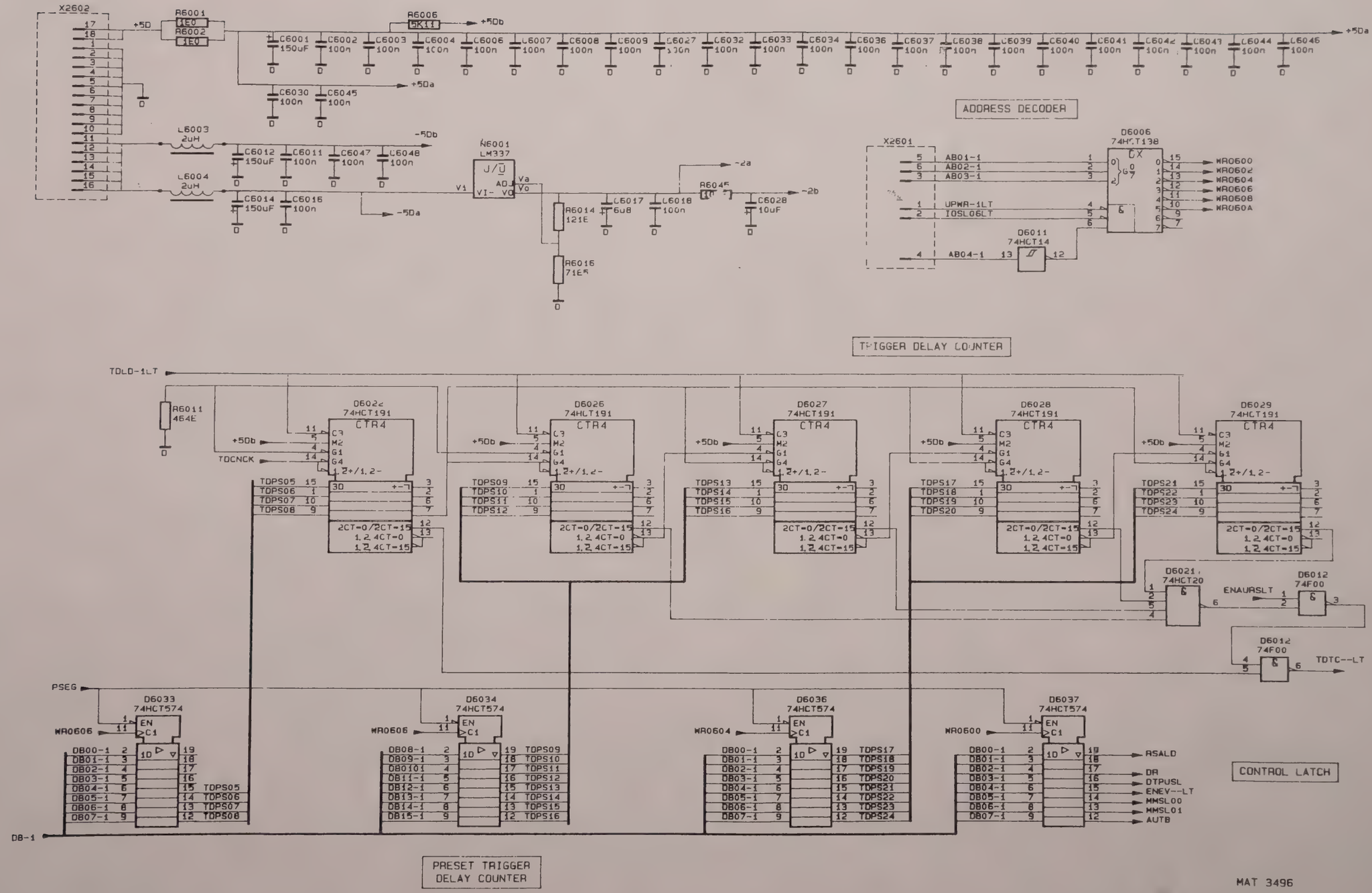


Figure 8.26.3 Unit A26 - CCD LOGIC - circuit diagram.

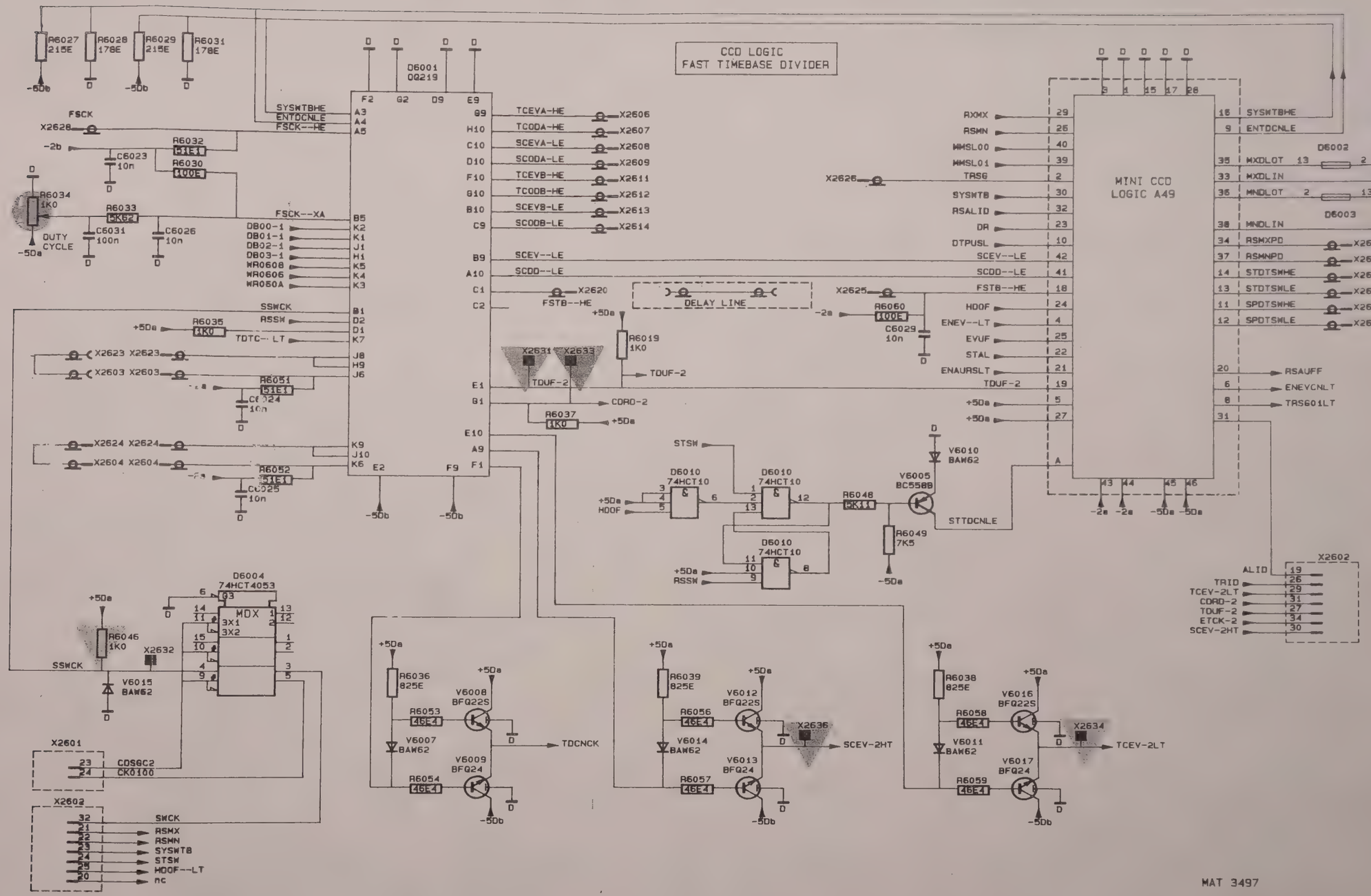
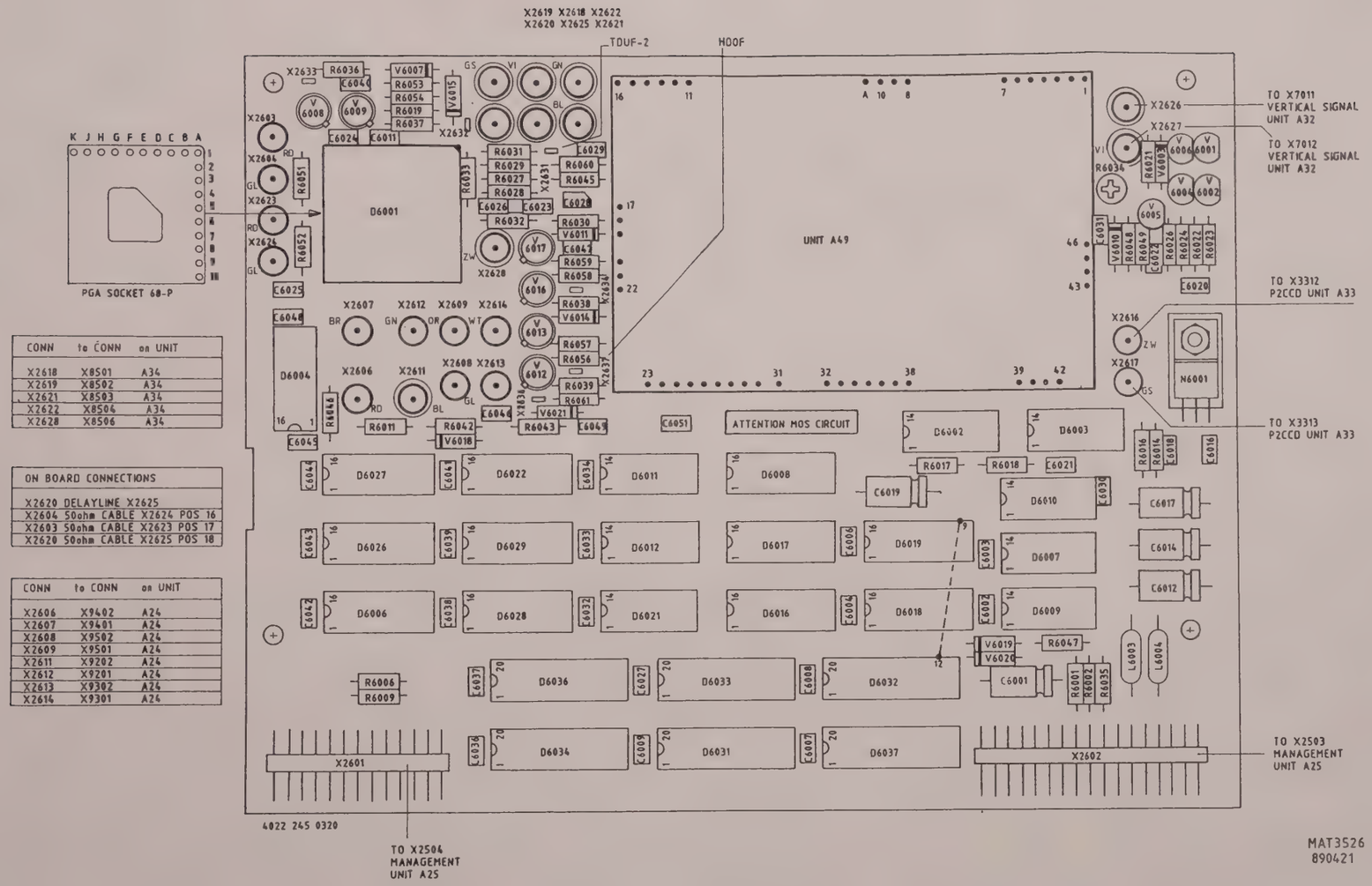


Figure 8.26.4 Unit A26 - CCD LOGIC - cicuit diagram.

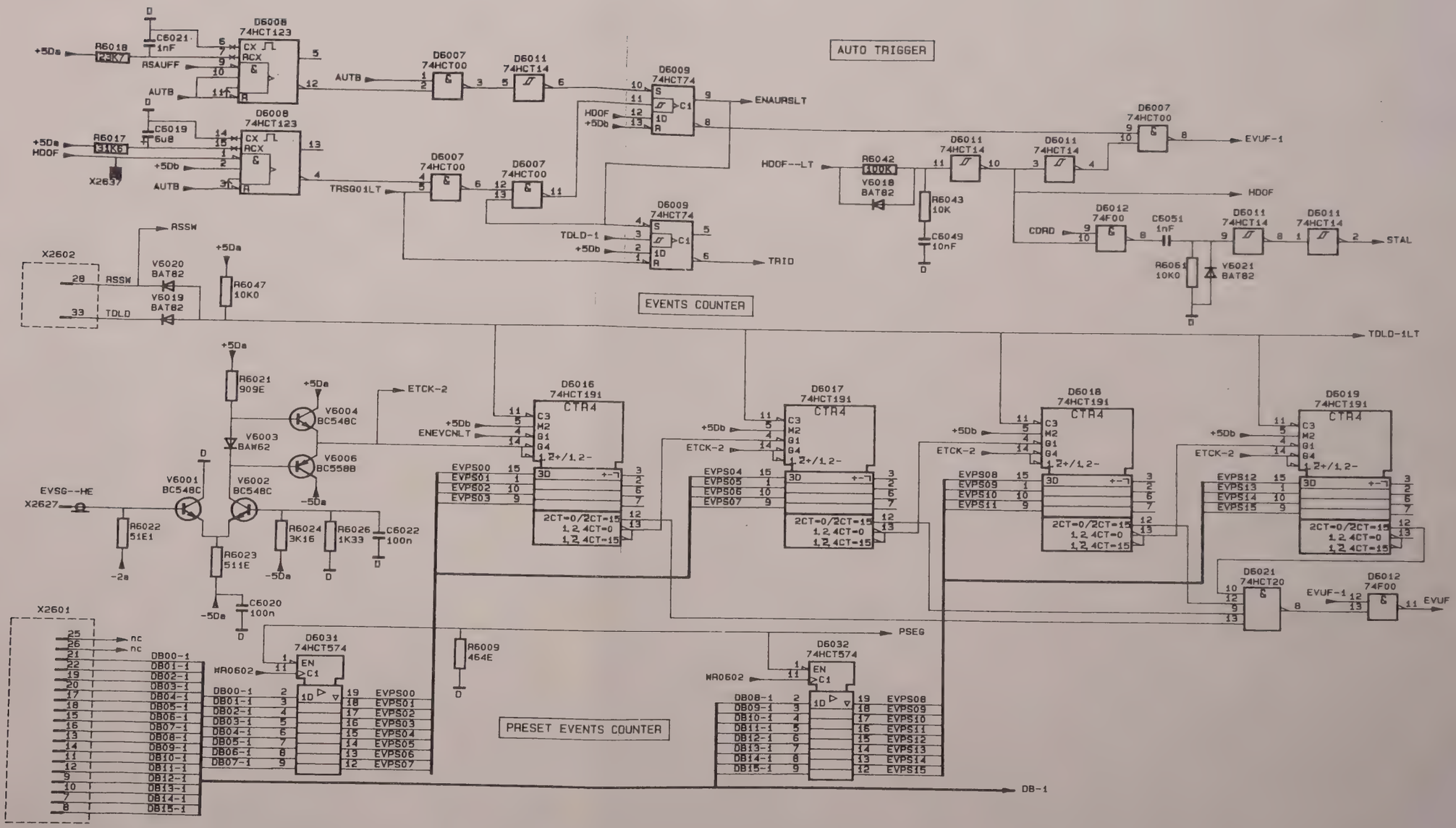


CONN	to CONN	on UNIT
X2618	X8501	A34
X2619	X8502	A34
X2621	X8503	A34
X2622	X8504	A34
X2628	X8506	A34

ON BOARD CONNECTIONS
X2620 DELAYLINE X2625
X2604 50ohm CABLE X2624 POS 16
X2603 50ohm CABLE X2623 POS 17
X2620 50ohm CABLE X2625 POS 18

CONN	to CONN	on UNIT
X2606	X9402	A24
X2607	X9401	A24
X2608	X9502	A24
X2609	X9501	A24
X2611	X9202	A24
X2612	X9201	A24
X2613	X9302	A24
X2614	X9301	A24

Figure 8.26.1 Unit A26 - CCD LOGIC - p.c.b. lay-out.



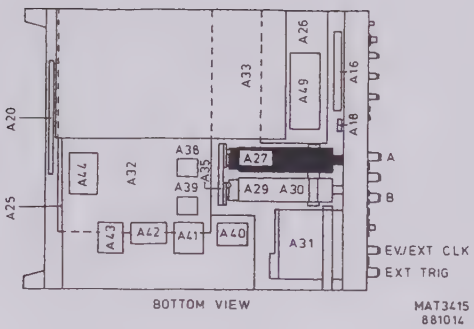
REF.NR	TYPE	Vcc +5Da	DIG. GND	Vee -5Db
D6001	000219	*	*	
D6002	60Z14A020H		1, 7, 14	
D6003	60Z14A020H		1, 7, 14	
D6004	74HCT4053	16	6, 8	7
D6006	74HCT138	16	8	
D6007	74HCT00	14	7	
D6008	74HCT123	16	8	
D6009	74HCT74	14	7	
D6010	74HCT10	14	7	
D6011	74HCT14	14	7	
D6012	74F00	14	7	
D6021	74HCT20	14	7	
D6022	74F191	16	8	

REF.NR	TYPE	Vcc +5Da	DIG. GND
D6016 D6017 D6018 D6019 D6026 D6027 D6028 D6029	74HCT191	16	8
D6031 D6032 D6033 D6034 D6036 D6037	74HCT574	20	10
N6001	LM337		

MAT 3495

Figure 8.26.2 Unit A26 - CCD LOGIC - circuit diagram.

UNIT A27(A29) - HF VERTICAL ATTENUATOR



CONTENTS

8.27.1 Introduction..... 8.27-1
8.27.2 Circuit description..... 8.27-1
8.27.3 Signal name list..... 8.27-3

8.27.1. Introduction

The A and B channel attenuators are identical: so only A is described. Every attenuator module consists of two printed circuit boards:

- the h.f. attenuator unit
- the l.f. attenuator unit (see section 8.28)

The signal names in this description and in the circuit diagram between brackets are valid for the attenuator of channel B.

8.27.2 Circuit description (see figure 8.27.2)

The input signal from the Y BNC connector (A or B) is divided into five paths:

- three identical a.c.-coupled h.f. signal paths with different capacitive attenuation factors
- a 50-Ohm termination path
- a direct-coupled signal path to the l.f. attenuator unit A28 (A30)

The h.f. signal paths and the 50-Ohm termination are selected by the contacts of reed relays mounted on the l.f. unit and controlled by buffer D6903 (see figure 8.28.2.). This buffer is controlled by the Management unit A25 via the adaption unit A35.
Dealing first with the 50-Ohm termination, the reed relay contact connects the input signal across 50-Ohm (an array with two 100-Ohm resistors connected in parallel to earth). The array includes a temperature sensor which activates a temperature-sensing circuit (N6803) if the input signal exceeds 5 V.
The three h.f. paths are a.c.-coupled via C6809 (1x range) and C6814 (0.1x range), C6801 (0.01x range) which form part of the RC attenuators. The attenuator stages are each followed by a FET impedance converter stage (V6806 in the 1x path). A diode clipper in the gate circuit of the two lower ranges protects the input source follower of the impedance converter from excessive input voltages.

The impedance converter is switched by a PNP transistor (V6807) in its drain circuit. A +5 V switches it off and a +4,2 V switches it on.
The signal is then coupled via a diode (V6812) to transistor V6829, part of a summation stage (where also the l.f. signal is added, LFXA (B) via V6836 and V6833.
The truth-table of the input relay contacts is given in section 8.28.2.
When "0" coupling is selected, (ZEA-Hx ZEB-Hx active high) transistor V6828 takes over the current which is normally drawn by one of the coupling diodes (V6811 or V6812) in the h.f. path. This serves to maintain the circuit in d.c. balance.
Signal ZEA-Lx (ZEB-Lx) is routed to the LF attenuator to switch off the d.c. signal path.
The gain of the summation stage is determined by the ratio of its collector resistance to its emitter resistance, $\frac{Rc}{Re}$.
In the xl position, the collector resistance of V6829 is R6851 + (R6850//R6863), switched by V6819.
Switching is achieved by the logic level applied to the base of V6826; 0 V selects the xl range, +5 V selects the x5 range (x5 range not used).
The output signal from the summation stage V6829 is routed to the output amplifier with V6837 and V6839. The output signal from this amplifier is routed to the vertical signal unit A32 via a coaxial cable. A part of the output signal is routed to the feedback loop on the l.f. attenuator unit, HFXA(B), for LF and d.c. compensation.

There are three auxiliary circuits on the HF attenuator unit:

- Multiplexer D6801 for h.f. attenuator switching
- Window discriminator for 50-Ohm terminator protection (N6802)
- Temperature sensing circuit for 50-Ohm input termination (N6803)

Multiplexer D6801 is controlled by the signals ATSW0A(B) and ATSW1A(B) to select the xl, x10 and x100 capacitive attenuators, on pins 12, 14 and 15 respectively. These pins are connected with V6807/base, V6816/base and V6802/base.
The xl and x5 ranges are also selected by switching 0 V or +5 V to V6826/base (x5 range is not used). These voltages are made by multiplexer D6801/3, 4 and voltage divider resistors R6871 and R6862.

The window discriminator checks the voltage across the h.f. attenuator output by means of two operational amplifiers N6802. One detects the positive signal peak and the other detects the negative signal peak. The resultant outputs are summed, and if the input voltage of 5 V is exceeded during this measurement, the summation amplifier N6802/8, 9, 14 switches off transistor V6842. This gives a logic high PT50A-LT (PT50B-LT) (unsafe) signal to the central microprocessor. In this situation it is not possible to switch from 1M-Ohm to 50-Ohm input impedance.

A temperature sensing circuit of operational amplifier N6803. The temperature of the 50-Ohm termination resistor is measured by a 1 k-Ohm resistor, present in the OM545, with a temperature coefficient of +0,75 percent per degree Celcius. If the temperature gets too high, operational amplifier input N6803/2 goes high and switches V6846 on.

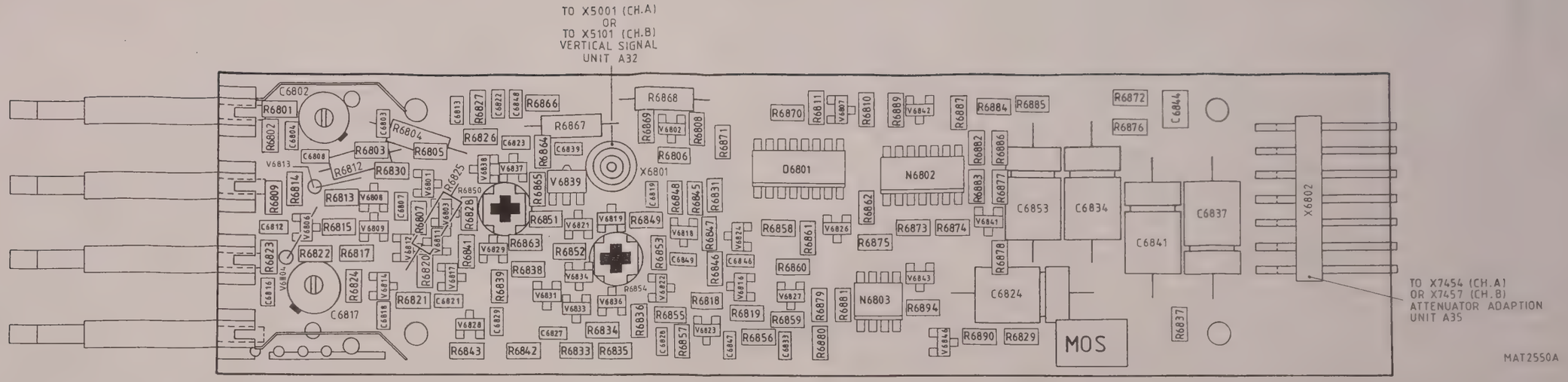
V6846 switches resistor R6890 between the probe indication line PRIFA-XA (PRIFB-XA) and earth. The central microprocessor knows that either a high-ohmic probe or a 50-Ohm overload is present now. The detection between the two is done as follows:

- The window of the discriminator is changed from 5 V to 25 V in combination with the x0,01 attenuator section, via a low level from op-amp output D6803/1 applied to the window discriminator via diode V6843 and switching FET V6841.
- The microcomputer switches the x0,01 attenuator section on for a moment and looks at the discriminator output (PT50A-LT(B): if the output is low, the voltage across the 50-Ohm resistor is between 5 and 25 V and the current through the 50-Ohm resistor is such that it can be switched off. With the discriminator output being high, the voltage is above 25 V and the current through the 50-Ohm resistor is too high to be switched off. Now a warning becomes visible on the C.R.T. of the instrument.
- Some seconds after having switched-off the 50-Ohm resistor, the microprocessor looks again to the probe indication line PRIFA-XA (PRIFB-XB). The temperature-sensing resistor is cooled down again and the probe indication line must be free again; if not, the microprocessor knows that it was not a 50 Ohm overload but that a high-ohmic probe is connected.

8.27.3 Signal name list

UNIT A27 (A29)

Signal name	Description	Signal source	Signal destination(s)
ATSWØA	Attenuator switch Ø A	A35	-
(ATSWØB)	Attenuator switch Ø B	A35	-
ATSW1A	Attenuator switch 1 A	A35	-
(ATSW1B)	Attenuator switch 1 B	A35	-
HFXA	High frequency A	A27	A35-A28
(HFXB)	High frequency B	A29	A35-A30
LFXA	Low frequency A	A28	-
(LFXB)	Low frequency B	A30	-
PRIFA-XA	Probe indication A	A27+A28	A35-A50-A25
(PRIFB-XB)	Probe indication B	A29+A30	A35-A25
PT5ØA-LT	Protect 5Ø Ohm A	A27	A35-A50-A25
(PT5ØB-LT)	Protect 5Ø Ohm B	A29	A35-A25
ZEA-HX	Zero A	A25	-
(ZEB-HX)	Zero B	A25	-
ZEA-LX	Zero A	A27	A35-A28
(ZEB-LX)	Zero B	A29	A35-A30



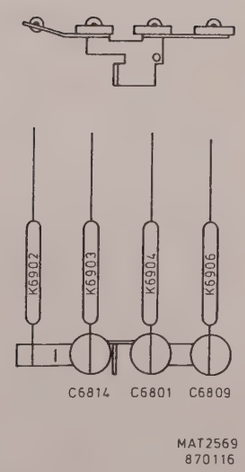


Figure 8.27.1 Unit A27(A29) - HF ATTENUATOR - p.c.b. lay-out.

SIGNAL NAMES BETWEEN BRACKETS ARE VALID FOR UNIT A29 (CHANNEL B)

IMP.CONV

SUMMATION STAGE

WINDOW DISCRIMINATOR

50Ω TEMP SENSING

NOT USED

LF RESPONSE 50mV

LF RESPONSE 500mV

		ATTENUATION
0	0	1×
0	1	0,1×
1	0	0,01×

TYPE	MARKING
BAW56	A1
BAT17	A3
BAV70	A4
BAV99	A7
BCW30	C2
BCW30R	C5
BCW33R	C6
BFS20	G1
BFS20R	G4
BSR56	M4
BFR92	P1
BFR92R	P4
BFR93	R1
BFR93R	R4
BFS12	S8
BFT92	W1
BFT93	X1
BFG19	FF

POS	TYPE
D6801	HEF4052
N6802	LM339
N6803	LM358
N6804	OM545

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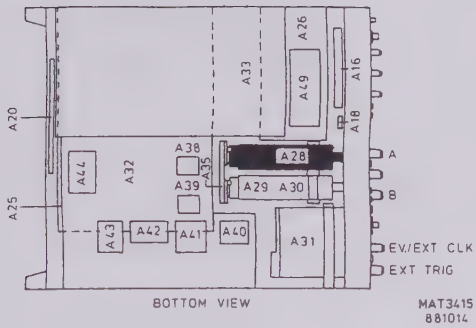
Figure 8.27.2 Unit A27(A29) - HF ATTENUATOR - circuit diagram.

UNIT A28(A30) - LF VERTICAL ATTENUATOR



CONTENTS

8.28.1 Introduction..... 8.28-1
8.28.2 Circuit description..... 8.28-1
8.28.3 Signal name list..... 8.28-3

8.28.1 Introduction

The A and B channel attenuators are identical: so only A is described. Every attenuator module consists of two printed circuit boards:

- the h.f. attenuator unit (see section 8.27)
- the l.f. attenuator unit

The signal names in this description and in the circuit diagram between brackets are valid for the attenuator of channel B.

8

8.28.2 Circuit description (see figure 8.28.2)

The function of the LF attenuator unit is to compensate LF signals and to prevent DC drift. Also the DC OFFSET is controlled in this unit. The l.f. or d.c. path is chosen by the AC/DC reed relay switch contact (K6901). When "0" input coupling is chosen, the FET switch V6904 is switched off by signal ZEA-LX (ZEB-LX) on its gate. Then FET V6903 switches the input to earth potential via V6909. The diodes V6901 and V6902 protect the switch V6903 against switch-off spikes. The signal on the d.c. path is fed to the operational amplifier N6901 together with the d.c. input (via R6909, HFXA/B).
Any difference in the comparator is applied to the summation stage LFXA(B) consisting of V6836, V6833 and V6829 (on the HF unit). Note that when added, the h.f. signal and l.f. and d.c. signal shown at the summation stage form a reconstituted version of the signal applied to the input.
Feedback capacitors in the operational amplifier N6901 ensure that the frequency response of the d.c. path matches that of the a.c. path. Feedback capacitor C6906 is always in circuit. The feedback capacitors C6907 and C6908 are switched into the circuit by the FET-switches V6906 and V6907. In the x0,1 attenuation position C6906 and 6907 are in circuit. In the x0,01 attenuation position C6906, C6907 and C6908 are all in circuit as feedback capacitance. The connection between the inverting input of operational amplifier N6901 and the output of the HF attenuator unit HFXA(B) is made via a network of switchable feedback resistors. The amount of resistors switched into the circuit by FET-switches depends on the attenuator setting.

The feedback resistance networks are:

x1 : R6909 (always in circuit)
x0.1 : R6909//R6912 switched by V6911
x0.01: R6909//R6912//(R6913//R6914) switched by V6911 and V6913

Via the switchable feedback resistor network also the OFFSET level [OSA-(OSB-)] is applied to the comparator N6901 via R6911, R6920, R6916 and R6922.
In this way vertical shift of the base-line is achieved.

The FET switches V6906, V6907 (to switch the feedback capacitors) and V6911, V6913 (to switch the feedback resistors) are controlled by D6901 which on its turn is controlled by the data bus signals ATSW0A(B) and ATSW1A(B).

The relays on the HF unit (K6902...K6906) and K6901 on this unit are controlled by the data bus via N6903. The truth-table is given below.

Relay contact:	K6901	K6804	K6802	K6803	K6801
Relay coil :	K6901	K6902	K6903	K6904	K6906
Output N6903 :	16	15	14	13	12
5 mV/div	X	X	H	H	L
50 mV/div	X	X	L	H	H
500 mV/div	X	X	H	L	H
"0"	X	X	H	H	H
"AC"	H	X	X	X	X
"DC"	L	X	X	X	X
50 Ohm	X	L	X	X	X

H: not active, relay contact open
L: active, relay contact closed
X: don't care

8.28.3 Signal name list

UNIT A28(A30)

Signal name	Description	Signal source	Signal destination(s)
ACDCA	AC/DC A	A25	-
(ACDCB)	AC/DC B	A25	-
ATSWØA	Attenuator switch Ø A	A35	-
(ATSWØB)	Attenuator switch Ø B	A35	-
ATSW1A	Attenuator switch 1 A	A35	-
(ATSW1B)	Attenuator switch 1 B	A35	-
AT1A	Attenuator switch x1 A	A25	-
(AT1B)	Attenuator switch x1 B	A25	-
AT1ØA	Attenuator switch x1ØA	A25	-
(AT1ØB)	Attenuator switch x1ØB	A25	-
AT1ØØA	Attenuator switch x1ØØ A	A25	-
(AT1ØØB)	Attenuator switch x1ØØ B	A25	-
HFXA	High frequency A	A27	-
(HFXB)	High frequency B	A29	-
LFXA	Low frequency A	A28	A35-A27
(LFXB)	Low frequency B	A30	A35-A29
OSA	Offset A	A25	-
(OSB)	Offset B	A25	-
OSBIAAXA	Offset bias A	A35	-
(OSBIABXA)	Offset bias B	A35	-
PRIFA-XA	Probe indication A	A27+A28	A35-A50-A25
(PRIFB-XA)	Probe indication B	A29+A30	A35-A25
TM5ØA	Termination 5Ø Ohm A	A25	-
(TM5ØB)	Termination 5Ø Ohm B	A25	-
ZEA-LX	Zero A	A27	-
(ZEB-LX)	Zero B	A29	-

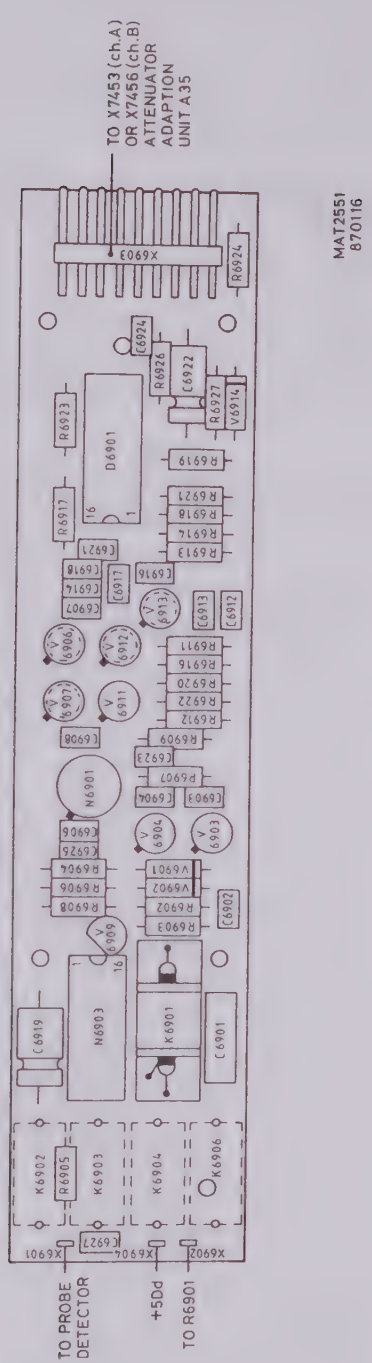
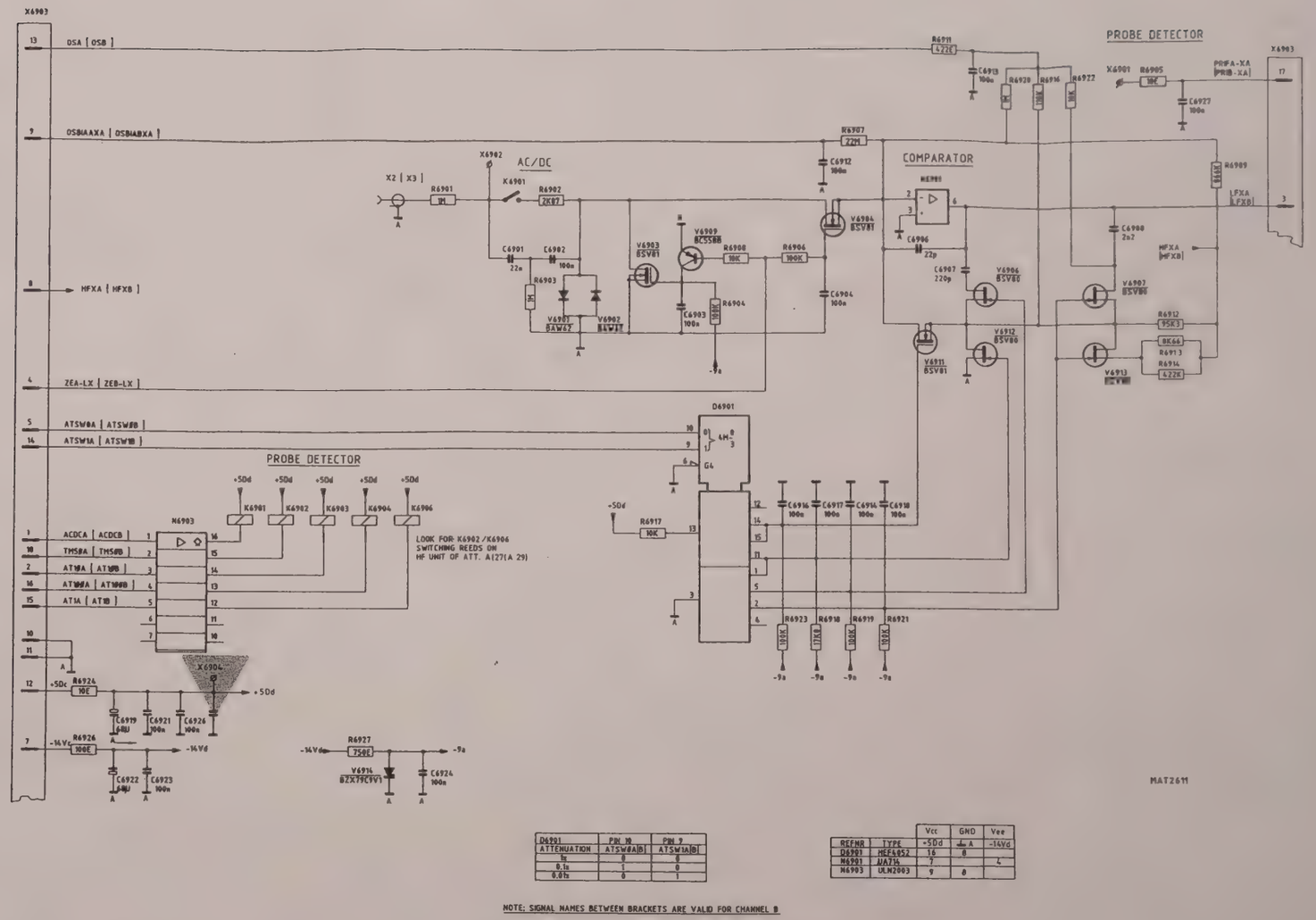


Figure 8.28.1 Unit A28(A30) LF ATTENUATOR - p.c.b. - lay-out.



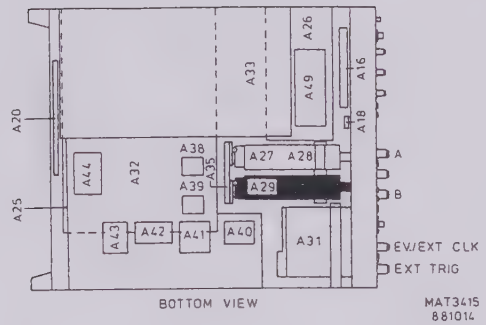
D6901 ATTENUATION	PIN 10 ATSW8A|B|	PIN 7 ATSW1A|B|
1x	0	0
0.1x	1	0
0.01x	0	1

REFNR	TYPE	Vcc +50d	GND ⏚ A	Vee -14Vd
D6901	MEF4052	16	8	
N6901	UA714	7		4
N6903	ULN2003	9	8	

NOTE: SIGNAL NAMES BETWEEN BRACKETS ARE VALID FOR CHANNEL B

Figure 8.28.2 Unit A28(A30) - LF ATTENUATOR - circuit diagram

UNIT A29 - HF VERTICAL ATTENUATOR



CONTENTS

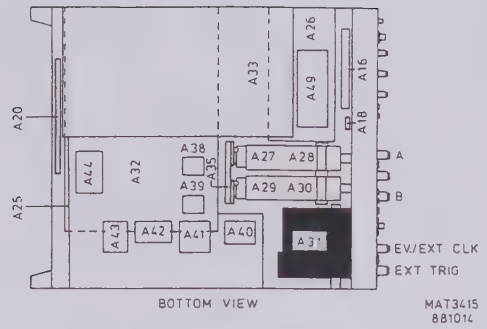
8.29.1 Introduction..... 8.29-1

8.29.1 Introduction

See section 8.27.

The circuit description, signal name list, p.c.b. lay out and circuit diagram of this unit are idential to unit A27.
The signal names for channel B are given between brackets.

UNIT A31 - EXTERNAL TRIGGER UNIT



CONTENTS

8.31.1 Introduction..... 8.31-1
8.31.2 Circuit description of the EXT TRIG input..... 8.31-1
8.31.3 Circuit description of the EVENTS/EXT CLOCK input..... 8.31-2
8.31.4 Signal name list..... 8.31-3

8.31.1 Introduction

This unit consists of two main circuits:

The EXT TRIG input and the EVENTS/EXT CLOCK input.

On this unit S.M.D.'s (Surface Mounted Devices) and "normal" components are used together on one p.c.b..
The handling of S.M.D.'s is described in section 12.3.1.

Via the EXT TRIG input the time base can be triggered externally and via the EVENTS/EXT CLOCK input the time base can be started after a preselected number of trigger events and the horizontal deflection speed can be controlled via the CLOCK signals (in EXT CLOCK mode) applied to this input.

8.31.2 Circuit Description of the EXT TRIG input (see figure 8.31.2.)

The control signals for this unit are coming from the management unit A25.
The EXT TRIG input unit is similar to the vertical attenuator unit except that there are only two different attenuator positions, x0,2 (:5) and x0,02 (:50). Consequently, the EXT TRIG and EVENTS/EXT CLOCK input socket is coupled to two h.f. paths and one l.f. path. Alternatively, a LINE input signal can be switched via FET V4739 to provide triggering.

The two h.f. paths have no input switching reed relay contacts.
The x0,2 attenuator consists of the capacitive-network C4701, R4701, R4702, C4702 in the gate circuit of FET V4701. A logic low control signal ETTR/5 on the base of V4728 causes this transistor to conduct, which turns on source-follower FET V4701.
In turn, V4703 conducts and the signal is passed via switching diode V4704 to the summation amplifier V4709, V4711.
The logic low control signal is also applied to a switching network, V4719, V4721, V4722, which provides the collector load via diode V4727 for V4709 in the x0,2 position. The x0,2 gain adjust is R4751.

The x0,02 attenuator consists of a double capacitive-network C4707, R4708, R4709, C4708, and R4711, C4709, R4712, C4711 in the gate circuit of FET V4706. The control and switching circuits (V4731, V4726, V4724, V4723) are identical to the x0,2 position section. When the x0,02 position is selected, the gain adjustment in the collector load of V4709 is R4753.

The 1.f. path is connected via resistor R4777 to the AC/DC switch K4701, which is controlled by a reed relay in the collector of transistor V4748.
The a.c. path is via C4742 and C4743 in series (two series capacitors to reduce leakage). Reversed diodes V4732, V4733 to earth provide input protection. With EXT TRIG selected, FET V4734 is off and FET V4736 is on. The 1.f. or d.c. signals are therefore fed via V4736 to pin 2 of operational amplifier N4701, together with the feedback signal from the output via R4761, R4783 and C4748 in the x0,2 position; also via R4784//R4785 and C4749 in x0,02 position as V4737 and V4738 are conducting (diode V4746 blocked by logic high from N4702/1).The output on pin 6 of the operational amplifier N4701 is applied via the base of buffer amplifier V4713 to the summation amplifier V4711/V4709. Here, the h.f. signal and 1.f. signals recombine. This recombined input signal is applied to V4717 and emitter follower V4718 which together form the low-impedance output driver stage. This driver stage feeds the TRIGGER SELECTION circuit on the vertical signal unit via a coaxial cable.

When LINE TRIG is selected, the EXT TRIG is inhibited by the LINE control signal LNTR applied to inputs 9 and 12 of operational amplifiers N4702:

- The output N4702-8 cuts off the h.f. path FETs V4701 and V4706 via switching diodes V4729. This output also switches off the 1.f. path FET V4736 via diode V4744.
  Transistor V4714 (switched on in LINE trigger mode) ensures that the circuit d.c. balance is maintained by taking over the current from the switching diodes V4704.
- The output N4702-14 switches on FET V4734 to short circuit the 1.f. signal to earth via diode V4743. Output N4702-14 also switches on FET V4739 to provide a LINE TRIG signal path via its source, V4738 and R4783 to the output. A parallel path is also provided via R4784//R4785.

The source-drain capacitance of FET V4738 (switched off in the x0,2 position) is prevented from giving cross-talk by the circuit V4742 and FET V4741. In the x0,2 position, a -14 V output on N4702-1 turns on V4742 and thus FET V4741, which clamps the drain to earth.

8.31.3 Circuit description of the EVENTS/EXT CLOCK input (see figure 8.31.3.)

The EVENTS/EXT CLOCK input unit is almost identical to the EXT TRIG input unit except that there is a trigger event level input (TREVLV) and no LINE TRIG input. There are two different attenuator positions, x0,2 and x0,02 (only the x0,2 (:5) is used). Consequently, the input socket is coupled to two h.f. paths and one 1.f. path. The two h.f. paths have no input switching with reed-relays.

The x0,2 attenuator consists of the capacitive network C4801, R4801, R4802, C4802 in the gate circuit of FET V4801.

A logic low control signal TREV/5 on the base of V4828 causes this transistor to conduct, which turns on source-follower FET V4801. In turn, V4803 conducts and the signal is passed via diode V4804 to the summation amplifier V4809, V4811.
The logic low control signal TREV/5 is also applied to a switching network, V4819, V4821, V4822, which provides the collector load via diode V4827 for V4809 in the x0,2 position. The x0,2 gain adjust is R4851. The x0,02 attenuator consists of a double capacitive network C4807, R4808, R4809, C4808, and R4811, C4809, R4812, C4811 in the gate circuit of FET V4806. The control and switching circuits (V4831, V4826, V4824, V4823) are identical to the x0,2 position. When the x0,02 position is selected, the gain adjustment in the colllector load of V4809 is then R4853.

The 1.f. path is connected via resistor R4877 to the negative input of comparator N4801-2.
Reversed diodes V4832, V4833 to earth provide input protection. The 1.f. or d.c. signals are fed to pin 2 of operational amplifier N4801, together with the trigger event level signal (TREVLV) coming from the management unit A25 and together with the feedback signal from the output via R4861, R4883 and C4848 in the x0,2 position; also via R4884//R4885 and C4849 in position x0,02 as V4837 and V4838 are conducting (diode V4846 blocked by logic high from N4702-7). The output on pin 6 of the operational amplifier N4801 is applied via the base of buffer amplifier V4813 to the summation amplifier. Here, the h.f. signal and 1.f. signals recombine.

This reconstituted input signal is applied to V4817 and emitter follower V4818 which together form the low-impedance output driver stage.
The output signal EVSGIN is routed via a 50-Ohm coaxial cable to the input of the event counter on the CCD LOGIC UNIT A26.
The source-drain capacitance of FET V4838 (switched off in the x0,2 position) is prevented from giving cross-talk by the circuit V4842 and FET V4841. In the x0,2 position, a -14 V output on N4702-7 turns on V4842 and thus FET V4841, which clamps the drain to earth.

8.31.4 Signal name list

UNIT A31

Signal name	Description	Signal source	Signal destination(s)
ETSGIN	External trigger signal in	A31	A32
ETTR/5	External triggering /5	A25	-
ETTR/5Ø	External triggering /5Ø	A25	-
EVSGIN	Events signal in	A31	A32
LN	Line trigger	A20	-
LNTR	Line triggering	A25	-
TRACDC	Trigger AC or DC	A25	-
TREVLV	Trigger event level	A25	-
TREV/5	Trigger event /5	A25	-
TREV/5Ø	Trigger event /5Ø	A25	-

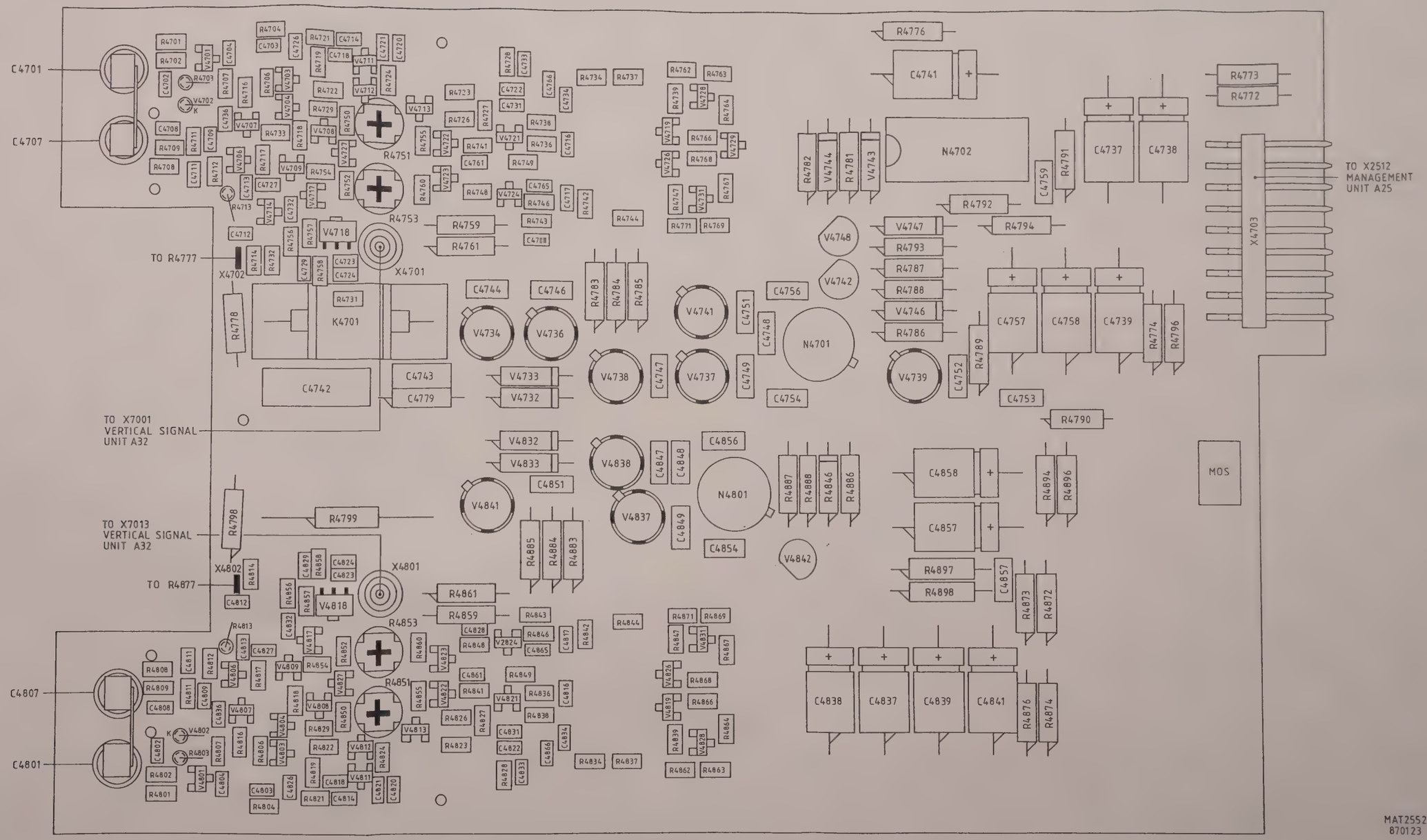


Figure 8.31.1 Unit A31 - EXT TRIG and EVENTS/EXT CLOCK INPUT - p.c.b. lay-out.

EXT.TRIG. INPUT

CAPACITIVE ATT.

LF+DC

AC/DC

COMPARATOR

SUMMATION AMPLIFIER

LF RESPONSE (EXT)

HF RESPONSE (EXT : 10)

TYPE	MARKING CODE
BAV70	A4
BAW56	A1
BCW30	C2
BCW30R	C5
BCW33	U3
BCW33R	D6
BF512	S8
BFQ19	FF
BFR92	P1
BFR92R	P4
BFT92R	W4

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Figure 8.31.2 Unit A31 - EXT TRIG INPUT - circuit diagram.

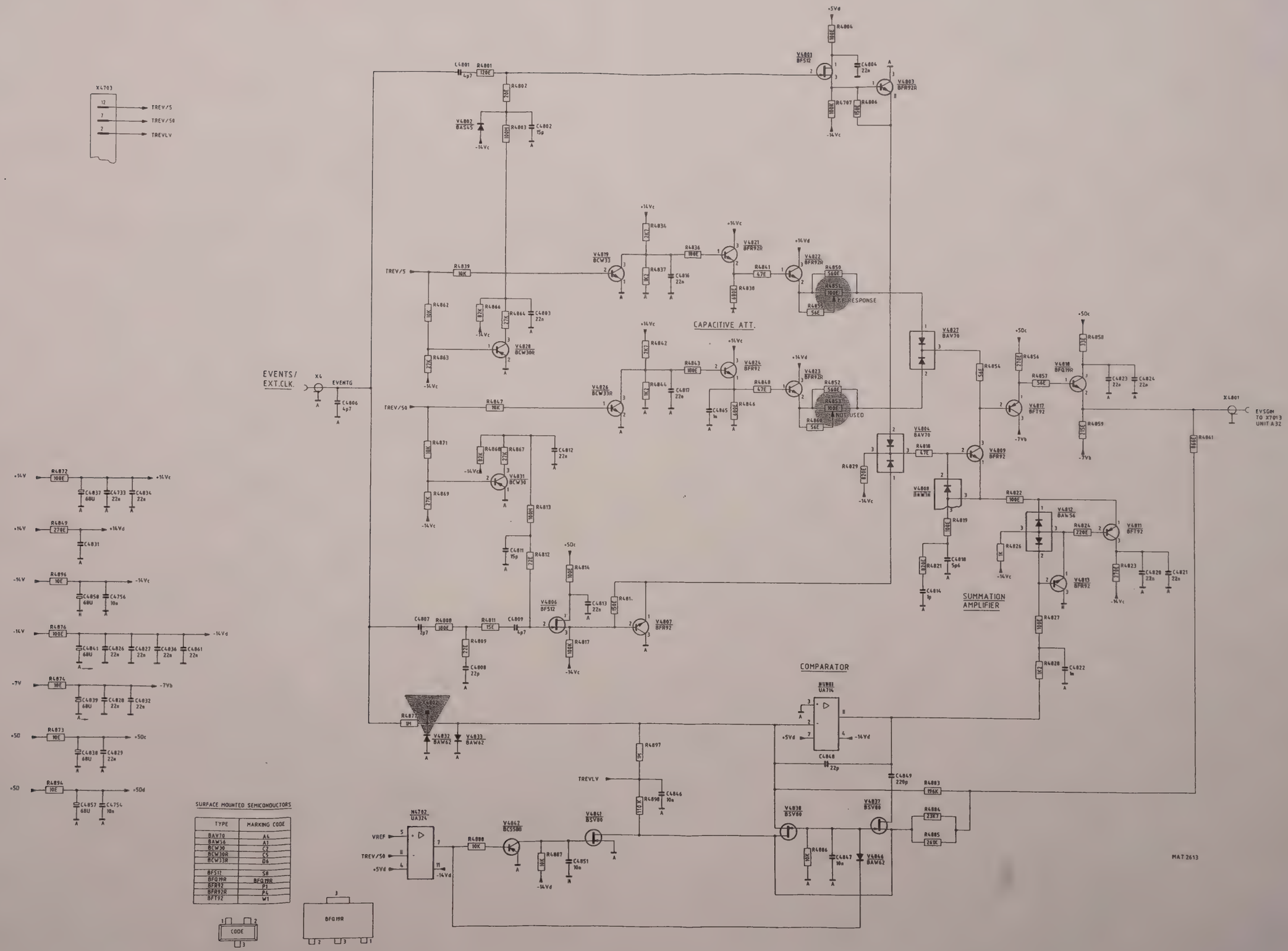


Figure 8.31.3 Unit A31 - EVENTS/EXT CLOCK INPUT - circuit diagram.

Dual trigger mode: (see also fig. 8.32.2)

The input conditions: - TRTVMO module pin 7 is high
- TRDUMO module pin 6 is high

Output D7352 pin 4 is low, so the input signal applied to the Schmitt-trigger D7351-3-6 is active on input 18 of D7352.
Output D7352 pin 6 is also low, so the input signal applied to the Schmitt-trigger D7351-17-16 that is routed via the delay line (between module pins 11 and 14) is active on input 17 of D7352 (EX-OR).
If both inputs are low or high the output pin 16 will be low. Because of the delay of 3,5 ns the pulses applied to D7352-17 are shifted in time with respect to the pulses on D7352-18.
The minimum shift is 3,5 ns. This minimum delay is necessary to compensate propagation delays.
The result is an output signal TRSG on D7352 pin 16 that is routed via module pin 9 to unit A49 module pin 2.
If the LEVEL in dual mode is turned the signal will be vertically shifted as given in the right part of fig. 8.32.2.
This vertical shift results in another pulse width of the signal TRSG. This results in other trigger level points on the signal.

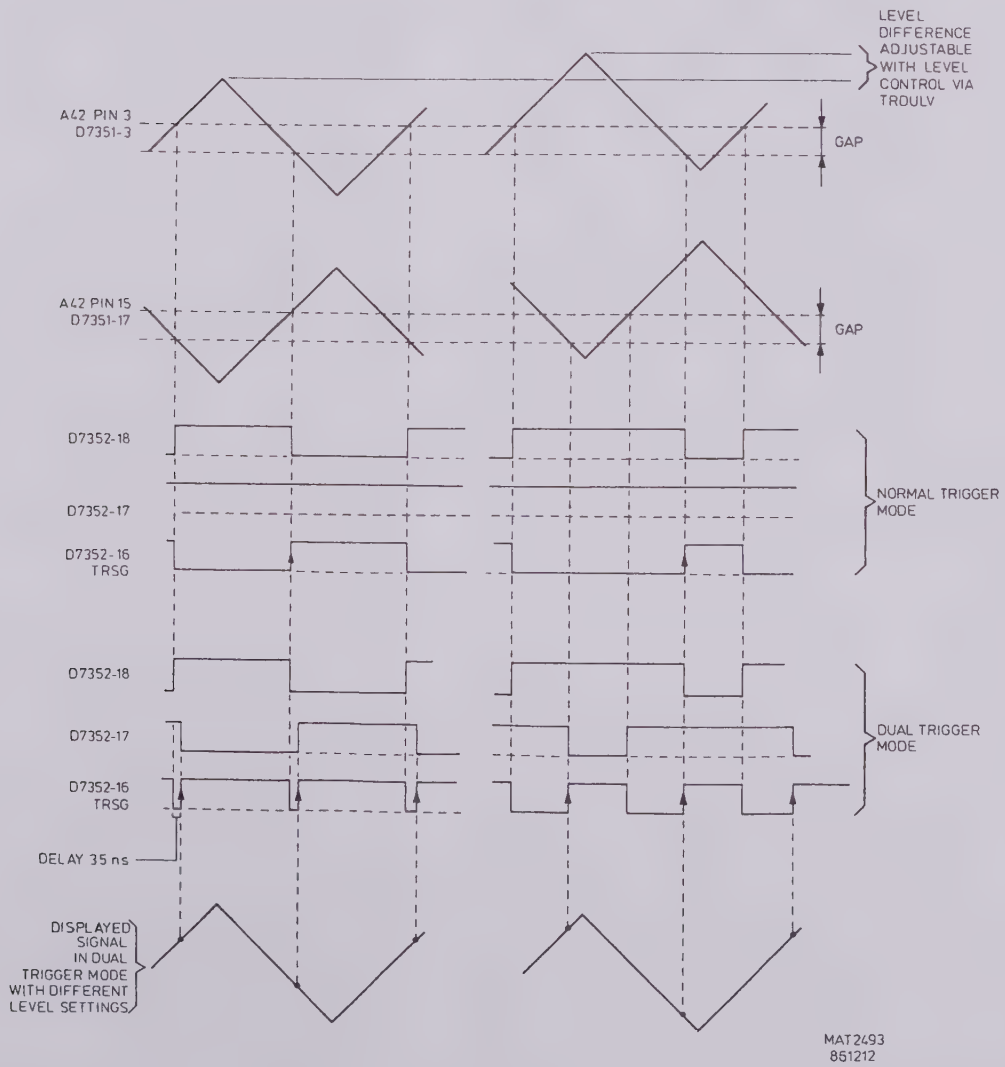


Fig. 8.32.2 Trigger logic levels

TV trigger mode:

The input conditions: - TRTVMO module pin 7 is low
- TRDUMO module pin 6 is low

In this mode the signals applied to the inputs 18 and 17 of EX-OR port D7352 are blocked, because both inputs are constantly high.
This makes output D7352 pin 16 low.
The TV sync. trigger pulse (coming from the TV sync. separator via module pin 17) are routed to module pin 9 (as TRSG) via Schmitt-trigger D7351-19-14.

8.32.8 The TV sync. separator circuit

This circuit consists of V7027...V7032 and D7003.
The input signal is derived from the TRIGGER AMPLIFIER unit A41 (module pin 22).
The trigger signal is applied via a video clipper circuit consisting of V7028/V7029 to two re-triggerable monostable one-shots in series (D7003).
These two monostable one-shots have different pulse times determined by the RC networks on pins 14 and 15 and pins 6 and 7.
The output of the first one-shot (pin 4) is applied to the clock input of D-flip flop D7004 pin 11.
This flip-flop is enabled by the TV signal.
At the output pin 9 of D7004 a 50 Hz field pulse is available.
To obtain frame pulses the inverting output D7004 pin 8 is applied to the clock input D7004 pin 3.
At the D input D7004 pin 2 the output of the second one-shot is applied.
The frame pulses now appear at the output D7004 pin 5.
The frame and field pulses are combined in the output stage V7031/V7032.
The combined field and frame pulses are fed as TV trigger pulses to the TRIGGER LOGIC unit A42 module pin 17.
To inhibit the TV trigger signals in other modes than TV mode the control signal TRTVMO is applied to the set inputs of the D-flip-flops D7004.
In TV mode this control signal is high.

8.32.7 The EVENTS AMPLIFIER unit A43 and TRIGGER LOGIC unit A42

* EVENTS AMPLIFIER unit A43

On this module the EVENTS signals coming from the EVENTS/EXT CLOCK input via A31 are converted into symmetrical signals to control the slope, the trigger symmetry and the trigger gap.
The output is a asymmetrical signal which is fed to the TRIGGER LOGIC unit A42 (module pin 1).
The integrated circuit D7401 makes the slope selection possible controlled by the signal TREVSP applied to module pin 3.
If TREVSP is high the signal path via D7401-pin 14 and 15 is open and if TREVSP is low the signal is routed via D7401 pins 16 and 17.
In this way the symmetrical signal can be inverted.
This selected signal is applied to the symmetrical amplifier consisting of four transistors in one housing D7402.
The input currents applied to the bases of D7402 pins 4 and 15 are in antiphase and are applied to the output via transistor V7401 and V7402 to the asymmetrical output. The function of V7401 and V7402 is to adapt the output level.
The currents coming out of the collectors of V7401 and V7402 are fed to the circuit V7403/V7404 and are substracted in this circuit.
The result is that the common current components are eliminated and only the current variations (signal) are fed to the output module pin 8.
On output module pin 8 a resistor divider network adjustable with R7159 is present. The function of this R7159 is to adjust the voltage output level of the EVENTS signals. This voltage EVENTS signal is fed to pin 1 of A42.

* TRIGGER LOGIC unit A42

This unit consists of logic circuits and Schmitt-trigger circuits to control the various trigger modes.
The symmetrical input trigger signals coming from the TRIGGER AMPLIFIER A41 are applied to module pins 15 and 3.
The control signals TRTVMO (pin 7) and TRDUMO (pin 6) are selecting the trigger signals for respectively the TV mode and the DUAL TRIGGER mode.
The TV sync. trigger is applied to module pin 17.

The EVENTS signals coming from the EVENTS AMPLIFIER unit A43 are applied to module pin 1.
These EVENTS signals are fed via a Schmitt trigger circuit D7351 pins 23-24-11-12 to output module pin 13.
The signal EVSG-HE is routed to the EVENTS COUNTER on the CCD LOGIC unit A26.

The selectable trigger modes are now separately described.

Normal trigger mode: (see also fig. 8.32.2)

The input conditions: - TRTVMO module pin 7 is high
- TRDUMO module pin 6 is low

The input signal applied to module pin 3 is routed via Schmitt-trigger D7351 pins 3 and 6 to EX-OR port D7352 pin 18. Input D7352 pin 17 is high in this mode (via EX-OR D7352 pin 6). The output D7352 pin 16 is as indicated in fig. 8.32.2 (the inverted signal of input pin 18).
If the level is changed (right part of fig. 8.32.2) the pulse width of TRSG will be influenced. This output signal TRSG is fed via module pin 9 to unit A49 (pin 2) for aliasing detection and start acquisition.

8.32.6 The Auto Offset Level Detection circuit.

In this circuit the peak-peak detection for the level range and the auto offset detection is done.
The input trigger signal for this circuit is derived from the TRIGGER AMPLIFIER unit A41.
The current sources V7018 and V7019 feed the input stage V7012/V7013.
To make the current sources V7018 and V7019 equal a comparator N7001 is present inbetween.
Integrated circuit D7002 (OQ 0128) is a peak detector circuit which detects, if AUTO TRIG is selected, the amplitude of the trigger signal.
If AC or DC triggering is selected (AUTO off) the peak-peak detection is not used and the level range is not determined by the peak-peak value of the trigger signal.
Only the control signal TRLV (trigger level) applied to D7002 pin 1, coming from the LEVEL control via the management unit A25 is determining the dc level of the trigger signal.
The trigger signal is shifted by control signal TRLV on D7002-1: a control range of 0 V...5 V gives a level shift range of -10...+10 div. (full level range).
If AUTO triggering is selected the control signal AULV applied to D7002 pin 13 is high and the peak-peak detector is active.
The dc level of the trigger signal is now determined by the control signal TRLV and the peak-peak value of the trigger signal. The AUTO TRIGGER LEVEL can be adjusted with R7044 via D7002 pin 5.
If AUTO OFFSET is active, the control signal AULV is high and TRLV is fixed on +2,5 V.
The dc level of the trigger signal is now only determined by its own dc component.
This dc component is fed via comparator N7003 pin 7 and 8 to the management unit A25 as control signal AOLD (Auto Offset Level Detection).
The level of AOLD can be adjusted with R7052

The uP reads this signal AOLD and adapts the dc offset in the attenuator.
After that, the signal AOLD is read again and the dc offset is corrected again etc.. up to the moment that AOLD has a correct value.
Repeating the correction sequence is necessary because the range of the ADC is ±10 div. and the offset range on screen is ± 100 div.
If the auto d.c. offset is correct, the signal AULV will become low again and TRLV stays on 2,5 V level.
In AUTO OFFSET mode, the SHIFT is set to the middle of the screen (0 V). The minimum reaction time of the OQ 0128 circuit (D7002) is 0,1 sec., so the AUTO OFFSET will not function correctly for signals with a lower repetition time.
The dc shifted trigger signals are fed to the symmetrical output stage V7023/V7024 where the TRIGGER SYMmetry can be adjusted with R7129 which is connected between the collectors of V7023/V7024.
The slider of R7129 is controlled by the signals OSTRDU and AULV via inverter N7003 and V7039.
If in AUTO, AUTO OFFSET and DUAL TRIGGER mode these signals are high, the low output D7003-14 will switch on V7039 to supply the slider of R7129.
Via dual transistor V7026 the symmetrical output is fed to the TRIGGER AMPLIFIER unit A44 for level control.
In this stage the symmetry can be adjusted with R7084. The current sources for V7026 are V7021 and V7022 and they are compared by comparator N7001.

Via the symmetrical output stage V7002 the selected trigger signals are fed to module A40 pins 14 and 15.
On unit A40 they are recombined with the signals coming from D7202 pins 16 and 17.
The current sources for the output stage V7204/V7206 are V7007 and V7008.
They are compared by comparator N7001 and can be balanced by potentiometer R7036 (in AUTO trigger mode).
The slider of the AUTO-DC jump potentiometer R7036 is connected with the -14 V via transistor V7011, which on its turn is controlled by signal AULV which is high in AUTO trigger mode.
The selected triggersignal range is fed to the TRIGGER AMPLIFIER unit A41 via V7204/V7206.

* TRIGGER AMPLIFIER unit A41

The symmetrical trigger signals are applied to module pins 4 and 12 and fed to D7251 pins 2 and 9.
The trigger signals are picked off via D7251 pins 1 and 10 and fed to the AUTO OFFSET LEVEL DETECTION circuit D7002 and accosiated circuitry.
The output signal of this circuit is fed back to the input of the TRIGGER AMPLIFIER D7251 pins 5 and 6 (module A41 pins 7 and 9) for AUTO LEVEL control.
The dc levels coming from the AUTO OFFSET LEVEL DETECTION circuit are controlling the level of the input trigger signal applied to D7251.
In D7251 the trigger slope can be selected by means of control signal TRSP. The output signal can be routed via output D7251 pins 16 and 17 (negative slope; TRSP--LX is low) or 14 and 15 (positive slope; TRSP--LX is high) to the inputs of the dual trigger circuits.
The current triggersignals are applied to the bases of transistorpairs D7252 and D7253.
On the bases of these transistors also DC levels are applied coming from the dual transistor V7034.
The positive level is applied to D7252 and the negative level to D7253.
In this way both levels are determined in dual trigger mode.
The positive and negative levels are both activated by control signal TRDUMO applied to the base of V7038 which activates current source V7037.
This current source drives the dual transistor V7034.
One base of the double transistor V7034 is connected to the positive input of comparator N7003 via a voltage divider network with potentiometer R7116 which determines the trigger gap between positive and negative triggering.
The other base of V7034 is connected with the output of comparator N7003 via which the level in dual trigger mode is determined.
Transistors V7251 and V7252 together with V7253 convert the symmetrical positive slope trigger signal into an asymmetrical voltage signal which is fed to the TRIGGER LOGIC via module pin 24.
The same is done for the other half of the circuitry by V7257/V7258 and V7259 via module pin 18.
The trigger signal used for the TV SYNC SEPARATOR is derived from V7252 via V7254 and is routed to this circuit via module pin 22.

LF filter and DC selection (D7001)

The trigger signal from the summation amplifier V7201/V7202 is also fed to D7001 pins 5 and 6.
In D7001 three symmetrical signal paths can be selected by two control signals ACTRCOHX and DCTRCOHX applied to respectively D7001 pins 10 and 9.
In fig. 8.32.1 is indicated which filter is selected with these control signals.
When DC is selected the trigger signal is routed via the outputs D7001 pins 18 and 11, when AC is selected via D7001 pins 17 and 12 via capacitors C7002 and C7003.
The trigger signals are blocked when the control signal HFTRCOHX is high and DCTRCOHX and ACTRCOHX are low and then the outputs D7001 pins 16 and 13 are short circuited (see fig. 8.32.1).
These control signals are coming from three level adapters N7002 pins 8, 14 and 7.
These three level adapters are adapting the TTL input signal to analog values: high on the input gives +7 V on the output and low on the input gives -7 V on the output

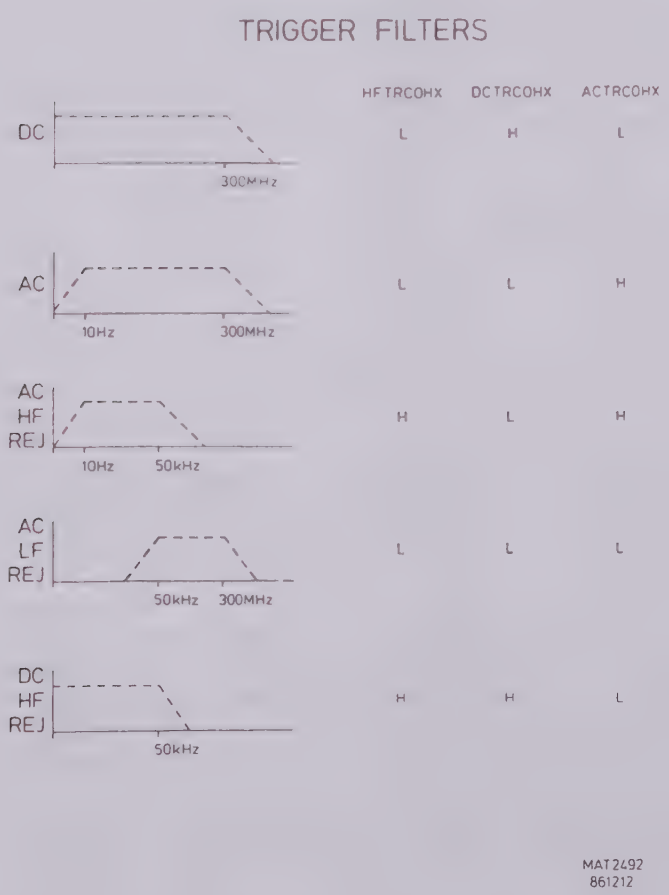


Fig. 8.32.1 Trigger Filters

8.32.4 The TRIGGER SELECTOR unit A38 (A39)

On this module A38 (A39) the trigger source channel A(B) is selected and the AC-DC balance is corrected.
The module of channel A and B is identical, so only A is described.
The symmetrical trigger pick-off signal is coming from the channel A preamplifier D5002 and is applied via module pins 2 and 5 to D5301 pins 2 and 9.
The circuitry in D5301 is symmetrical and can be balanced with potentiomter R5030 (AC-DC balance) via module pin 1.
One half of the double symmetrical output is not used and connected to the supply voltage.
The other half can be switched on and off by the control signal TRSOA- applied to module pin 7, coming from the management unit A25.
The output signal is routed to the TRIGGER FILTER unit A40.

8.32.5 The TRIGGER FILTERS and TRIGGER AMPLIFIER (units A40 and A41)

* TRIGGER FILTERS

The module A40 consists of an input circuit for the EXT TRIGGER signals (ETSGIN) and a trigger summation stage and a switch circuit for an HF filter.
The input circuit for the EXT TRIGGER signal is the same as for A and B signals on unit A38 and A39 only the input signal is asymmetrical applied to module pin 1 (coming from unit A31).
This asymmetrical input signal is converted into a symmetrical output signal, which can be selected with the control signal ETTR applied to module pin 3.
The input of the symmetrical summation stage consisting of V7201 and V7202 can be derived from channel A (module pins 5 and 21) channel B (module pins 6 and 22) or EXT TRIG (D7201 pins 14 and 15) whichever is selected.

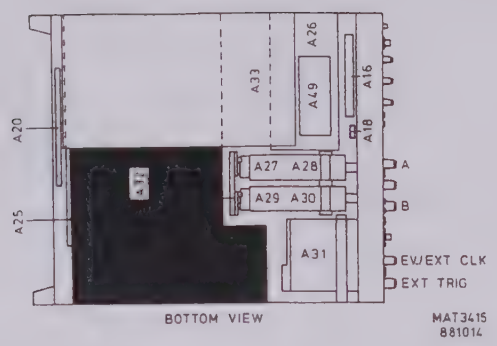
The current sources for the transistors V7201/V7202 are V7003 and V7004 applied via module pins 8 and 9.
Both current sources are compared with comparator N7001. The balance of the current sources for AC-DC jump correction can be adjusted with R7022 connected between the collectors of V7003 and V7004.
The output of V7201/ V7202 is split up into two pathes:

- via module pins 17 and 18 to D7001 pins 5 and 6 on unit A32 for AC/DC filter selection and to input pins 5 and 6 of D7202 for HF filter selection

  HF filter selection (D7202)

  Integrated circuit D7202 selects one of the two signal pathes control by signal HFTRCOHX.
  When this control signal is high the HF filter formed by C7212, R7246 and R7247 is switched into the signal path via output pins 14 and 15 (HF REJ on).
  The HF REJ jump can be adjusted with R7019 via module pin 19.
  When sigal HFTRCOHX is low the HF filter is switched off and the full trigger bandwidth is available (see fig. 8.32.1).
  Via the output stage V7204/V7206, where it is combined with the trigger signals coming from D7001, the trigger signal is fed to the TRIGGER AMPLIFIER.

UNIT A32 - VERTICAL SIGNAL UNIT



CONTENTS

8.32.1	General information	8.32-1
8.32.2	Channels A and B pre-amplifiers	8.32-2
8.32.3	The VERTICAL AMPLIFIER PROCESSOR unit	8.32-3
8.32.4	The TRIGGER SELECTOR unit A38	8.32-4
8.32.5	The TRIGGER FILTERS (unit A40) and TRIGGER AMPLIFIER (A41)	8.32-4
8.32.6	The Auto Offset Level Detection circuit	8.32-7
8.32.7	The EVENTS AMPLIFIER unit A43 and TRIGGER LOGIC unit A42	8.32-8
8.32.8	TV sync separator circuit	8.32-10
8.32.9	Signal name list	8.32-11

8.32.1 General information

In this section also the mini units A38...A44 are described.
The Vertical Signal unit A32 is connected between the outputs of the attenuators, trigger input circuits and the Signal acquisition part (P^2CCD unit A33)
The circuits are divided over three diagrams:

- diagram 8.32.2: - channels A and B pre-amplifiers
  - channel selection (unit A44)
  - trigger pick-offs A and B
- diagram 8.32.3: - trigger selection and filters (unit A40)
  - auto offset level detection circuit
- diagram 8.32.4: - trigger amplifier (unit A41)
  - events amplifier (unit A43)
  - trigger logic (unit A42)
  - t.v. sync. separator circuit

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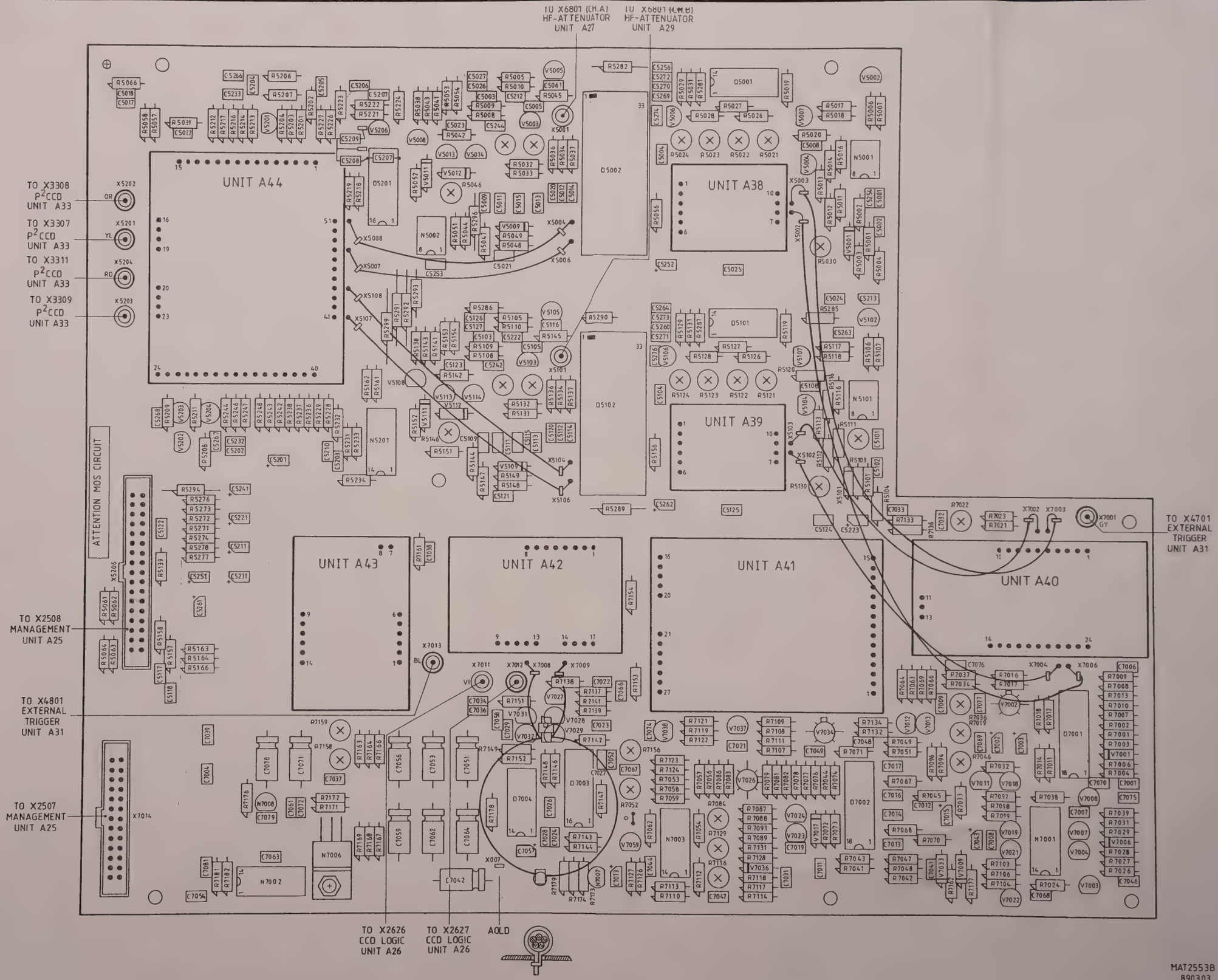


Figure 8.32.3 Unit A32 - VERTICAL SIGNAL - p.c.b. lay-out.

8.32.9 Signal name list unit A32 (including units A38...A43)

Signal name	Description	Signal source	Signal destination(s)
ACTRCO	AC trigger coupling	A25	-
ACTRCOHX	AC trigger coupling	A32	A32
AOLD	Auto offset level detection	- A32	- A25
AULV	Auto level	A25	-
A+B---HT	Add-mode	A25	-
A+B---LT	Add-mode	A25	-
BWL---HT	Bandwidth limiter	A25	-
BWL---LT	Bandwidth limiter	A25	-
DCTRCO	DC trigger coupling	A25	-
DCTRCOHX	DC trigger coupling	A32	A32
ETTR	External triggering	A25	-
ETSGIN	External trigger signal in	A31	-
EVSGIN	Events signal input	A31	-
EVSG--HE	Events signal	A32	A26
HFTRCO	HF trigger control	A25	-
HFTRCOHX	HF trigger control	A32	A32
IVA	Invert A	A25	-
IVB	Invert B	A25	-
NOA-	Normal A	A25	-
NOB-	Normal B	A25	-
OSTRDU	Offset dual triggering	A32	A32
PA/1A	Pre-amplifier /1 A	A25	-
PA/1B	Pre-amplifier /1 B	A25	-
PA/2A	Pre-amplifier /2 A	A25	-
PA/2B	Pre-amplifier /2 B	A25	-
PA2,5AHT	Pre-amplifier x 2,5 A	A25	-
PA2,5BHT	Pre-amplifier x 2,5 B	A25	-
PA2,5ALT	Pre-amplifier x 2,5 A	A25	-
PA2,5BLT	Pre-amplifier x 2,5 B	A25	-
PA/4A	Pre-amplifier x 4 A	A25	-
PA/4B	Pre-amplifier x 4 B	A25	-
SHA	Shift A	A25	-
SHB	Shift B	A25	-
SWINAN	Signal switch input A N	A32	A33
SWINAP	Signal switch input A P	A32	A33
SWINBN	Signal switch input B N	A32	A33
SWINBP	Signal switch input B P	A32	A33
TRDULV	Trigger dual level	A25	-
TRDUMO	Trigger dual mode	A25	-
TREVSP	Trigger events slope	A25	-
TRLV	Trigger level	A25	-
TRSG	Trigger signal	A32	A26-A49
TRSOA	Trigger source A	A25	-
TRSOB	Trigger source B	A25	-
TRSP	Trigger slope	A25	-
TRSP--LX	Trigger slope	A25	A32
TRTVMO	Trigger TV mode	A25	-
VGA	Variable gain A	A25	-
VGB	Variable gain B	A25	-

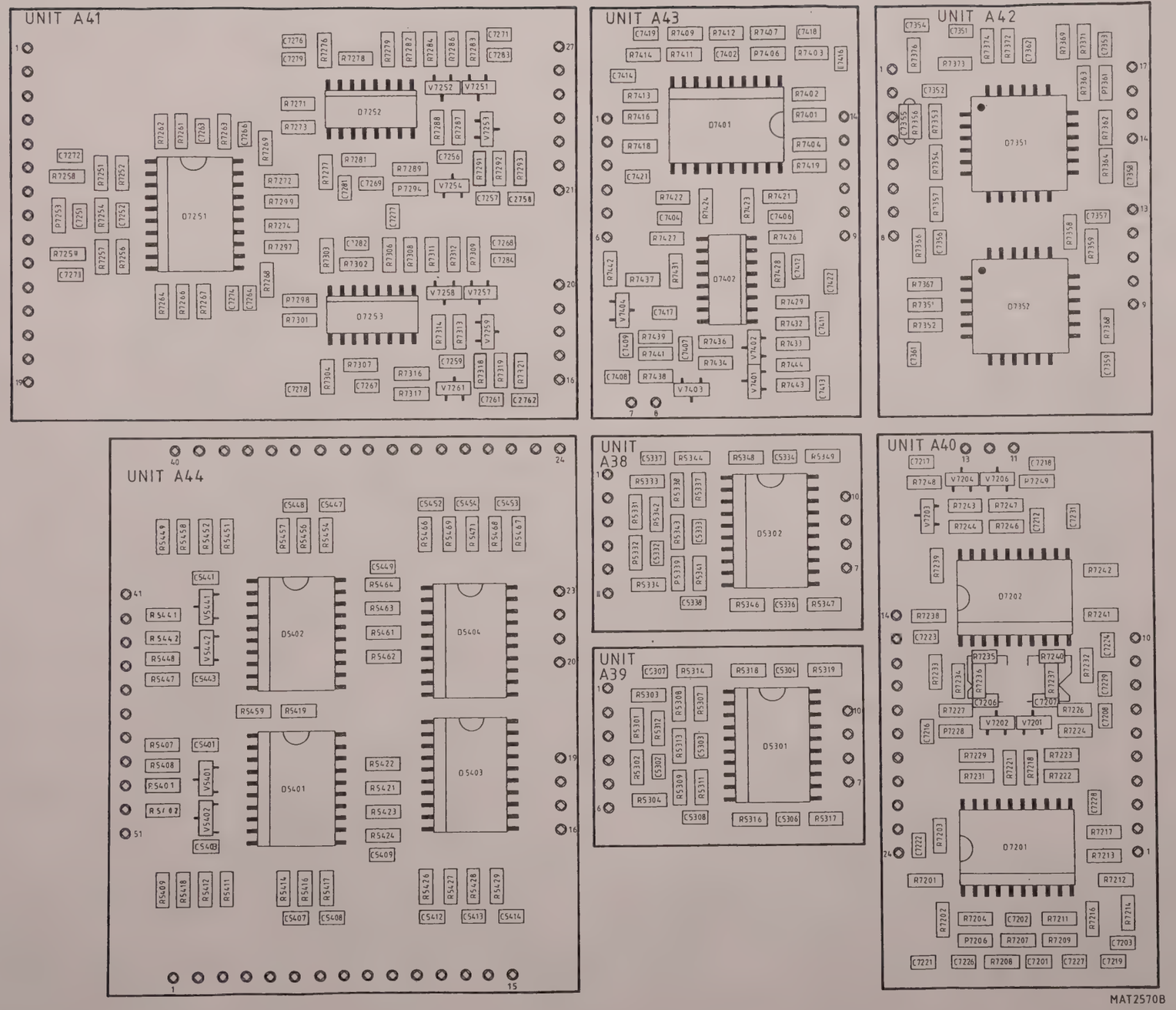


Figure 8.32.4 Unit A32 - VERTICAL SIGNAL - p.c.b. lay-out.

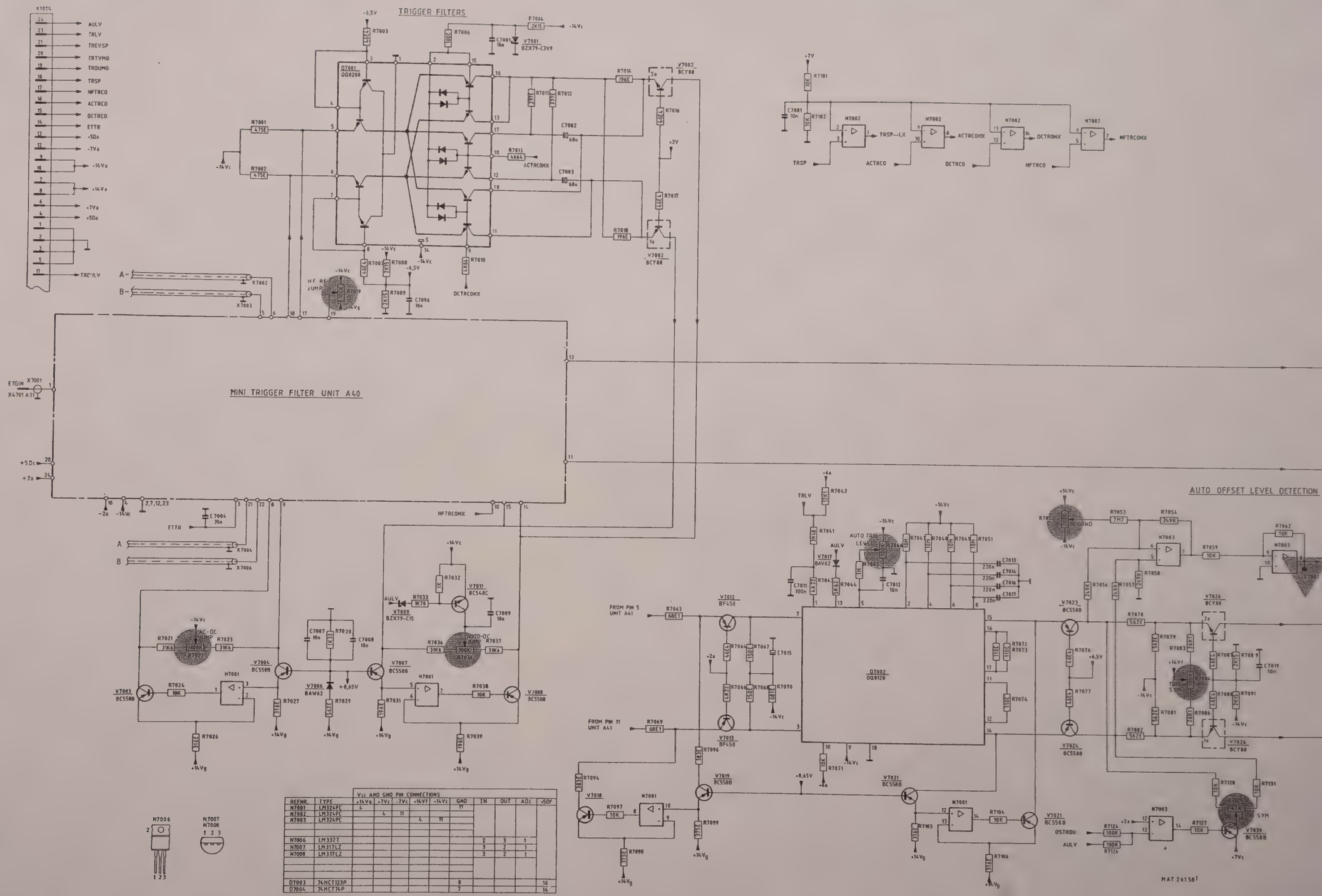


Figure 8.32.8 Unit A32 - VERTICAL SIGNAL - circuit diagram.

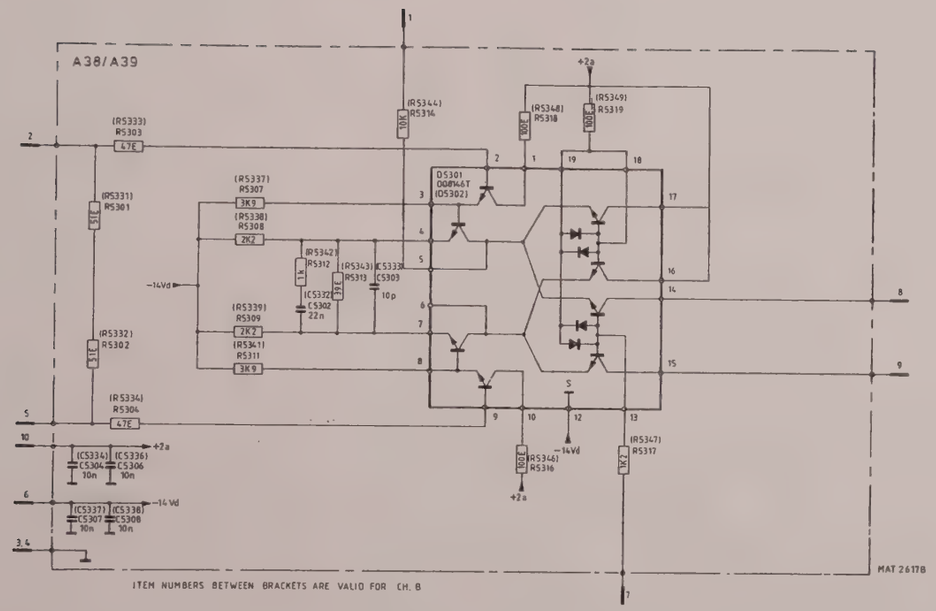


Figure 8.32.6 Unit A32 - VERTICAL SIGNAL - circuit diagram.

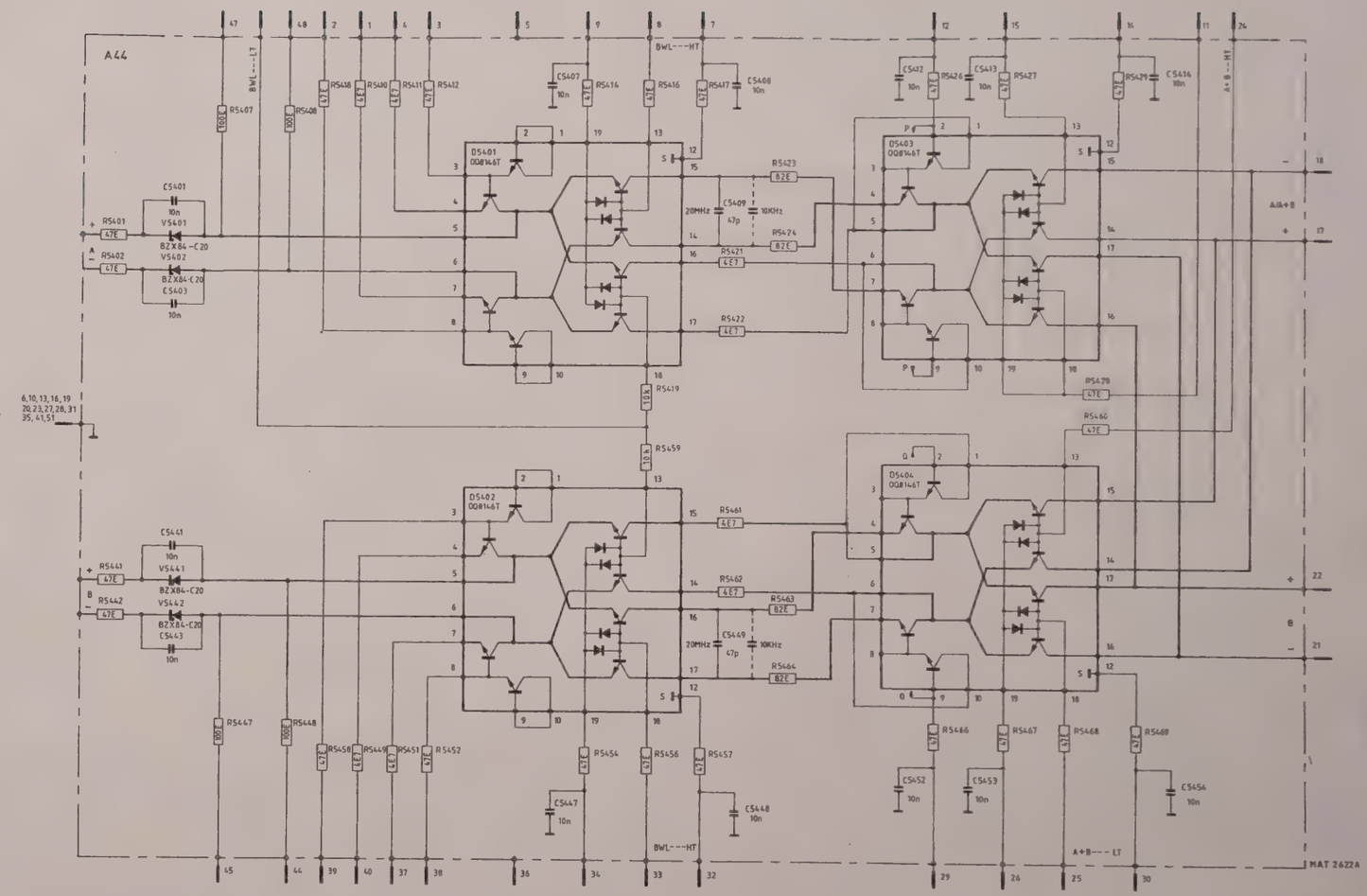
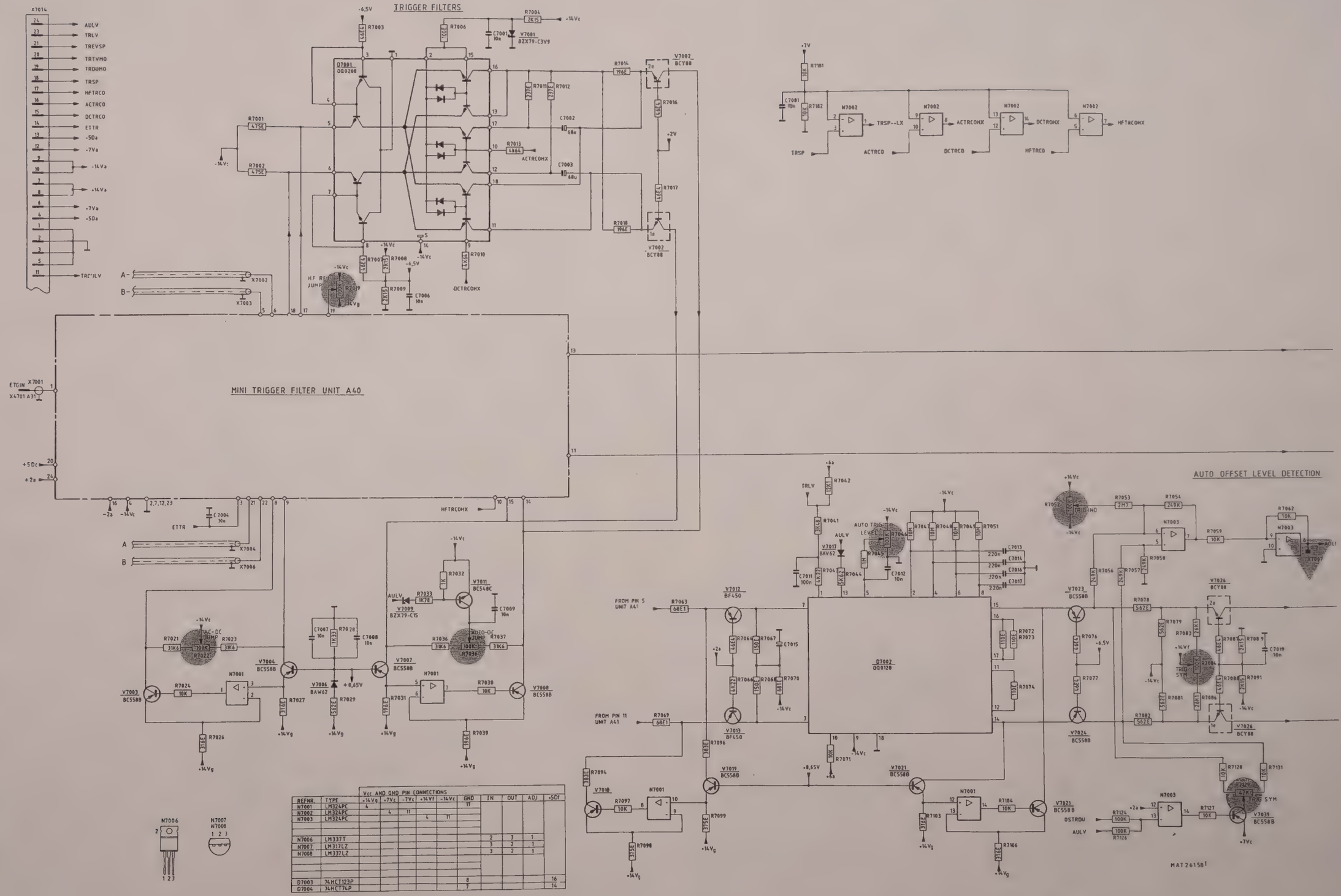


Figure 8.32.7 Unit A32 - VERTICAL SIGNAL - circuit diagram.



REFNR.	TYPE	Vcc AND GND PIN CONNECTIONS +14Vg	+7Vc	-7Vc	+14Vf	-14Vc	GND	IN	OUT	ADJ	+5Of
N7001	LM324PC	4					11				
N7002	LM324PC		4	11							
N7003	LM324PC				4	11					
N7006	LM337T							2	3	1	
N7007	LM317LZ							3	2	1	
N7008	LM337LZ							3	2	1	
D7003	74HCT123P						8				16
D7004	74HCT74P						7				14

Figure 8.32.8 Unit A32 - VERTICAL SIGNAL - circuit diagram.

Figure 8.32.9 Unit A32 - VERTICAL SIGNAL - circuit diagram

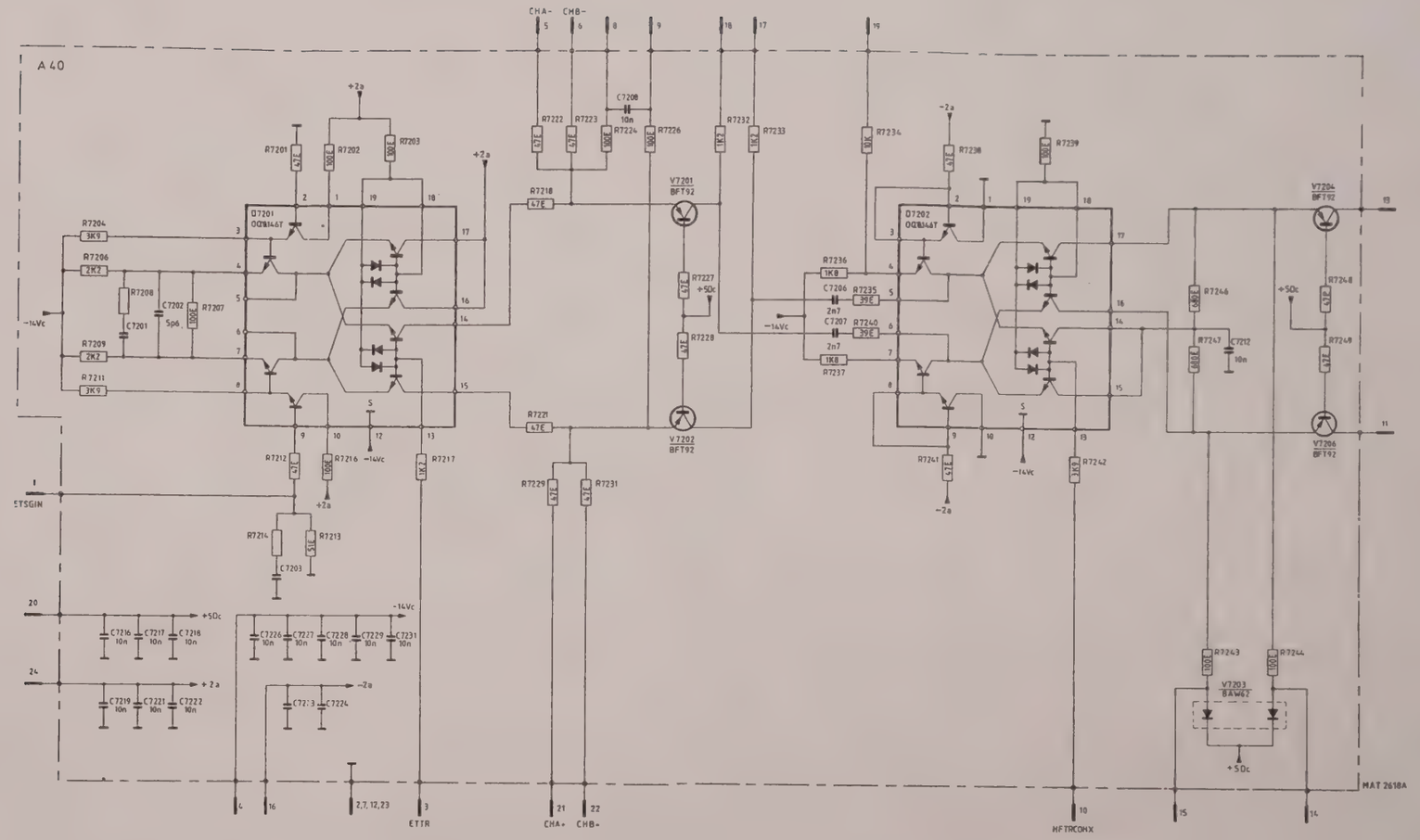


Figure 8.32.10 Unit A32 - VERTICAL SIGNAL - circuit diagram.

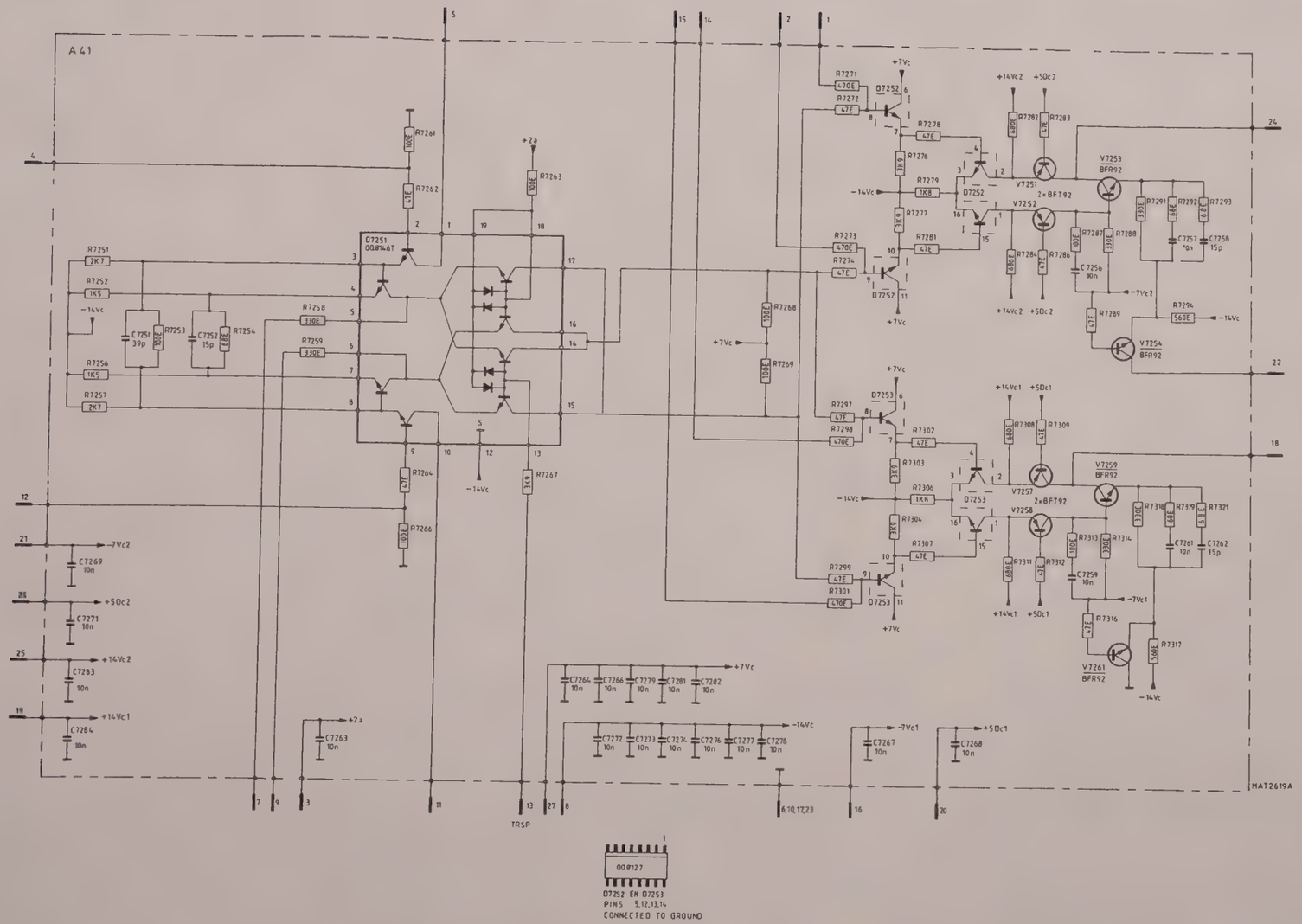


Figure 8.32.11 Unit A32 - VERTICAL SIGNAL - circuit diagram.

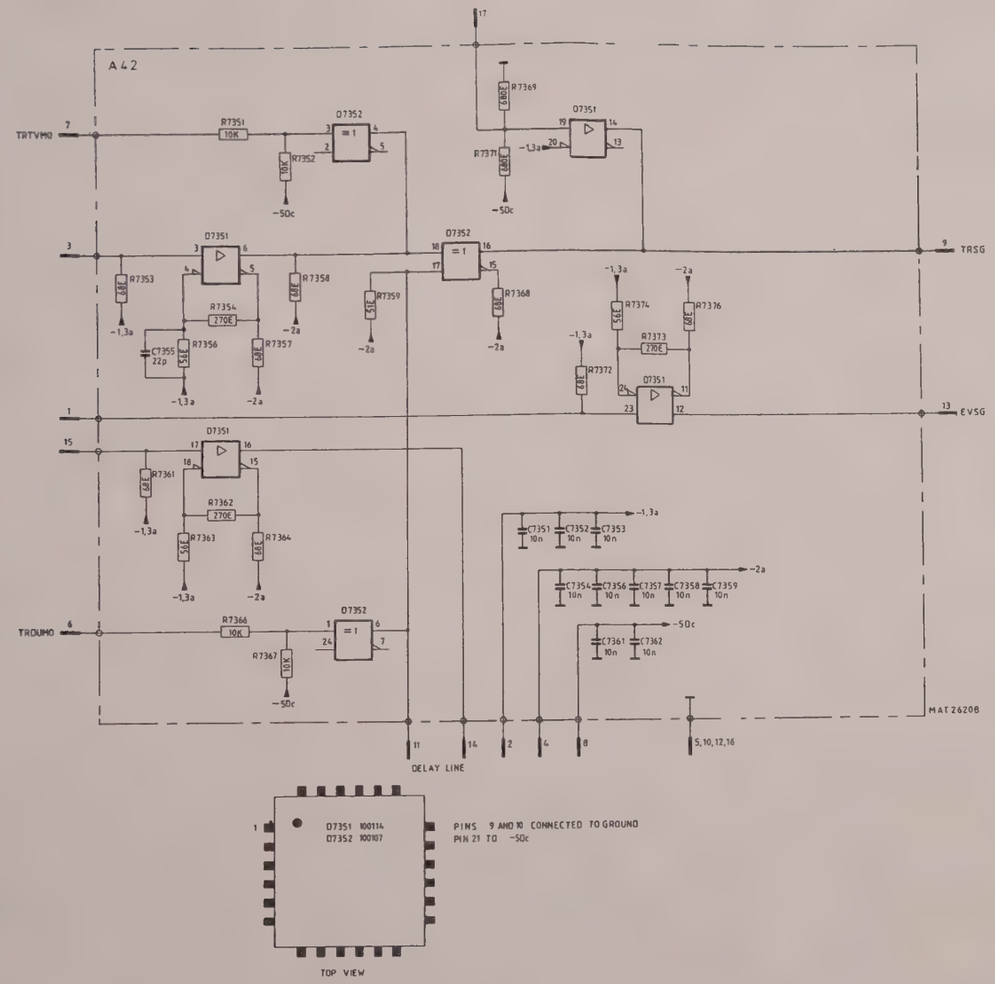


Figure 8.32.12 Unit A32 - VERTICAL SIGNAL - circuit diagram.

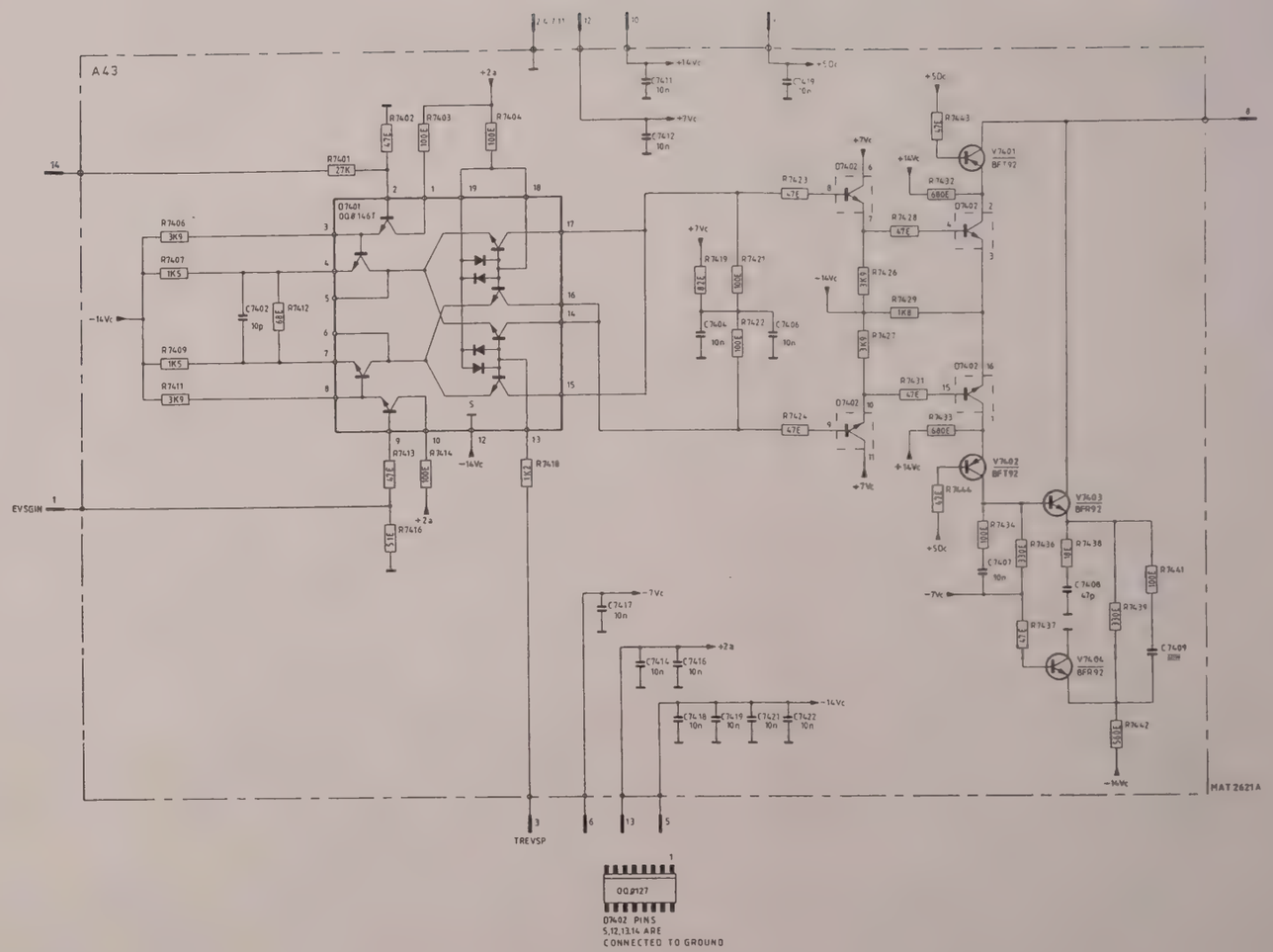


Figure 8.32.13 Unit A32 - VERTICAL SIGNAL - circuit diagram.

Signal name	Description	Signal source	Signal destination(s)
SWCK	Slow clock	A33	A33, A25,A25-A26
SWINAN	Signal switch input A N	A32	-
SWINAP	Singal switch input A P	A32	-
SWINBN	Signal switch input B N	A32	-
SWINBP	Signal switch input B P	A32	-
TCEV-1LT	Transport clock even	A33	A33,A25
TCEV-2LT	Transport clock even	A26	-
TCEVA-HE	Transport clock even A	A26	-
TCEVA-LX	Transport clock even A	A33	A33
TCEVB-HE	Transport clock even B	A26	-
TCEVB-LX	Transport clock even B	A33	A33
TCODA-HE	Transport clock odd A	A26	-
TCODA-LX	Transport clock odd A	A33	A33
TCODB-HE	Transport clock odd B	A26	-
TCODB-LX	Transport clock odd B	A33	A33
THINAN	Track and hold in analogue	A33	A11
TTEVA-LX	Transport clock terminator even A	A33	A33
TTEVB-LX	Transport clock terminator even B	A33	A33
TTEVDALX	Transport clock terminator even delayed A	A33	A33
TTEVDBLX	Transport clock terminator even delayed B	A33	A33
TTODA-LX	Transport clock terminator odd A	A33	A33
TTODB-LX	Transport clock terminator odd B	A33	A33
TTODDALX	Transport clock terminator odd delayed A	A33	A33
TTODDBLX	Transport clock terminator odd delayed B	A33	A33
ZECH	Zero channel	A5	-

Signal name	Description	Signal source	Signal destination(s)
CIHOAE	Clamp integrate hold out A even	A33	A33
CIHOAO	Clamp integrate hold out A odd	A33	A33
CIHOBE	Clamp integrate hold out B even	A33	A33
CIHOBO	Clamp integrate hold out B odd	A33	A33
CKØ1ØØ	Clock 1ØØ kHz	A33	A25-A26
CKØ2ØØ	Clock 2ØØ kHz	A33	A33
CKØ4ØØ	Clock 4ØØ kHz	A33	A33
CKØ8ØØ	Clock 8ØØ kHz	A33	A33
CK16ØØ-1	Clock 1,6 MHz	A25	-
CKCDOC-1	Clock P2CCD output control	A25	-
CLR	Clear	A33	A33
MM	Min/Max mode	A25	-
MMPTØ1	Min/Max pointer Ø1	A33	A33-A25-A12-A5
PDSWØ...PDSW2	Peak detector switch Ø...2	A25	-
PKHA	Peak high frequency A	A33	A33
PKHB	Peak high frequency B	A33	A33
PKLA	Peak low frequency A	A33	A33
PKLB	Peak low frequency B	A33	A33
RSEV--LT	Reset even	A33	A33
RSMNPD	Reset min peak detector	A49	-
RSMXPD	Reset max peak detector	A49	-
RSOD--LT	Reset odd	A33	A33
RVCDG	Refrence voltage P^2CCD gain	A33	A33
SCEV-1HT	Sample clock even	A33	A33,A25
SCEV-2HT	Sample clock even	A26	-
SCEVA-LE	Sample clock even A	A26	-
SCEVB-LE	Sample clock even B	A26	-
SCOCA	Sample clock output control A	A33	A24
SCOCB	Sample clock output control B	A33	A24
SCODA-LE	Sample clock odd A	A26	-
SCODB-LE	Sample clock odd B	A26	-
SSA1...3	Signal switch A 1...3	A33	A33
SSB1...3	Signal switch B 1...3	A33	A33
SSC	Signal switch control	A33	A33
ST1...1Ø	Status 1...1Ø	A33	A33
STCV	Start conversion	A33	A25-A12-A5, A25-A12-A11
STEVA-HX	Sample clock terminator even A	A33	A33
STEVB-HX	Sample clock terminator even B	A33	A33
STODA-HX	Sample clock terminator odd A	A33	A33
STODB-HX	Sample clock terminator odd B	A33	A33

8.33.7 Signal name list

UNIT A33

Signal name	Description	Signal source	Signal destination(s)
A-	Channel A	A25	-
A1...3	Channel A 1...3	A33	A33
A+B--1HT	Add mode 1	A25	-
AO	Channel A odd	A33	A33
ASEVA	Average sample clock Even A	A33	A33
ASEVB	Average sample clock Even B	A33	A33
ASODA	Average sample clock Odd A	A33	A33
ASODB	Average sample clock Odd B	A33	A33
B1...3	Channel B 1...3	A33	A33
CD	P^2CCD mode	A25	-
CDCPEV	P^2CCD clamp even	A33	A33
CDCPOD	P^2CCD clamp odd	A33	A33
CDIGEV	P^2CCD integrate even	A33	A33
CDIGOD	P^2CCD integrate odd	A33	A33
CDINAE	P^2CCD in A even	A33	A33
CDINAO	P^2CCD in A odd	A33	A33
CDINBE	P^2CCD in B even	A33	A33
CDINBO	P^2CCD in B odd	A33	A33
CDOCØØ...Ø3	P^2CCD output control ØØ...Ø3	A25	-
CDOGC1	P^2CCD output gain control 1	A25	-
CDOGC2	P^2CCD output gain control 2	A25	-
CDOTAE	P^2CCD out A even	A33	A33
CDOTAO	P^2CCD out A odd	A33	A33
CDOTBE	P^2CCD out B even	A33	A33
CDOTBO	P^2CCD out B odd	A33	A33
CDRD-2	P^2CCD read	A26	-
CDRSEV	P^2CCD reset even	A33	A33
CDRSOD	P^2CCD reset odd	A33	A33
CDSB	P^2CCD substrate	A33	A33
CDSGC1	P^2CCD sample gate control 1	A25	-
CDSGC2	P^2CCD sample gate control 2	A25	-
CHMMPT	Channel Min/Max pointer	A33	A33
CHPTØ1	Channel pointer Ø1	A33	A25-A12-A5
CHPTØ2	Channel pointer Ø2	A33	A33
CIHDOA	Clamp integrate hold difference out A	A33	A33
CIHDOB	Clamp integrate hold difference out B	A33	A33

When level A is present this level charges capacitor C8311 by the CDCPOD signal (Clamp phase).
When level B is present the voltage difference between A and B is present at the node C8311 and buffer V8312, because capacitor C8311 is clamped at level A.
This voltage is integrated during a constant time by the CDIGOD signal, when reset (CDRSOD) is low (Integrate phase). During this phase there are no switching signals to avoid interference.
Depending on the mode, one of the potentiometers R8421...R8424 (GAIN) is used to adjust the gain of the integrator. The potentiometers are connected to a reference voltage (RVCDG) to compensate offset in the P^2CCD output voltage.
Potentiometer R8319 (ZERO CORR) is used to adjust the output signal of the integrator to zero during a zero voltage sweep.
When the integration has stopped the output voltage of opamp N8311 represents the value of the sample.
This voltage remains there (Hold phase) until the reset signal (CDRSOD) becomes active. Meanwhile capacitor C8311 is clamped for the next sample.

The sequence Clamp, Integrate and Hold is called the microcycle. This microcycle is the same for all modes.
By varying the Hold time in different modes it is possible to apply the samples long enough to the P^2CCD switch to be switched through.
The samples are also applied to the differential stages. The differential stages are built up around opamps N8401 and N8411. Their outputs also go to the P^2CCD channel switch.
The P^2CCD channel switch is a multiplexer which switches the samples in the right sequence, depending on the mode, to the T&H and ADC on unit A11 (THINAN). The multiplexer is controlled by the P^2CCD output logic.

The P^2CCD control logic is built up around two PALs (Programmable Array Logic) D8303 and D8307.
PAL D8303 is driven by a number of P^2CCD status signals (CDRD-2 and CDOCØ1...CDOCØ2) coming from the management unit A25. It is clocked by CKCDOC-1, which is a 16 MHz clock signal, that is derived from the microprocessor clock on MRAM unit A5.
CKCDOC-1 also clocks latch D8301, which latches various signals from the slow clock divider, a transport clock (TCEV-LT), a sample clock (SCEV-2HT) and this sample clock divided by two by IC D8302.
The output signals control the P^2CCD channel switch, PAL D8307 and the output stages of the P^2CCDs (RSOD--LT and RSEV--LT).
The channel min/max pointer for the channel switch (CHMMPT) is derived from the MM signal (min/max) from the microprocessor and an output signal of the PAL (pin 19).
PAL 8307 is also clocked by the 16 MHz CKCDOC-1 signal. It generates a CLR signal for counter D8304, which also controls the PAL.
Furtheron the PAL generates the control signals for the CIH circuits (microcycle) and the STCV signal (Start Conversion) for the ADC on unit A11.

Resumed: a great deal of the signal acquisition in the various modes is determined by the two PALs D8303 and D8307.

8.33.6 P²CCD output circuit description

The P²CCD output circuit consists of 4 Clamp, Integrate and Hold (CIH) stages, 2 differential stages, the P²CCD channel switch, a slow clock divider and the P²CCD output logic. Figure 8.33.13 shows the principle and the timing diagram of the CIH AO circuit.

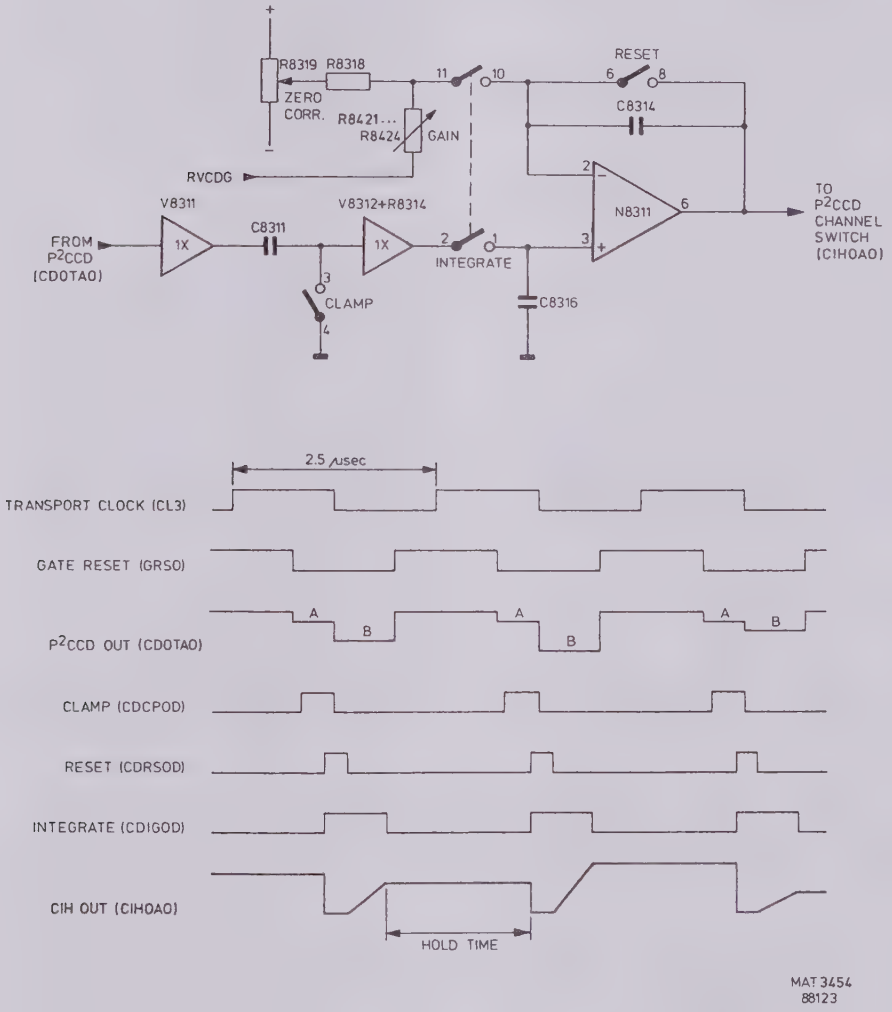


Figure 8.33.13 Principle and timing diagram of the CIH AO circuit.

While the output gate of the P²CCD is reset by GRSO its output voltage is about 20 V. This voltage is determined by the RC network at the DRSO and DRSE inputs of the P²CCD.
When this reset is removed the output voltage drops to an undefined level A. On the falling edge of the transport clock the sample leaves the output stage of the P²CCD (see also fig. 8.33.2). Now the output voltage drops to a level B. The voltage difference between level A and level B represents the value of the sample. This difference is detected as follows.

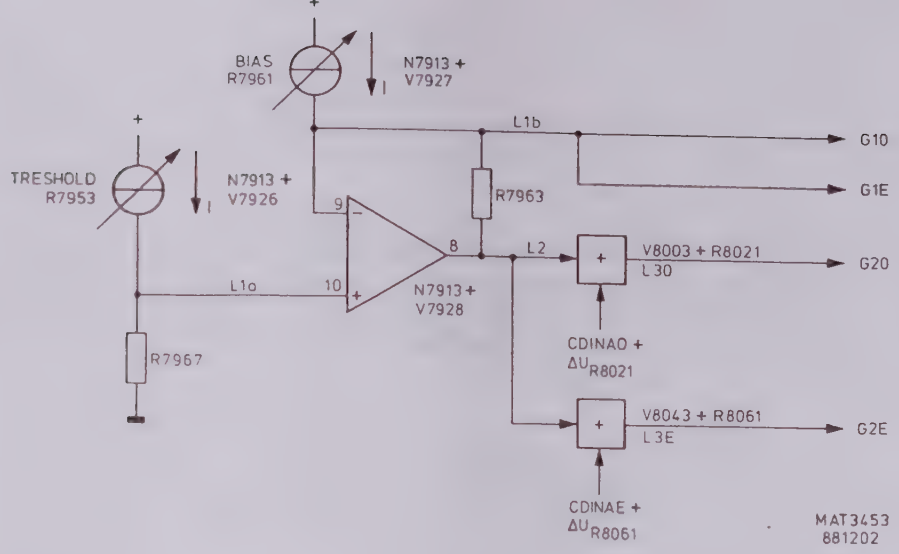


Figure 8.33.12 Principle of sample gate control.

Resumed: the circuit gives an adjustable voltage (TRESHOLD) to the G1O and G1E inputs. There is an adjustable voltage difference (BIAS) between the voltage of G1O (and G1E) and the average voltage of G2O (and the G2E).
The circuit causes the arise of charge packets in the P^2CCD. The size of these charge packets is modulated by the voltage on the G2O input (the analogue signal). These charge packets represent the samples of the input signal. Next they are transported through the P^2CCD under control of the Transport Clock.

The transport clocks (TCODA-LX) and (TCODDALX), which come from the driver unit A24, are applied directly to the P^2CCDs.
Since the transport clock on the Even side is always in antiphase with the transport clock on the Odd side, TCODA-LX is in antiphase with TCEVA-LX. TCODDALX is delayed 1 ns to TCODA-LX and TCEVDALX is delayed 1 ns to TCEVA-LX.
This results in a four phase clock system which is used for the peristaltic transport of samples inside the P^2CCD.
The output signal of the P^2CCD (OUTO = Out Odd) is led to the CIH AO circuit via transistor V8318 (CDOTAO).
Via transistor V8004 the output gate of the P^2CCD can be reset.

The remaining connections of the P^2CCD are kept at certain levels by means of simple RC networks.
These connections are:

- SUB Substrate
- DRSO Drain Reset Odd
- DRSE Drain Reset Even
- GSP Gate Separator
- DSFS Drain Source Followers.

8.33.5 P^2CCD circuit description

WARNING: The P^2CCD is a MOS device, which is sensitive for electrostatic discharges. It should be handled with care.

Since channel A and B are identical and of each channel the Even and the Odd side are identical, only channel A Odd side will be described.

The analogue input current from the signal switch (CDINAO) is led via a common base circuit, consisting of transistors V8002, V8003 and associated components, to the G2O input (Gate 2 Odd) of the P^2CCD.

The sample clock (SCODA-HX), which comes from the driver unit A24, is led to the following inputs of the P^2CCD:

- INO Input Odd
- G3O Gate 3 Odd
- G4O Gate 4 Odd

The signal STODA-HX is applied to the clock terminator circuit.
Via RC-networks (R7936,C7913 and R7937,C7914) the average DC levels of the odd and even sample clocks (ASODA and ASEVA) are applied to a differential amplifier, followed by an integrator. This is the circuit around opamp N7651. The output signal (SCOCA) is applied to the sample clock driver on driver unit A24.
This feedback system results in an equal average DC level of the odd and even sample clock.

The circuit around transistor V8001 is a current source, which gives a fixed current through resistor R8004 and choke L8007.
This results in a constant voltage difference between the G3O and G4O inputs.
The circuit around opamp N7911 and transistor V7919 is a very stable current source, which gives an adjustable current (R7939, BIAS CHARGE) through resistor R8003 and choke L8006. This results in a constant voltage difference between the INO and the G3O inputs.

Figure 8.33.12 gives the principle of the remaining circuit which is used for the control of the sample gate of the P^2CCD.
Via an adjustable current source (R7953, TRESHOLD) and R7967 a constant level (L1a) is made and buffered (L1b) by means of opamp N7913 and transistor V7928. This level is applied to the G1O and G1E inputs.
This level is dropped by means of an adjustable current source (R7961, BIAS) and R7963 (L2). To this level the voltage drop over R8021 (and R8061) and the analogue input signal is added and this is applied to G2O and G2E (L3O and L3E).

For timing reasons sometimes clock signals have to be delayed. This is done by using delay lines on cable spool assemblies as interconnection

NOTE: The sample clock signals are supplied from the driver unit A24 via 75 ohm coax cables, the transport clock signals are supplied via 50 ohm cables.

8.33.4 Signal switch circuit description

Since channel A and B are identical, only channel A is described

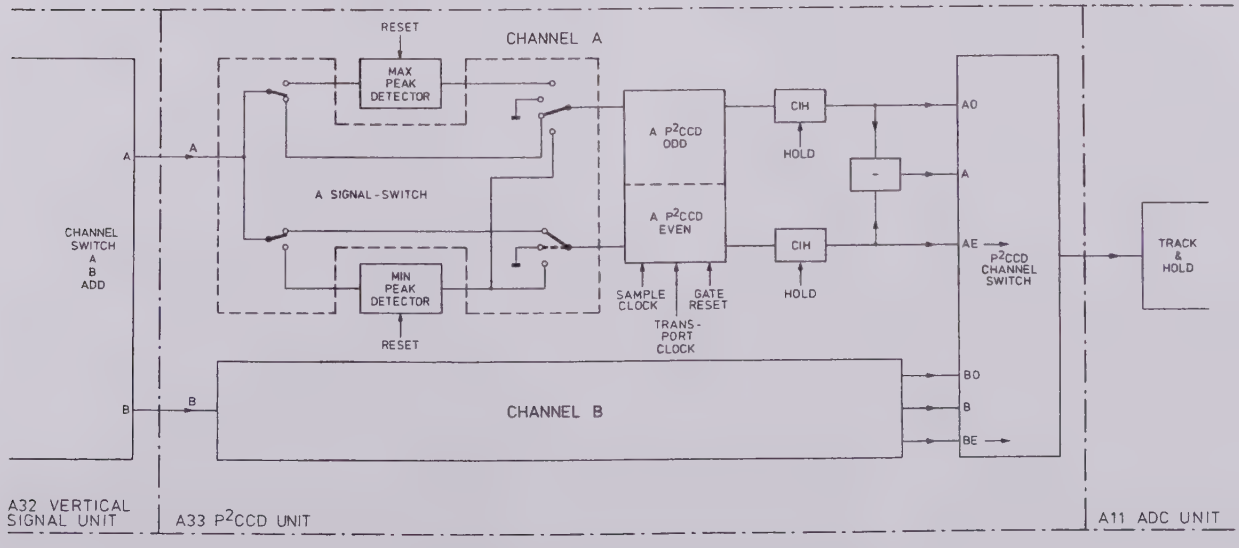
The symmetrical signals from the vertical signal unit A32 (SWINAN and SWINAP) go via V7502 and V7503 to the SIGNAL SWITCH, consisting of D7501, D5707, D5708, D5706 and associated components.
The circuit around transistors V7562 and V7563 is a compensation circuit for the DC level, when dual channel mode is switched on.
The circuit around transistor V7556 is a compensation circuit for the DC level when ADD mode is switched on. This circuit is not present in channel B.
The signal switch can guide the input signals to the MAX PEAK detector (D7502, pin 10) and the MIN PEAK detector (D7504, pin 10). The output signals of the peak detectors (pin 2) go back to the signal switch (D7507 and D7508 pin 3+4). The ICs D7507 and D7508 switch the signals to D7501 and D7506 (pins 19+20; symmetrical signal).
They can also switch a zero voltage level to pin 19 of the ICs D7501 or D7507 (pin 18, an asymmetrical signal) for the zero voltage sweeps.
Each peak detector has its own reset circuit, which is controlled by the reset pulses (RSMXPD and RSMNPB) coming from the mini CCD logic unit A49. The output currents of the signal switch (D7501 pin 22 and D7506 pin 22) go to the Odd (CDINAO) and the Even (CDINAE) side of the P^2CCD via coaxial cables.
The signal switch is controlled by 10 status signals (ST1...ST10), which are generated in the status logic. They are derived from ZECH, CHMMPT and PDSW0...PDSW2.
ZECH indicates if a zero voltage sweep is made in a P^2CCD mode or DIRECT SPECIAL mode (1 = zero voltage sweep).
CHMMPT indicates which peak detector is selected. It is generated in the P^2CCD output logic (0 = MAX, 1 = MIN).
Below the truth table for the other signals can be found.

Time base setting	PDSW 0	1	2	ST1	ST2	ST3	ST4	ST5	ST6	ST7	ST8	ST9	ST10
Normal >= 0.5 ms/div	0	1	0	1	0	0	x	x	x	x	x	x	x
Normal <= 0.2 ms/div	0	0	0	-z	-z	0	x	x	x	x	x	x	x
MIN / MAX >= 2 ms/div	1	1	0	0	1	-c	c	0	0	-c	0	1	1
MIN / MAX <= 1 ms/div	1	1	0	0	0	1	-z	0	z	-z	z	1	0

Note: z = ZECH
-z = not ZECH
c = CHMMPT
-c = not CHMMPT

8.33.3.8 RANDOM SAMPLING mode (50 ns/div...5 ns/div)
Single + Dual channel

In RANDOM SAMPLING mode samples are continously taken by the Even side of the P^2CCD with a rate of 50 MHz, so every 20 nsec. The transport clock frequency is 100 MHz, so between the samples there are dummy samples to reduce crosstalk between the samples (see figure 8.33.11). The number of samples, which are required for one sweep, depends on the time base setting.
In 50 ns/div setting, a sweep has a length of 500 nsec. The required number of samples is then 500/20=25 samples.
In 5 ns/div setting, the sweep length is 50 nsec, which means that there are 50/20=2.5 dots required.
Depending on the delta-t measurement result, 2 or 3 samples are needed. In this case there are always 3 samples taken. If the third sample is not needed, it is not used later by the DPU.
After a trigger, the sampling and transporting continues until the desired samples are just before the output gate in the P^2CCD.
Now the transport frequency changes over to 400 kHz and the samples are transported via the P^2CCD channel switch to the ADC.
In Single channel mode this switch is switched to the desired input channel (AEven or BEven).
In Dual channel this switch alternates between AEven and BEven, thereby ignoring the dummy samples (see figure 8.33.11).
When the samples are converted, a sweep of samples of zero voltage level is taken (see dashed position of signal switch in figure 8.33.11) and converted to perform digital leakage correction.
The Odd side of the P^2CCD´s is not used in this mode.
In case of a negative trigger delay (pretrigger) the P^2CCD´s serve as a pretrigger memory.
In Single channel mode, the addresses Ø, 8, 16, 24, etc of register RØ are used for samples. When the 512 different addresses are filled with samples a picture is complete. The remaining addresses are filled with interpolated samples.
In Dual channel mode the addresses Ø, 4, 8, 12, etc of register RØ are used.
In SINGLE SCAN mode, the acquisition stops as soon as 512 samples at different addresses are in register RØ.



8.33.3.7 P^2CCD mode (200 us/div...5 us/div)
Single + Dual channel, MIN / MAX

The signals from the channel switch are applied to the peak detectors. The P^2CCD´s take samples from their outputs (see figure 8.33.10). Further on, this mode works exactly equivalent as the P^2CCD mode with MIN / MAX off (time conversion principle).
In the time base setting 5 usec/div the sweep length is 50 usec. A sweep consists of 250 MAX and 250 MIN samples over 10 divisions on the screen.
So the distance between 2 MAX samples is 50/250 = 0,2 usec = 200 nsec.
The reset time of the peak detectors is 20 nsec, in which the peak detectors don´t watch the input signal.
So there is a "blind time" ratio of 10%.
In faster time base settings, the "blind time" ratio increases, so using MIN / MAX is not allowed.

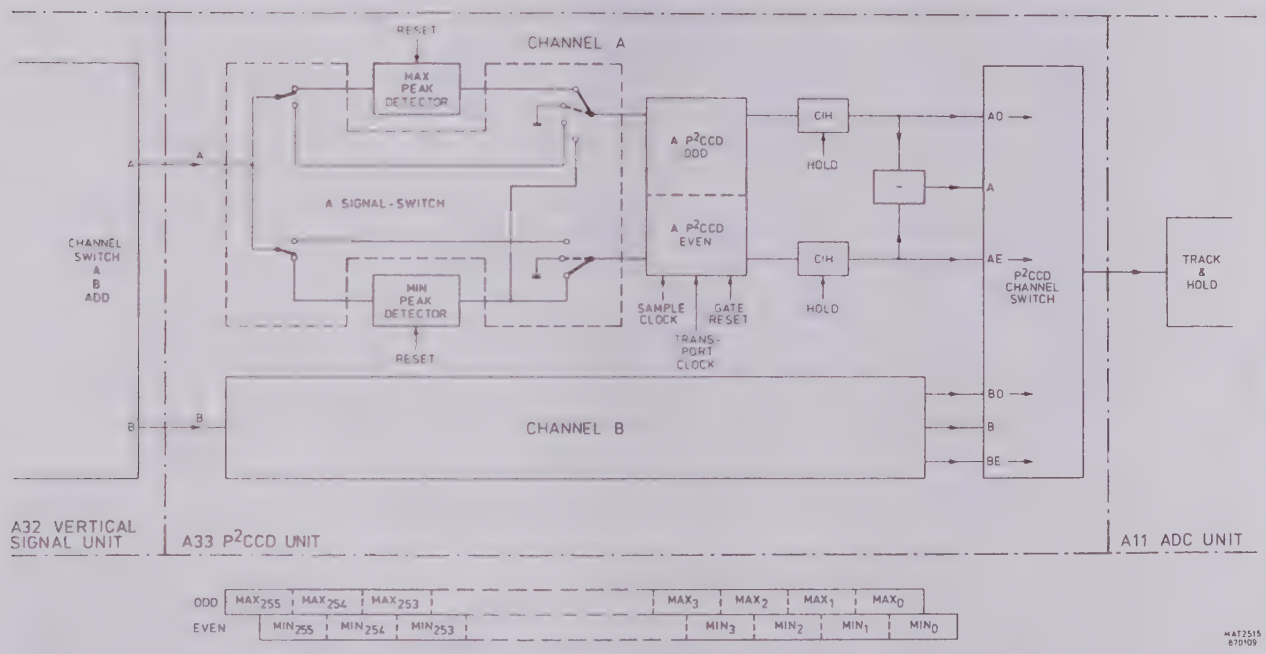


Figure 8.33.10 P^2CCD mode
Single + Dual channel, MIN / MAX.

8.33.3.6 DIRECT SPECIAL mode (1 ms/div and 500 us/div)
Single + Dual channel MIN / MAX

The signals from the channel switch are applied to the peak detectors. The Odd side of the P^2CCD takes continuously samples of the MIN peak detector, the even side takes samples of the MAX peak detector. Because the sample clock frequency (200 kHz) is the half of the transport clock frequency (400 kHz) dummy samples are placed between the MIN samples resp. the MAX samples (see figure 8.33.9).
In the 1 msec/div time base setting in Single channel mode, 4096 samples are converted after a trigger, 2048 from the MIN peak detector and 2048 from the MAX peak detector. The P^2CCD switch alternates between AO and AE, thereby ignoring the dummy samples.
Afterwards a sweep of 2x2048 samples of a zero voltage level is taken (see dashed line in figure 8.33.9) and converted to perform digital leakage correction in the DPU.
In Dual channel mode, 2048 samples (1024 on each P^2CCD side) are taken at each sweep (total 4096 samples), followed by zero sweep. The P^2CCD channel switch alternates between AO, BO, AE and BE.
In the 500 usec/div time base setting 512 samples on each channel (256 MIN samples and 256 MAX samples) are taken, followed by 2x256 zero voltage samples on each channel. The DPU performs the digital leakage correction.

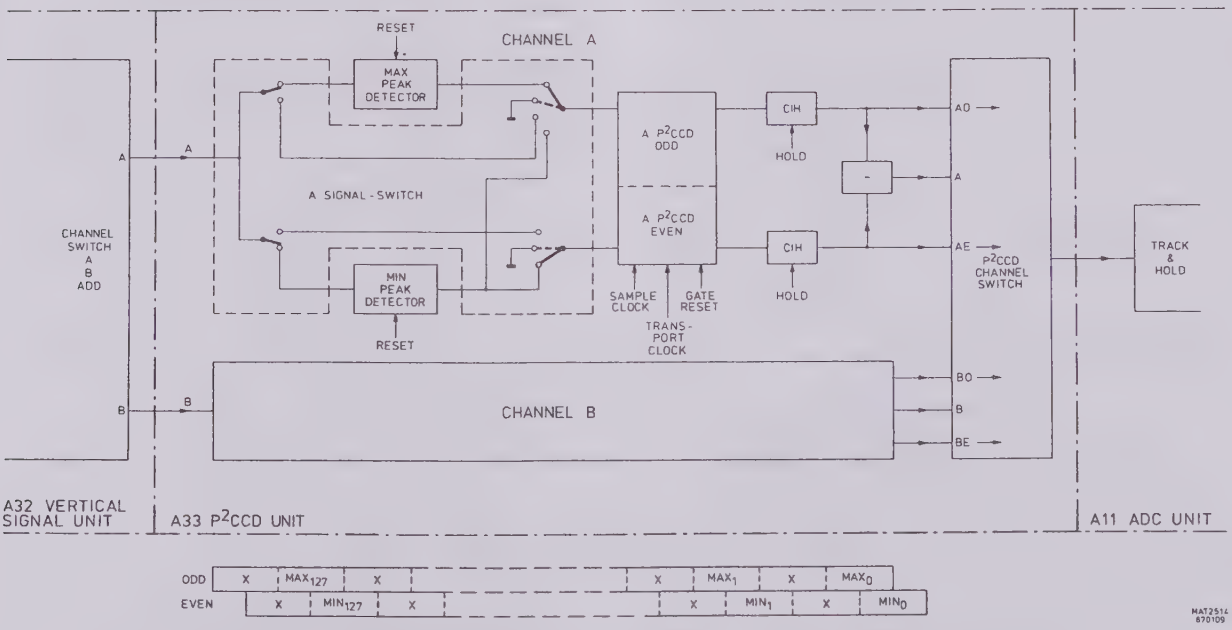


Figure 8.33.9 DIRECT SPECIAL mode
Single + Dual channel, MIN / MAX.

8.33.3.5 ROLL + DIRECT mode (360 s/div...2 ms/div)
Single + Dual channel, MIN / MAX

In these modes the signals from the channel switch are applied to the peak detectors, called resp. MAX peak detector and MIN peak detector (see figure 8.33.8).
The Odd side of the P^2CCD takes samples alternatively from the MAX and the MIN peak detector (see signal switch positions 1 and 2). Because the sample frequency is the half of the clock frequency dummy samples are placed between the MIN and MAX samples, to achieve less cross talk between the samples.

When a sample has been taken the concerning peak detector is reset with a pulse of 20 nsec. length, which comes from the CCD logic unit (A26).
The Even side of the P^2CCD takes samples of a zero voltage level, which are substracted from the Odd side samples in the differential stage behind the CIH circuits to achieve analogue leakage correction.
Next the corrected samples are selected by the P^2CCD channel swith and applied to the T&H and DAC.
In Single channel the P^2CCD channel switch remains in position A or B, depending on the selected input channel. Now every sample is converted twice, of which the DPU ignores one.

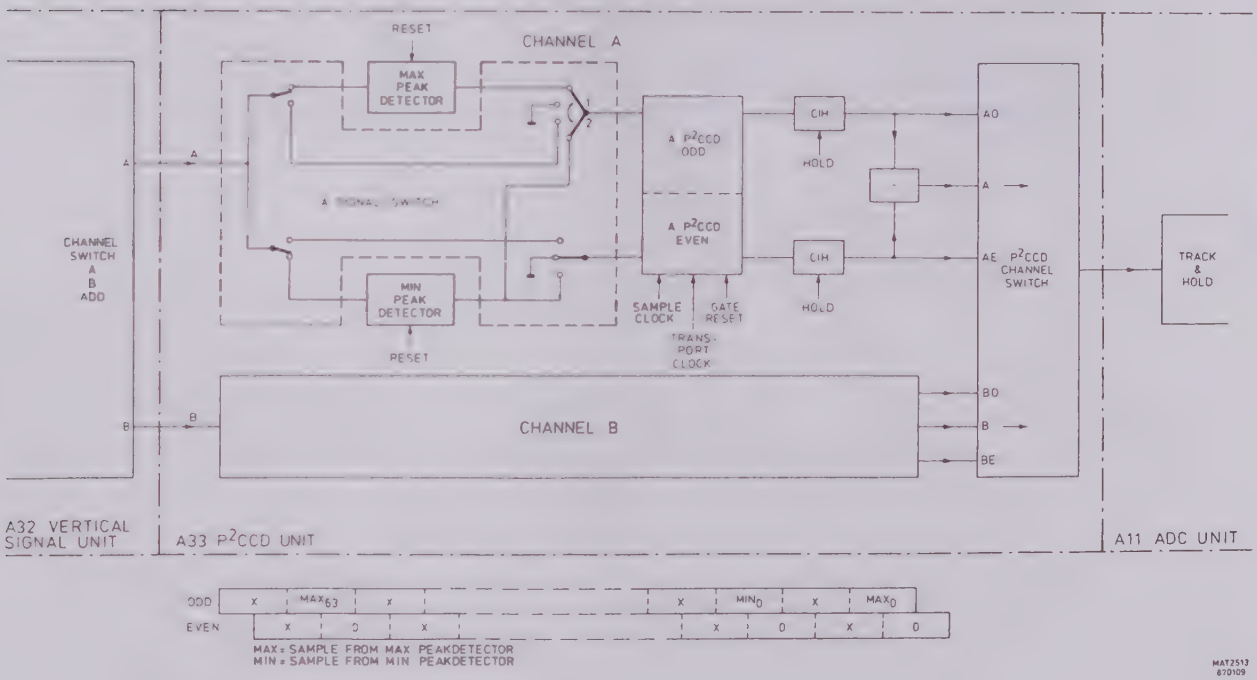


Figure 8.33.8 ROLL + DIRECT mode
Single + Dual channel, MIN / MAX.

The DPU determines which samples are placed on which address in register RØ, depending on time base settings, etc (see also ROLL + DIRECT mode, Single channel)
In the 2 ms/div time base setting in Single channel mode, all the real samples (4096/sweep) are converted.
At lower time base settings there are more samples converted as needed for placing in register RØ. Now the DPU dtermines for each series of MAX samples which one is the biggest. This sample is placed in register RØ.
The same is done for the MIN samples, but now the smallest one is placed in the register RØ.
This principle is called Digital MIN / MAX.

8.33.3.4 MAXIMUM RESOLUTION mode (500 us/div...100 ns/div) Single + Dual channel

In this mode every sweep 512 samples are taken in Single channel mode and 2 x 512 samples in Dual channel mode. The delta-t circuit on the clock unit (A34) measures the time between the trigger moment and the moment the first sample is taken. This is used to determine on which address between the first and the eight´s (4096/512) address the first sample has to be placed.
The next sample is placed 8 addresses higher and so on.
In Dual channel mode the delta-t information is used to determine on which address between the first and the fourth (2048/512) address the first sample has to be placed.
The next sample is placed 4 addresses higher and so on.

The remaining addresses are filled with samples, which are calculated by the DPU by means of interpolation.
When a new sweep of 512 samples is taken after a trigger, it is placed in the register RØ on the addresses which are determined by the value given by the delta-t circuit. So the calculated samples are replaced by real samples.
In this way, a high resolution display with low jitter is realised.
When SINGLE SCAN is selected the acquistion stops as soon as all interpolated samples are replaced by real samples.

8.33.3.3 P^2CCD mode (200 us/div...100 ns/div)
Single + Dual channel (see figure 8.33.8)

In these modes the time conversion principle is used.

Samples are taken and transported with a rate of 250 kHz to 250 MHz, depending on the selected time base setting (0,2 msec/div to 200 nsec/div.). After a trigger, the sampling and transporting is stopped after a while. The moment depends on the selected trigger delay.
The P^2CCD contains 512 samples, which are now transported with a low transport clock frequency of 100 kHz to the P^2CCD channel switch.
So every 2,5 microsecond a sample comes out of one of the P^2CCD's.
The P^2CCD channel switch alternates in Dual channel between AOdd, BOdd, AEven and BEven to apply the samples to the T&H and ADC, where they are converted (see figure 8.33.7).
In Single channel, the P^2CCD switch alternates between AOdd and AEven or BOdd and BEven, depending on the selected input channel. Now every sample is converted twice. The DPU "throws away" one of every two converted samples.
After all samples are converted, a new sweep of samples is taken with high sample and transport frequency and converted with the low transport frequency. This time the samples are taken of a zero voltage level (see dashed signal switch position in figure 8.33.8). Afterwards the DPU substracts these zero voltage samples from the corresponding signal samples to perform digital leakage correction.
The samples are placed at addressess in Register RØ in the same way as in the DIRECT SPECIAL mode.

On the screen 500 samples are displayed over 10 divisions, this is 50 samples/div. So in the time base setting 100 nsec/div every 2 nsec a sample is taken. This means a sample frequency of 500 Msamples/s, which is the maximum sample rate.
In case of a negative trigger delay (pretrigger) the P^2CCDs serve as a pretrigger memory.

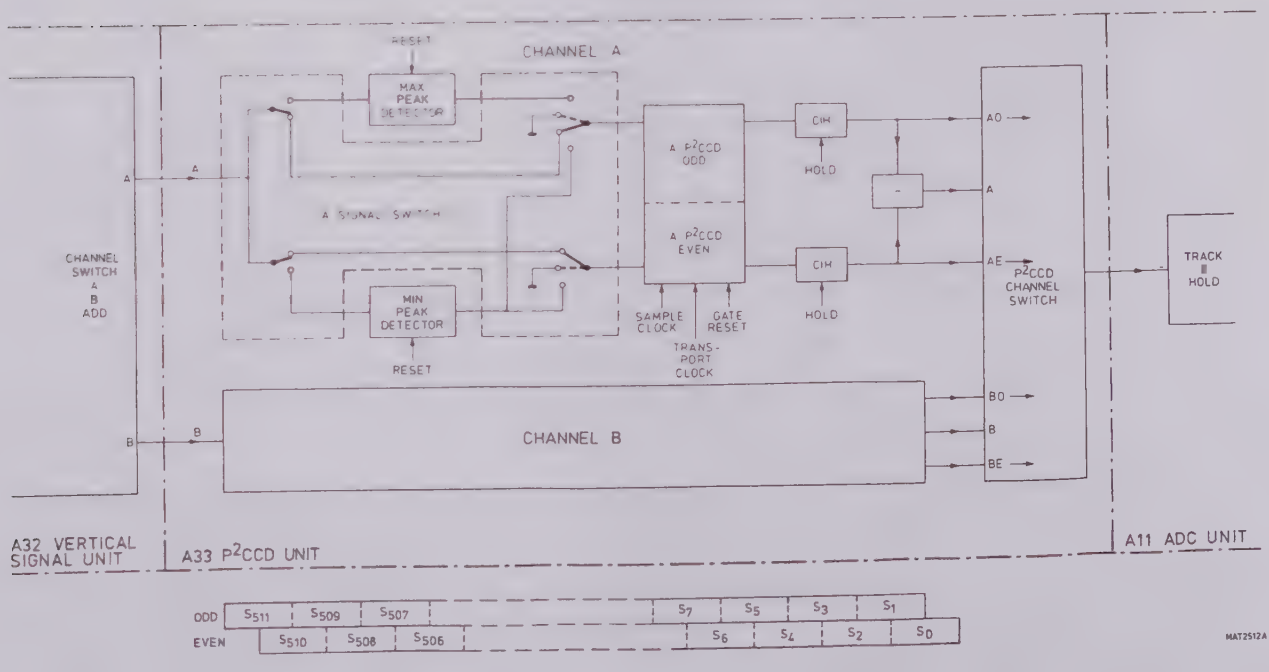


Figure 8.33.7 P^2CCD mode
Single + Dual channel.

8.33.3.2 ROLL, DIRECT and DIRECT SPECIAL mode (360 s/div...500 us/div)
Dual channel

Each channel works in the same way as described in the single channel mode (see figure 8.33.6). In both channels the samples are taken at exactly the same moments. Register RØ is now 2048 samples wide for each channel. The sample clock frequency (200 kHz) is the half of the transport frequency (400 kHz). So the real sample output rate of each P^2CCD is 200 kHz, which enables the P^2CCD switch to apply in an alternating way the samples of both channels to the T&H and ADC. The dummy samples are ignored.
In the DIRECT SPECIAL mode (500 us/div) 512 samples are taken at each channel. They are placed in addresses Ø, 4, 8, 12, etc of register RØ. The remaining addresses are filled with samples, which are calculated by the DPU by means of interpolation.

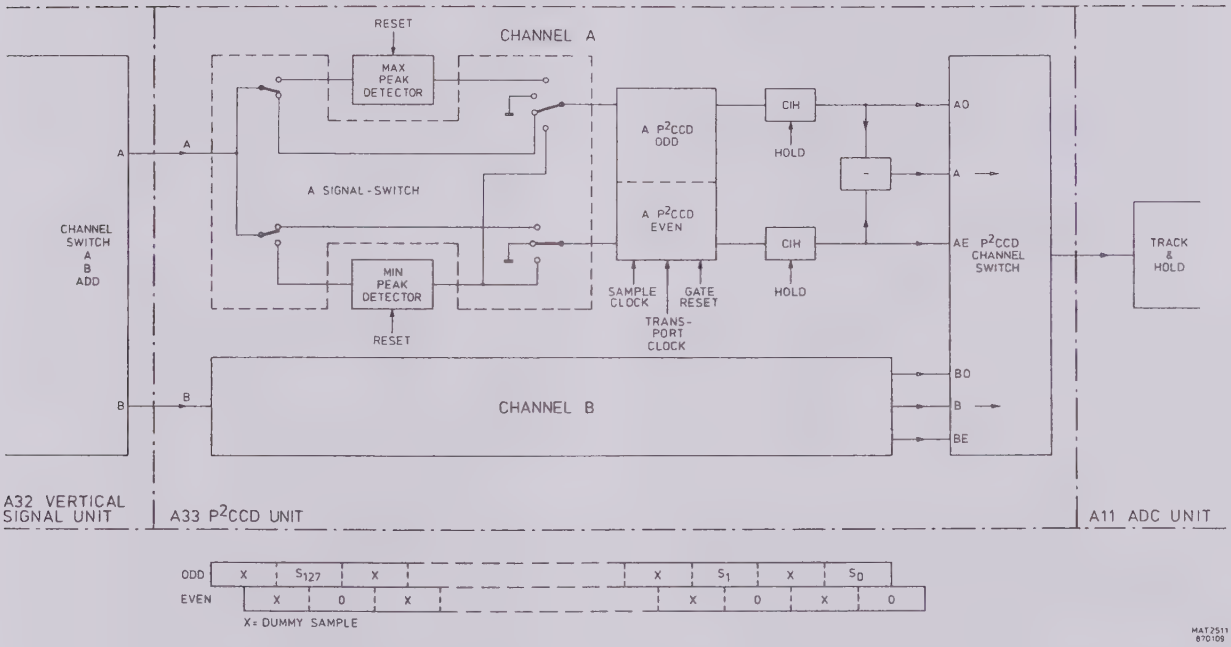


Figure 8.33.6 ROLL + DIRECT + DIRECT SPECIAL mode
Dual channel.

8.33.3.1 ROLL + DIRECT + DIRECT SPECIAL mode (360 s/div...500 us/div)
Single channel

In these modes samples are continuously taken with a rate of 400 kHz by the Odd side of the P^2CCD (see figure 8.33.5) and transported to the CIH circuit, where they can be held for a certain time. On the Even side samples of a zero voltage level are taken and transported to the CIH circuit. Signals on the Odd and Even side are substracted in the differential stage to perform analogue leakage correction of the P^2CCD circuit.
Next, the corrected samples are selected by the P^2CCD channel switch and applied to the T&H and ADC.
Every 2,5 microsecond a sample is converted.
The digital processing unit (DPU, unit A9) determines which samples are placed on which address in register RØ, depending on the selected time base setting and trigger delay.
In the 1 ms/div time base setting, all samples are placed in register RØ, which is 4096 converted samples wide.
In the DIRECT SPECIAL mode (500 us/div) 512 samples are taken. The samples are placed in addresses Ø, 8, 16, 24, etc of register RØ. The remaining addresses are filled with samples, which are calculated by the DPU by means of interpolation.

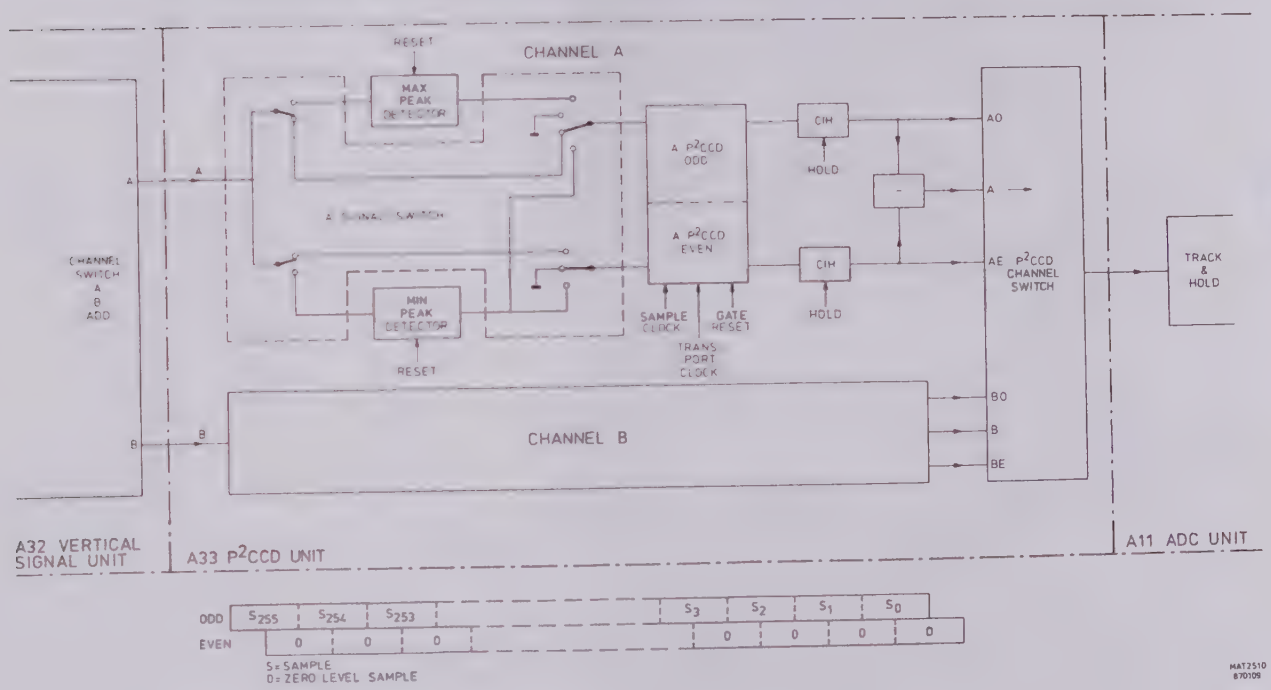


Figure 8.33.5 ROLL + DIRECT + DIRECT SPECIAL mode
Single channel.

Figure 8.33.4 shows a block diagram of unit A33. Signals from channels A and B from the vertical signal unit (A32) go via the signal switch to the P^2CCD's. The signal switch gives various switching possibilities (e.g. signals through peak detectors) for the input signals for the P^2CCD's.
Behind the P^2CCD's the already mentioned CIH circuits can be found. The output signals go directly to the P^2CCD channels switch and to a substraction stage. The substracted signal also goes to the P^2CCD channel switch.

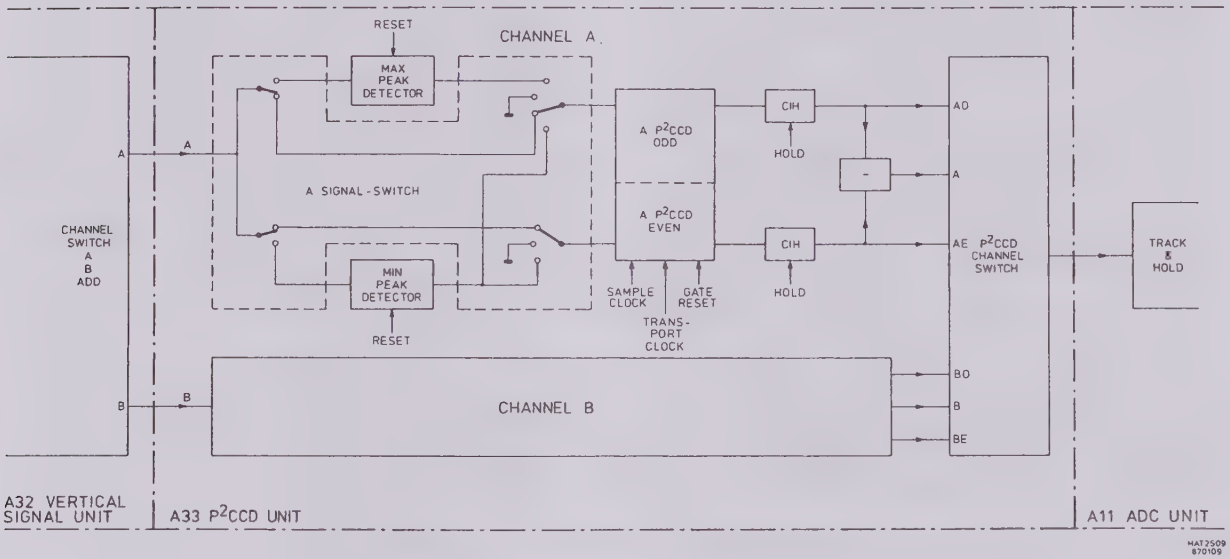


Figure 8.33.4 Block diagram of unit A33.

In all modes, the signal processing is exactly the same in both channels and happens synchronously until the P^2CCD switch. The P^2CCD switch applies the samples of both channels or one channel in the right sequence to the T&H circuit and the ADC, which can be found on unit A11.

Next all modes are discussed, illustrated with block diagrams with the signal switches in the correct position and with the schematic representation of the contents of a P^2CCD.

8.33.3 Operation of the modes

Below an overview can be found of the various modes in which the oscilloscope can operate.

	MODE				Samples/channel			
Time base Range	Normal		MIN / MAX		Normal		MIN / MAX	
	SINGLE	DUAL	SINGLE	DUAL	SINGLE	DUAL	SINGLE	DUAL
360s/div-50ms/div	ROLL	ROLL	ROLL	ROLL	4K	2K	4K	2K
5s/div-2ms/div	DIRECT	DIRECT	DIRECT	DIRECT	4K	2K	4K	2K
1ms/div			DIRECT SPECIAL	DIRECT SPECIAL			4K	2K
0,5ms/div	DIRECT SPECIAL	DIRECT SPECIAL	DIRECT SPECIAL	DIRECT SPECIAL	0,5K 4K *	0,5K 2K *	0,5K	0,5K
0,2ms/div-5us/div	P^2CCD-mode	P^2CCD-mode	P^2CCD-mode	P^2CCD-mode	0,5K 4K *	0,5K 2K *	0,5K	0,5K
2us/div-100ns/div								
50ns/div-5ns/div	RS- ** mode	RS- ** mode			0,5K	0,5K		

* Maximum Resolution
** Repetitive only

The sample clock frequency and the transport clock frequency are the same in the following modes:

- ROLL, DIRECT } Only Single channel, MIN / MAX off
- DIRECT SPECIAL} Only normal
- All P^2CCD modes, MIN / MAX off or on

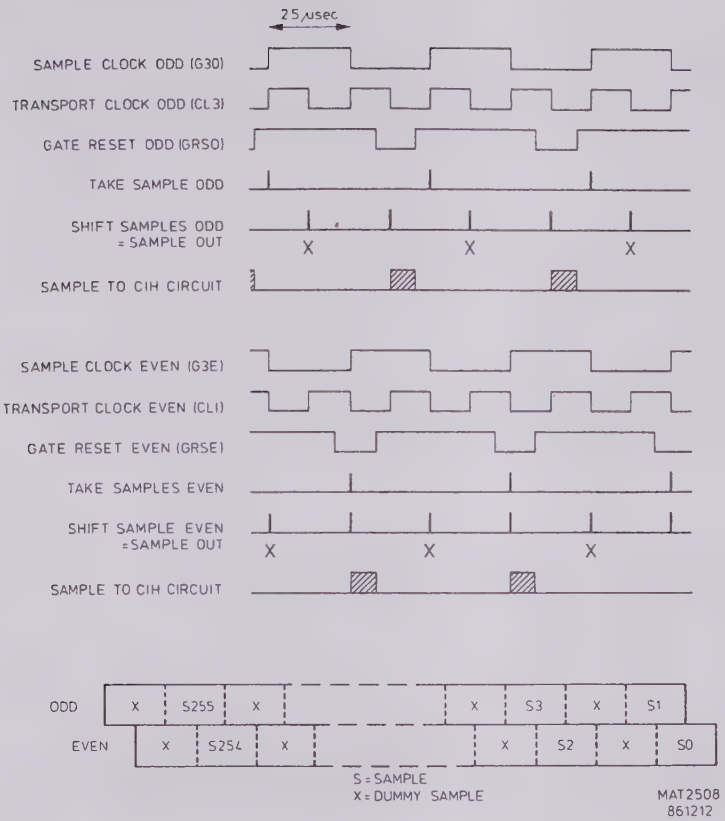


Figure 8.33.3 Sample and transport sequence II.

NOTE: The dummy samples, which are marked with an X, don´t come out the output gate, because the reset signal is active then.

During the transport, the level of the samples changes, due to leakage. This leakage depends upon the time the sample is in the P^2CCD. Of course this leakage has to be compensated. Generally this is done by taking a sample of a zero voltage level and transport it with the same speed as the original sample. As it comes out the P^2CCD its level is only determined by leakage. By substracting this level from the level of the original sample with leakage, the leakage is eliminated.

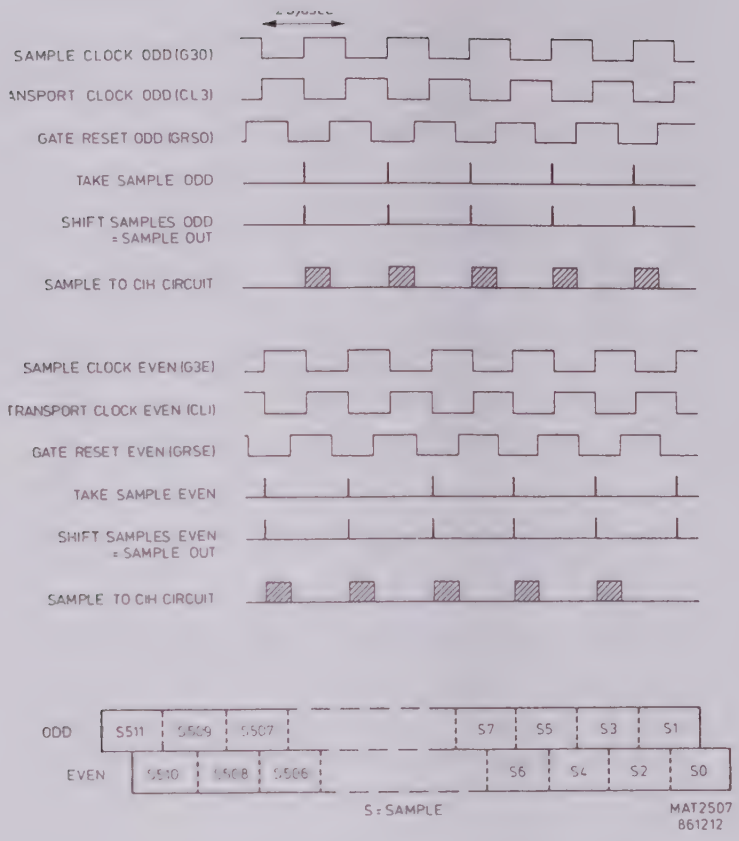


Figure 8.33.2 Sample and transport sequence I.

NOTE: The needles do not represent signals, but are moments on which a sample is taken and other samples are transported.

In some other modes the sample clock frequency is the half of the transport clock frequency. This means that transports take place, while there have no samples been taken.
In this way dummy samples are created between real samples.
These dummy samples reduce cross talk between real samples which is required in some modes.
The sampling and transport sequence and the contents of the P^2CCD are summarised below.

8.33.2 The P^2CCD description

The P^2CCD (Profiled Peristaltic Charge Coupled Device), which is basically an analogue shift register, consists of an ODD-side and an EVEN side. Each side consists of a sample gate, 256 stages through which the samples can be shifted and an output gate (see figure 8.33.1).

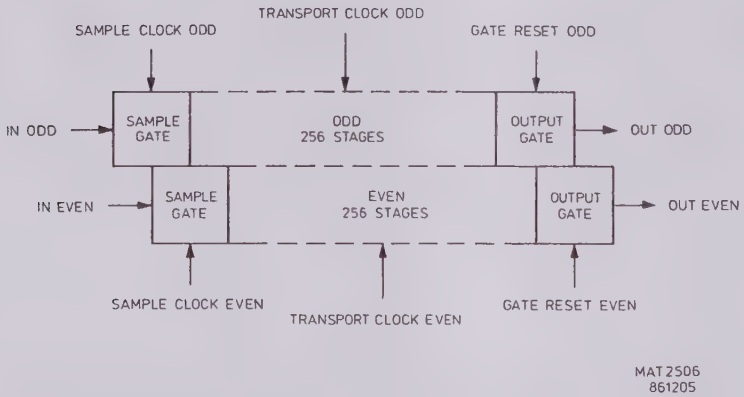
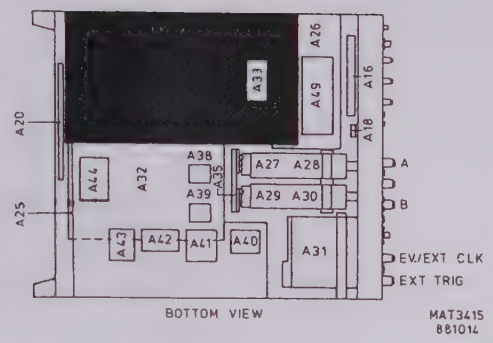


Figure 8.33.1 Schematic diagram of a P^2CCD circuit.

The clock signals of the ODD and the EVEN side are always in anti phase (see figure 8.33.2 and 8.33.3).
On the rising edge of the sample clock a sample of the input signal is taken.
On the falling edge of the sample clock this sample is shifted to the first stage. On the falling edge of the transport clock all the samples in the stages are shifted (transported) one stage and the last sample is transported to the output stage. Before the latter happens, the gate reset signal has to be removed.
Behind the P^2CCD there is a circuit that takes over the samples, after which the gate reset is applied again. This circuit, which consists of a Clamp, Integrate and Hold part, is called CIH circuit.
In a number of modes, of which an overview is given in chapter 8.33.2, the sample clock and the transport clock have the same frequency, but are in anti phase. In this case the sampling and transport sequence and the contents of the P^2CCD can be summarised as below.

UNIT A33 - P^2CCD UNIT



CONTENTS

8.33.1	General information	8.33-1
8.33.2	The P^2CCD description	8.33-2
8.33.3	Operation of the modes	8.33-5
8.33.4	Signal switch circuit diagram	8.33-15
8.33.5	P^2CCD circuit description	8.33-16
8.33.6	P^2CCD output circuit description	8.33-18
8.33.7	Signal name list	8.33-20

8.33.1 GENERAL INFORMATION

The P^2CCD unit takes samples from the analog input signals from the Vertical Signal unit A32 and supplies these samples to the ADC and T&H unit A11. The peak detectors for the min/max function are also on this unit.

The circuits are divided over 8 diagrams:

- figure 8.33.16 signal input of both channels and status logic.
- figure 8.33.17 peak detectors and signal switch of channel A.
- figure 8.33.18 peak detectors and signal switch of channel B.
- figure 8.33.19 P^2CCD control and P^2CCD of channel A.
- figure 8.33.20 P^2CCD control and P^2CCD of channel B.
- figure 8.33.21 P^2CCD output circuits of both channels.
- figure 8.33.22 P^2CCD output control logic and clock terminators.
- figure 8.33.23 power supply.

NOTE:

This unit has SMD components and conventional components.
Some components are soldered on the bottom side of the p.c.b.

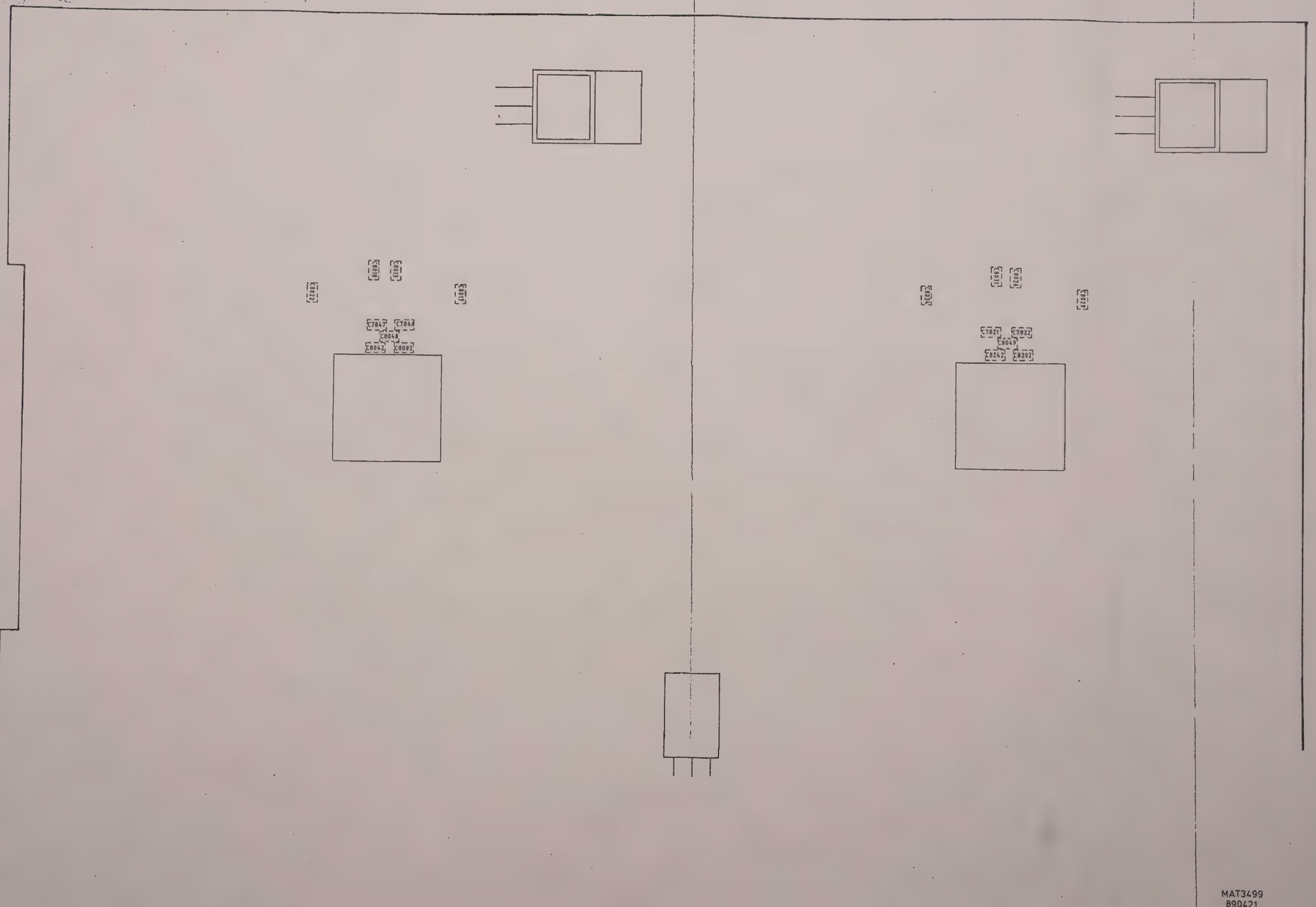
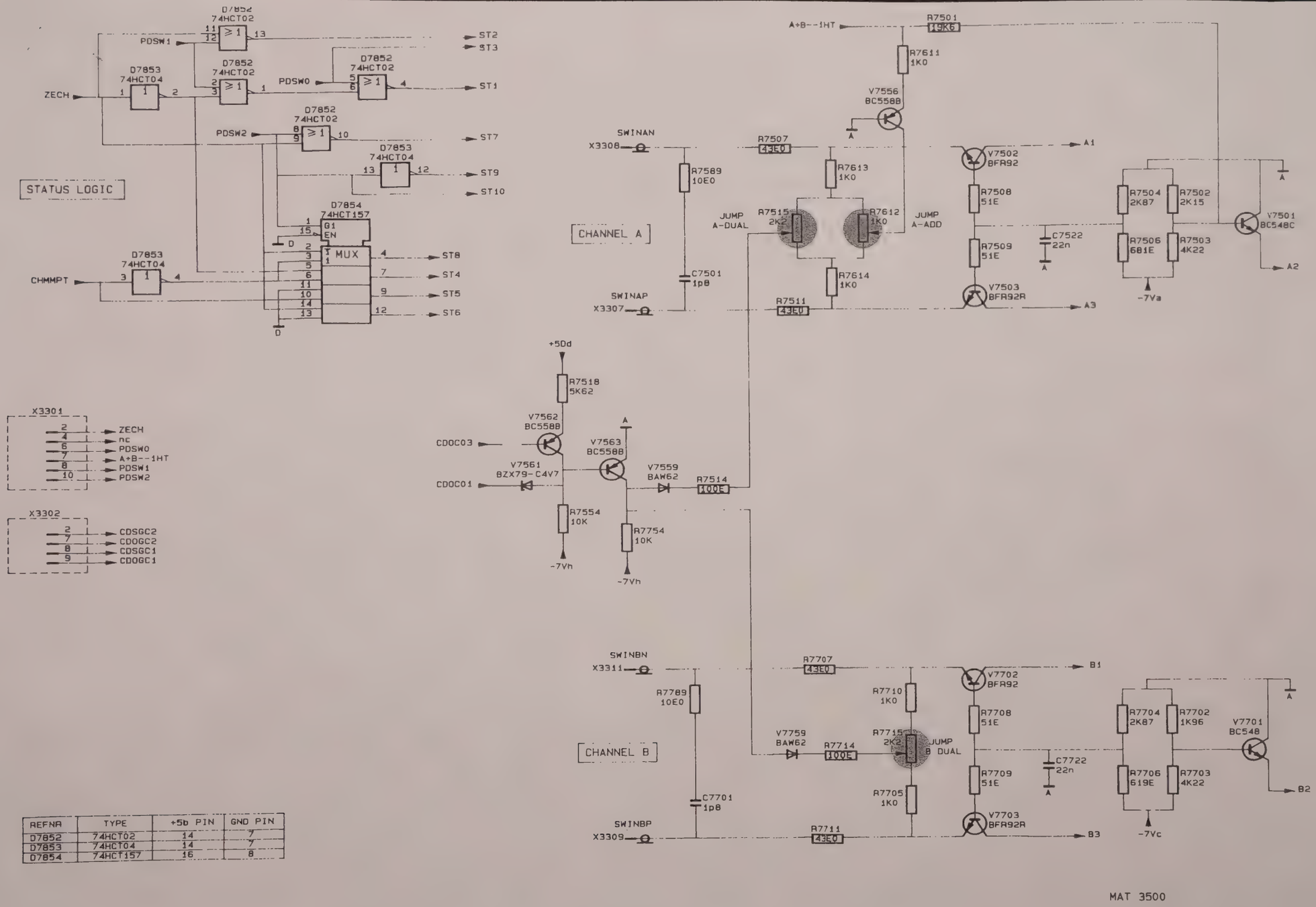
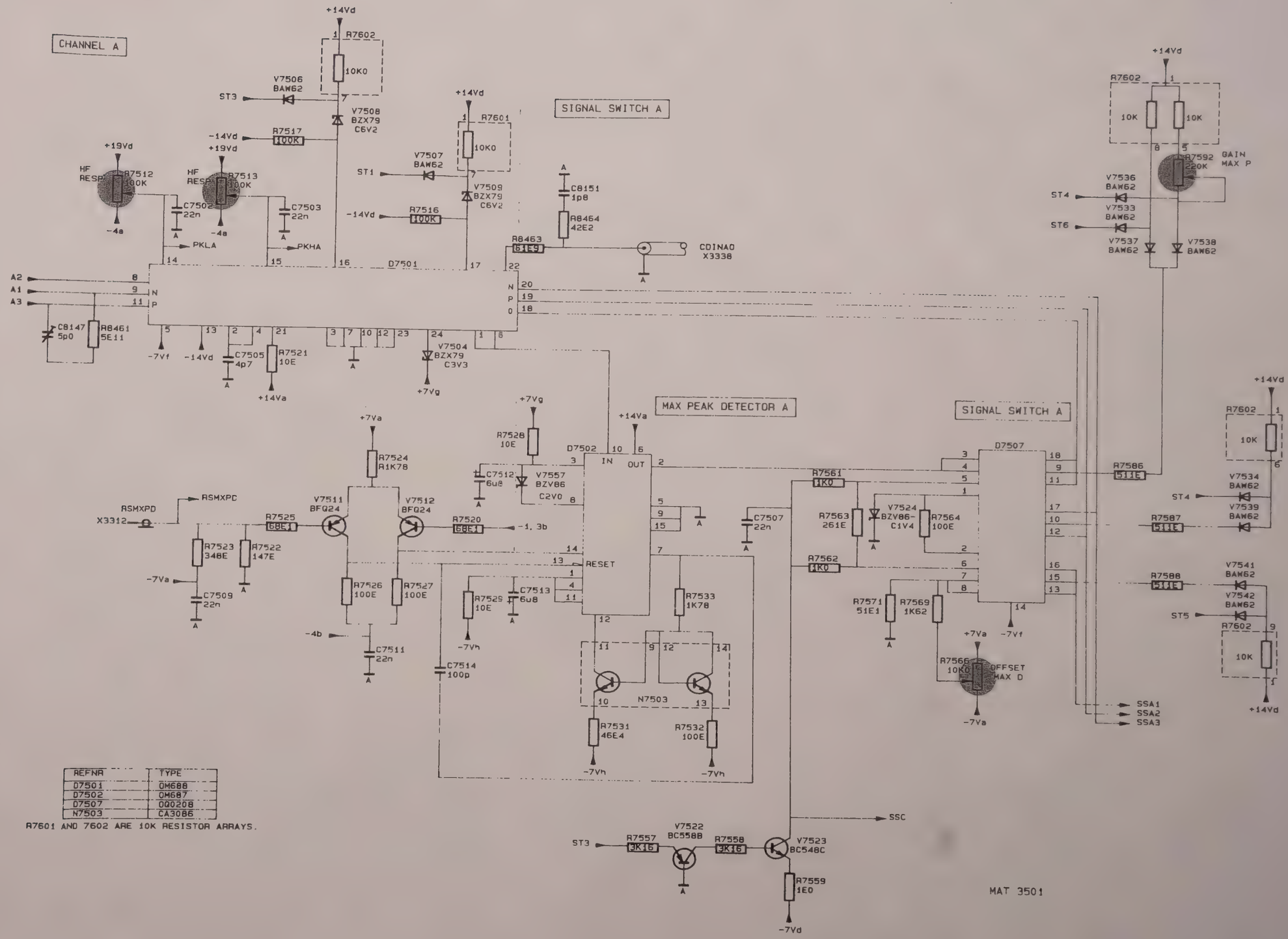


Figure 8.33.14 Unit A33 - P^2CCD - p.c.b. lay-out.



REFNR	TYPE	+5b PIN	GND PIN
D7852	74HCT02	14	7
D7853	74HCT04	14	7
D7854	74HCT157	16	8

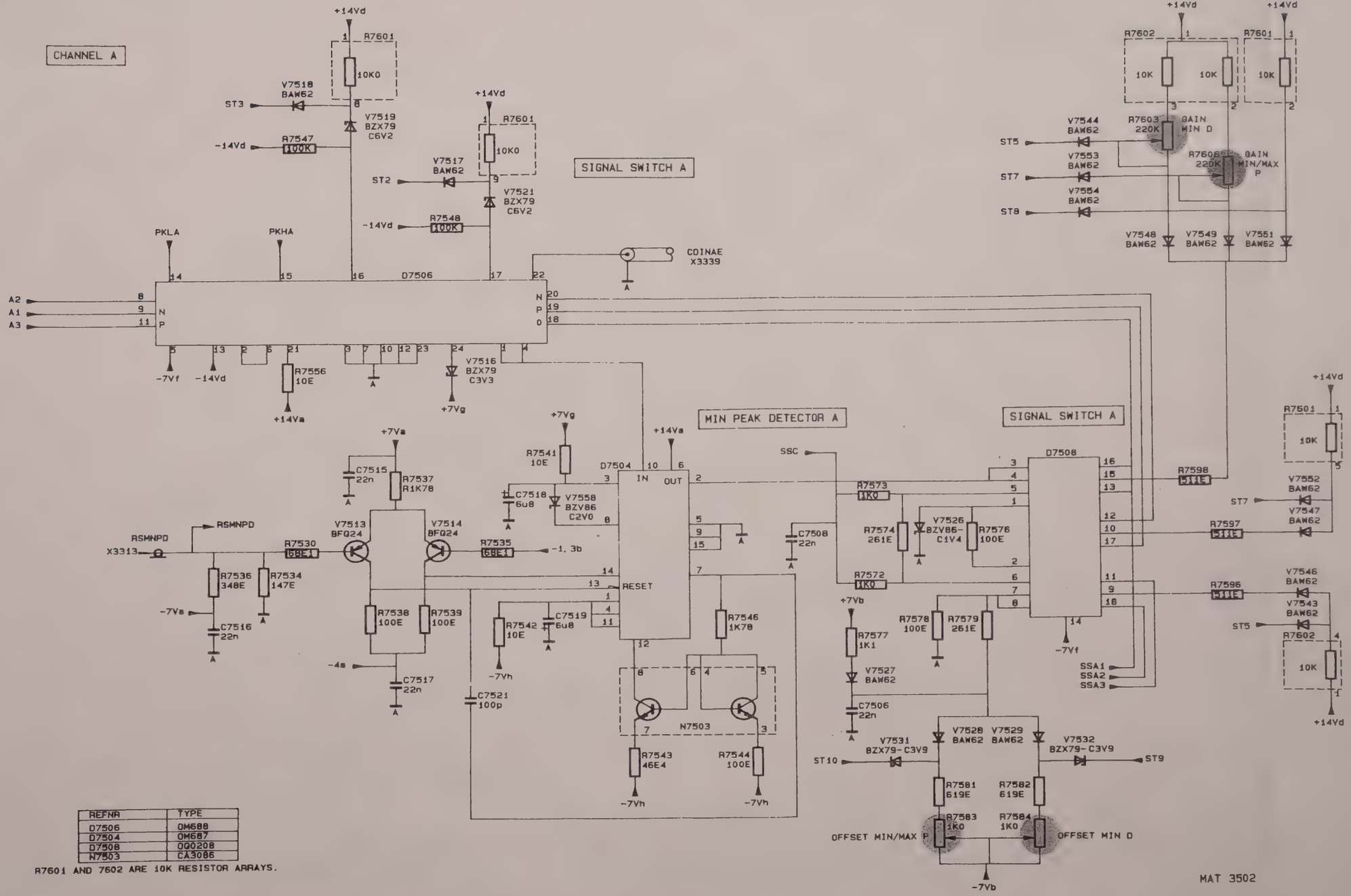
Figure 8.33.16 Unit A33 - P^2CCD - circuit diagram.



REFNR	TYPE
D7501	OM688
D7502	OM687
D7507	OQ0208
N7503	CA3086

R7601 AND 7602 ARE 10K RESISTOR ARRAYS.

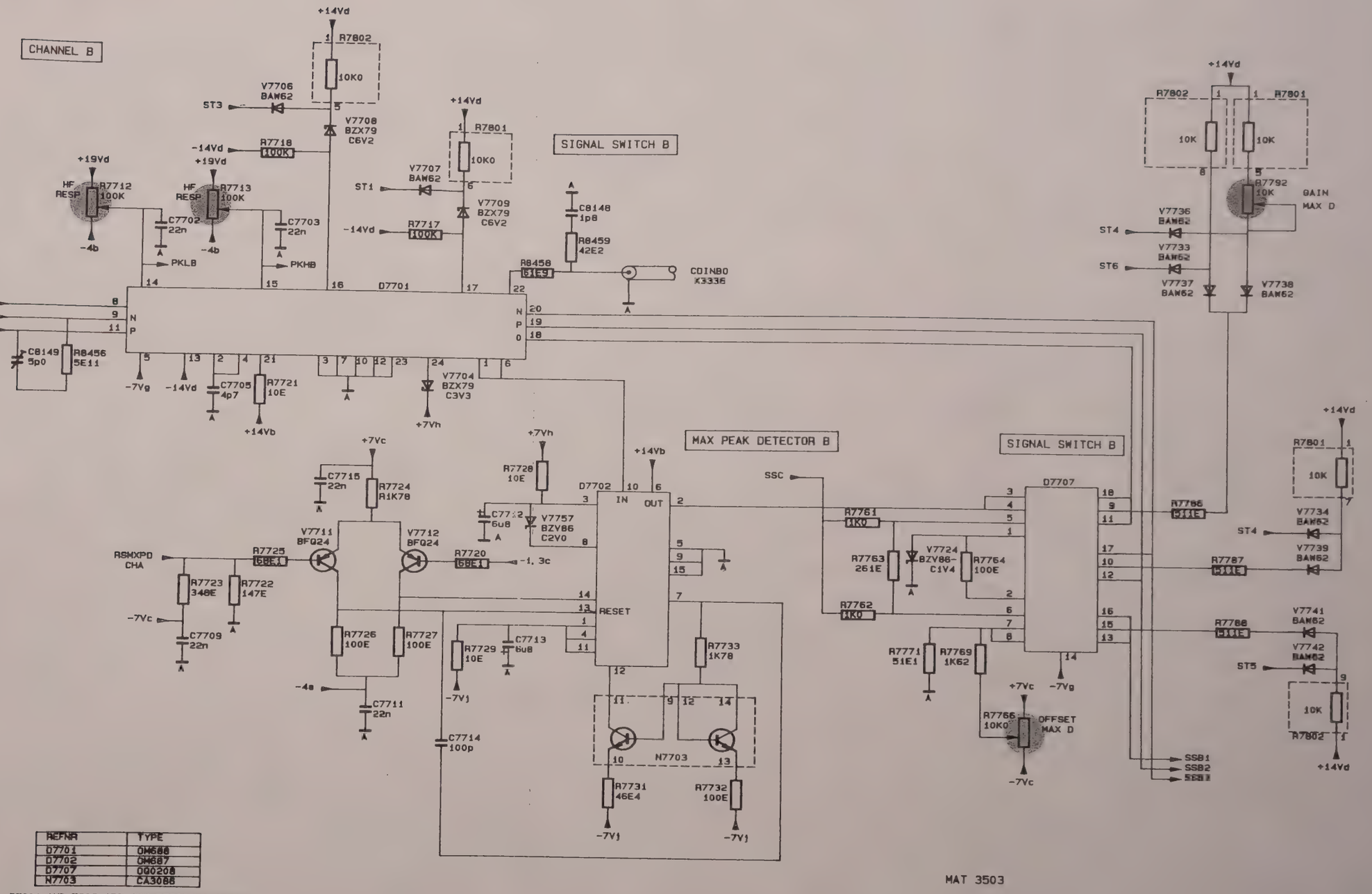
Figure 8.33.17 Unit A33 - P^2CCD - circuit diagram.



REFNR	TYPE
D7506	OM688
D7504	OM687
D7508	QQ0208
N7503	CA3086

R7601 AND 7602 ARE 10K RESISTOR ARRAYS.

Figure 8.33.18 Unit A33 - P^2CCD - circuit diagram.



REFNR	TYPE
D7701	OM680
D7702	OM687
D7707	OQ0208
N7703	CA3086

R7801 AND 7802 ARE 10K RESISTOR ARRAYS.

Figure 8.33.19 Unit A33 - P^2CCD - circuit diagram.

CHANNEL B

SIGNAL SWITCH B

MIN PEAK DETECTOR B

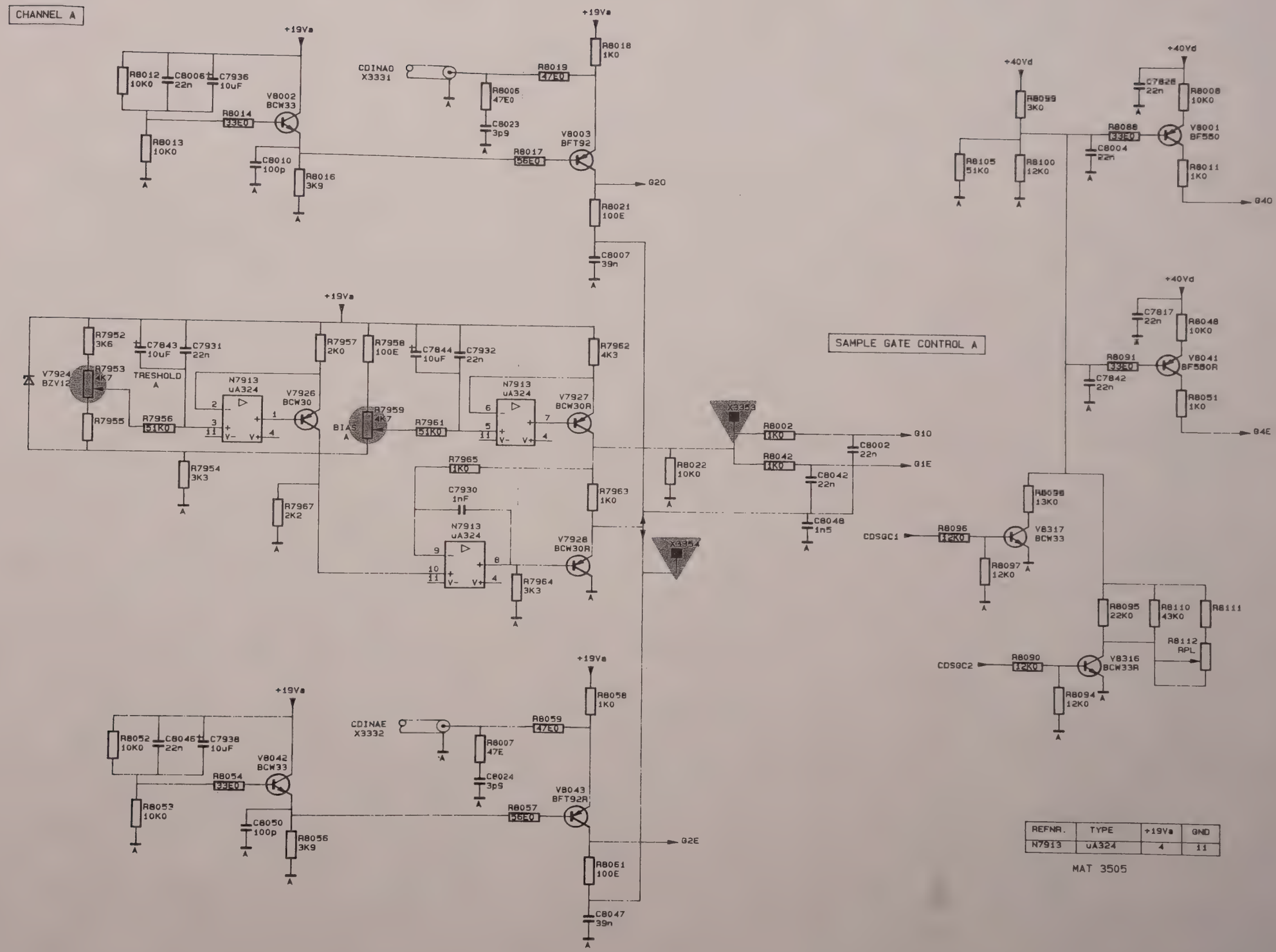
SIGNAL SWITCH B

REFNR	TYPE
D7706	OM688
D7704	OM687
D7708	OQ0208
N7503	CA3086

R7801 AND 7802 ARE 10K RESISTOR ARRAYS.

MAT 3504

Figure 8.33.20 Unit A33 - P^{2}CCD - circuit diagram.



REFNR.	TYPE	+19Va	GND
N7913	uA324	4	11

MAT 3505

Figure 8.33.21 Unit A33 - P^2CCD - circuit diagram.

REFNR.	TYPE	ODD ANALOG GROUND	EVEN ANALOG GROUND
D8001	OM3021	24, 25, 27, 28, 30, 31, 33, 34, 36	3, 4, 6, 7, 9, 10, 12, 13
N7911	LF356		
N7912	LF356		

Figure 8.33.22 Unit A33 - P^2CCD - circuit diagram.

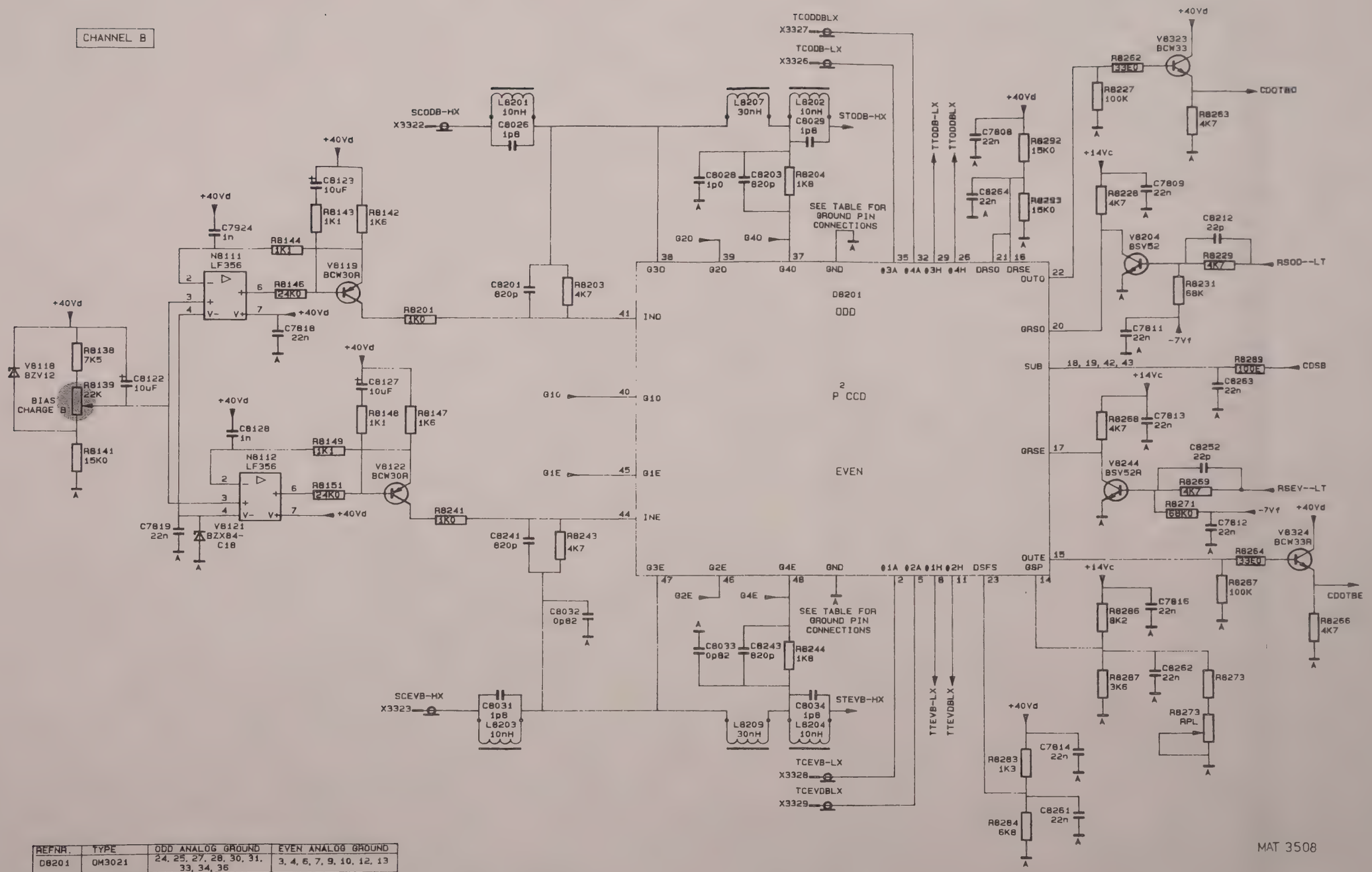
CHANNEL B

SAMPLE GATE CONTROL B

REFNR.	TYPE	+19Va	GND
N8113	uA324	4	11

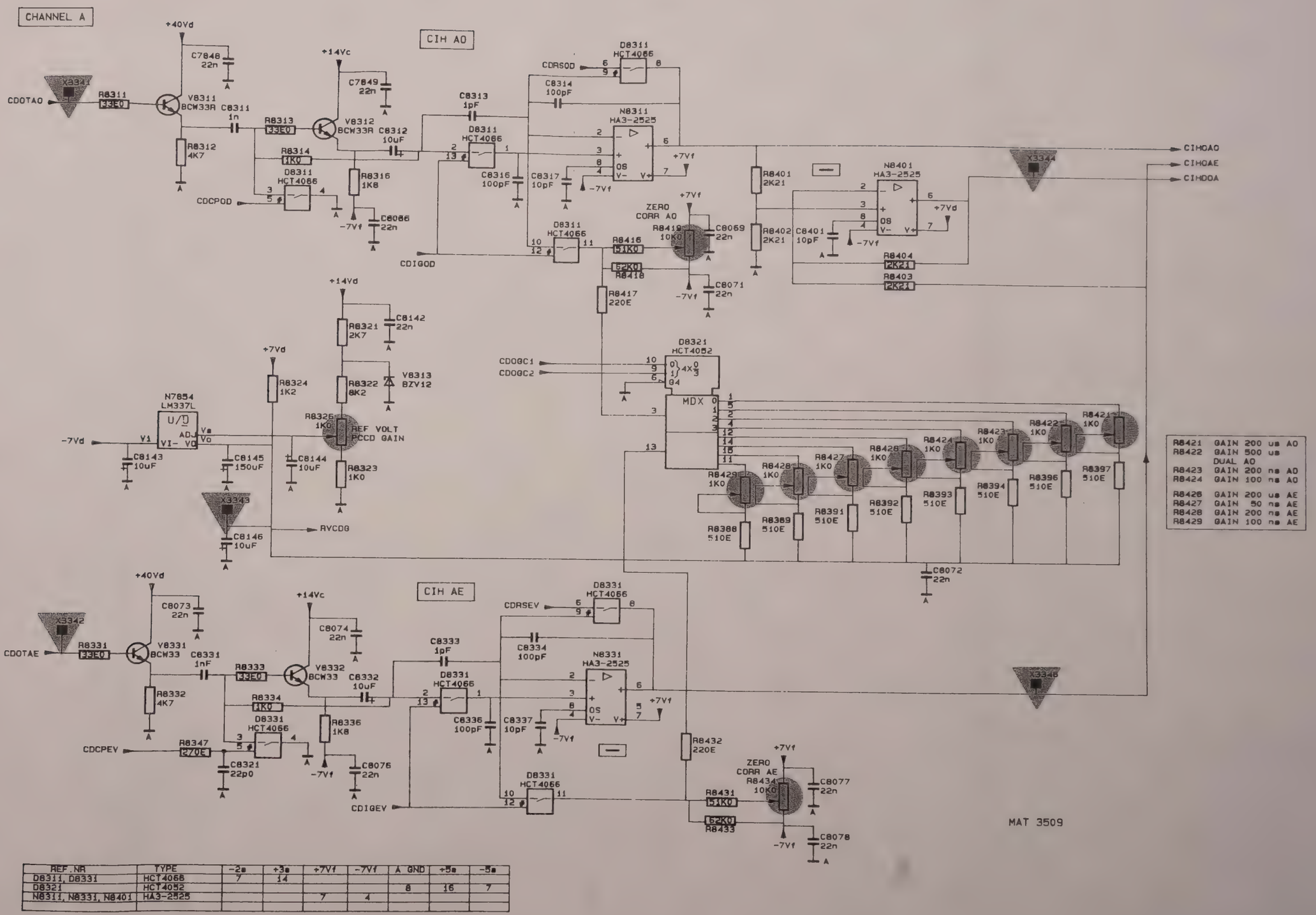
MAT 3507

Figure 8.33.23 Unit A33 - P^2CCD - circuit diagram.



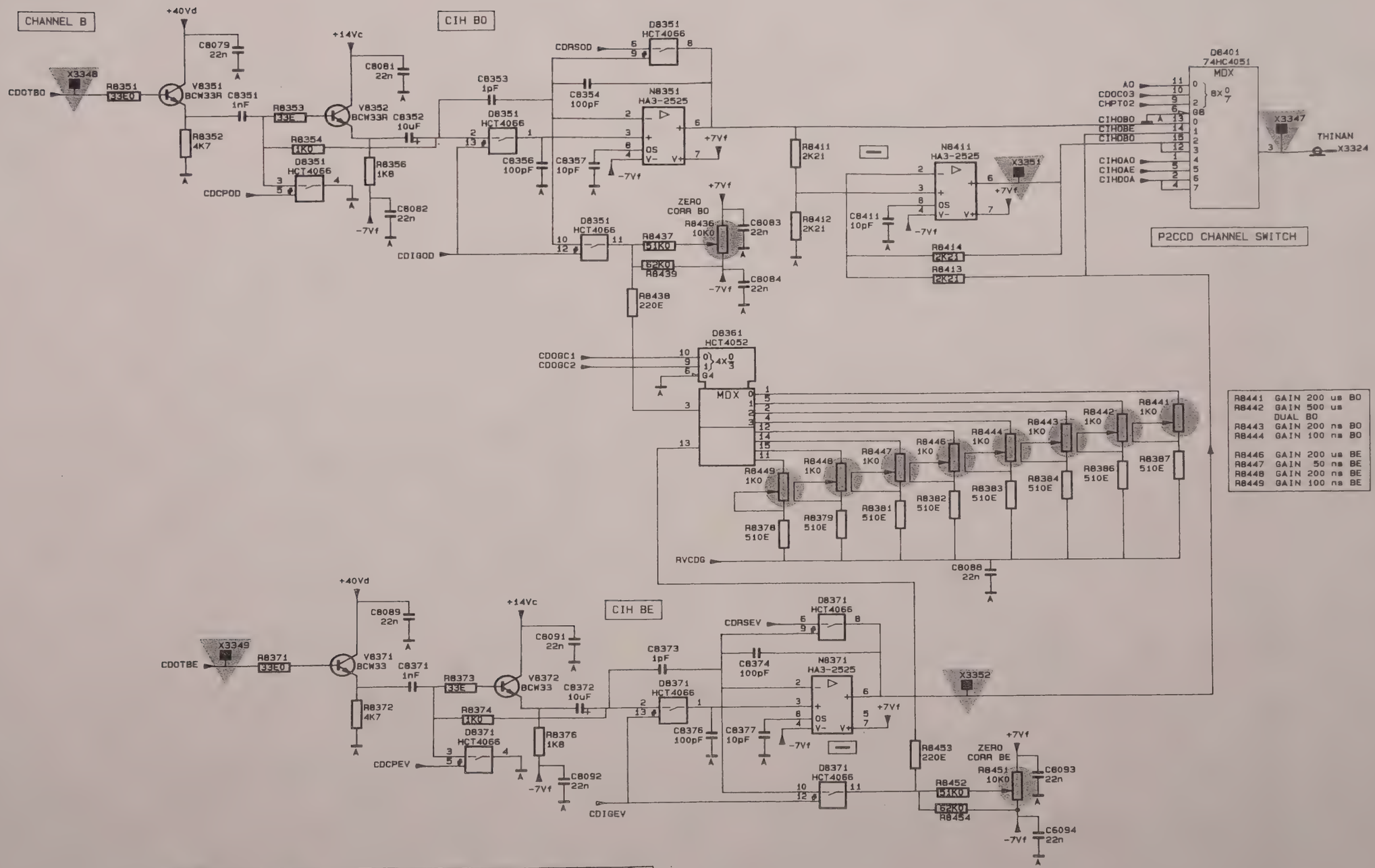
REFNR.	TYPE	ODD ANALOG GROUND	EVEN ANALOG GROUND
D8201	OM3021	24, 25, 27, 28, 30, 31, 33, 34, 36	3, 4, 6, 7, 9, 10, 12, 13
N8111	LF356		
N8112	LF356		

Figure 8.33.24 Unit A33 - P^2CCD - circuit diagram.



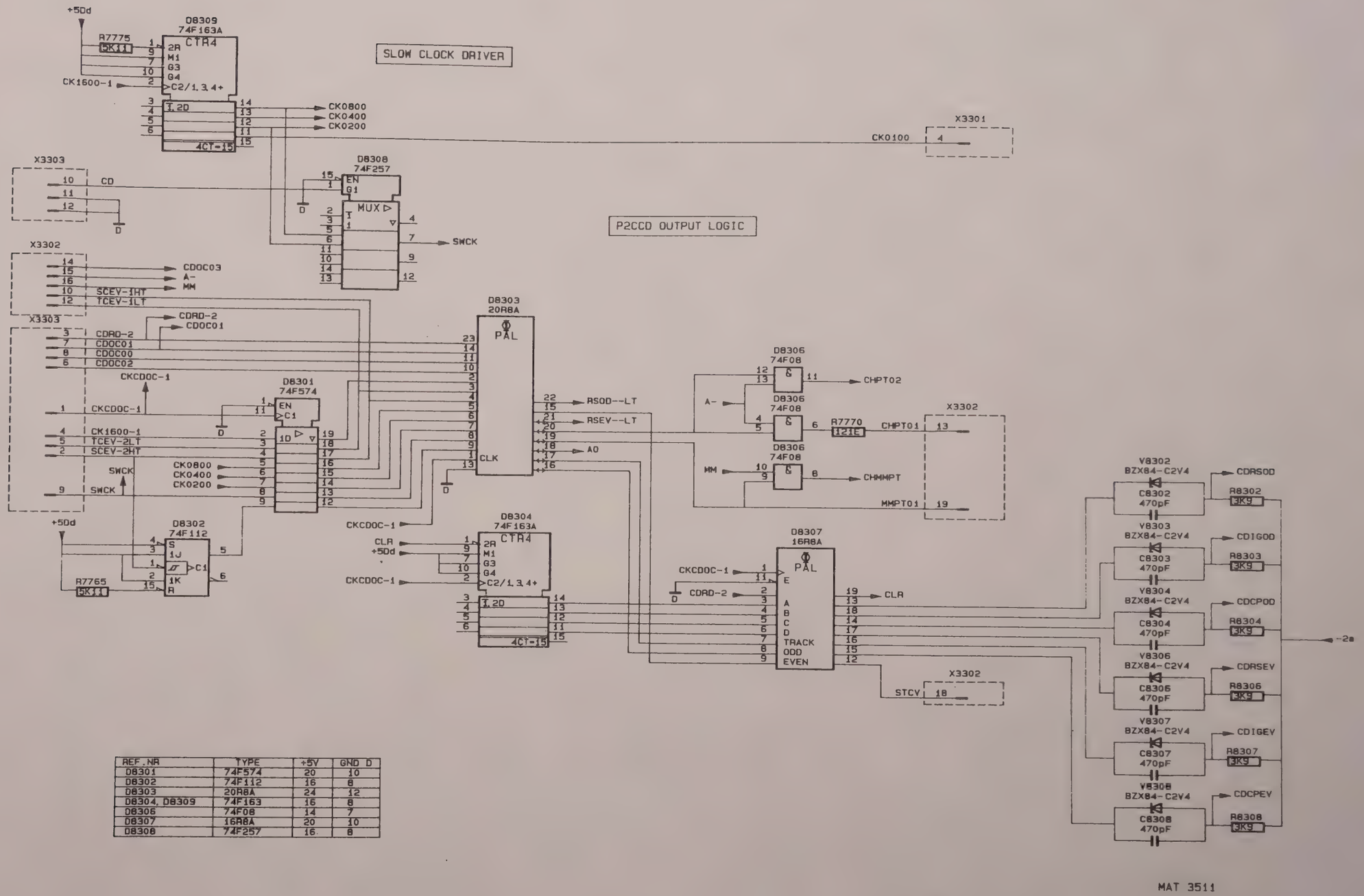
REF.NR	TYPE	-2s	+3s	+7Vf	-7Vf	A GND	+5s	-5s
D8311, D8331	HCT4066	7	14					
D8321	HCT4052					8	16	7
N8311, N8331, N8401	HA3-2525			7	4			

Figure 8.33.25 Unit A33 - P^2CCD - p.c.b. lay-out.



REF.NR	TYPE	-2a	+3a	+7Vf	-7Vf	A GND	+5a	-5a
D8401	HCT4051	7				8	16	
D8351, D8371	HCT4066	7	14					
D8361	HCT4052					8	16	7
N8351, N8371	HA3-2525			7	4			
N8411	HA3-2525			7	4			

Figure 8.33.26 Unit A33 - P^2CCD - circuit diagram.



REF.NR	TYPE	+5V	GND D
D8301	74F574	20	10
D8302	74F112	16	8
D8303	20R8A	24	12
D8304, D8309	74F163	16	8
D8306	74F08	14	7
D8307	16R8A	20	10
D8308	74F257	16	8

Figure 8.33.27 Unit A33 - P^2CCD - circuit diagram.

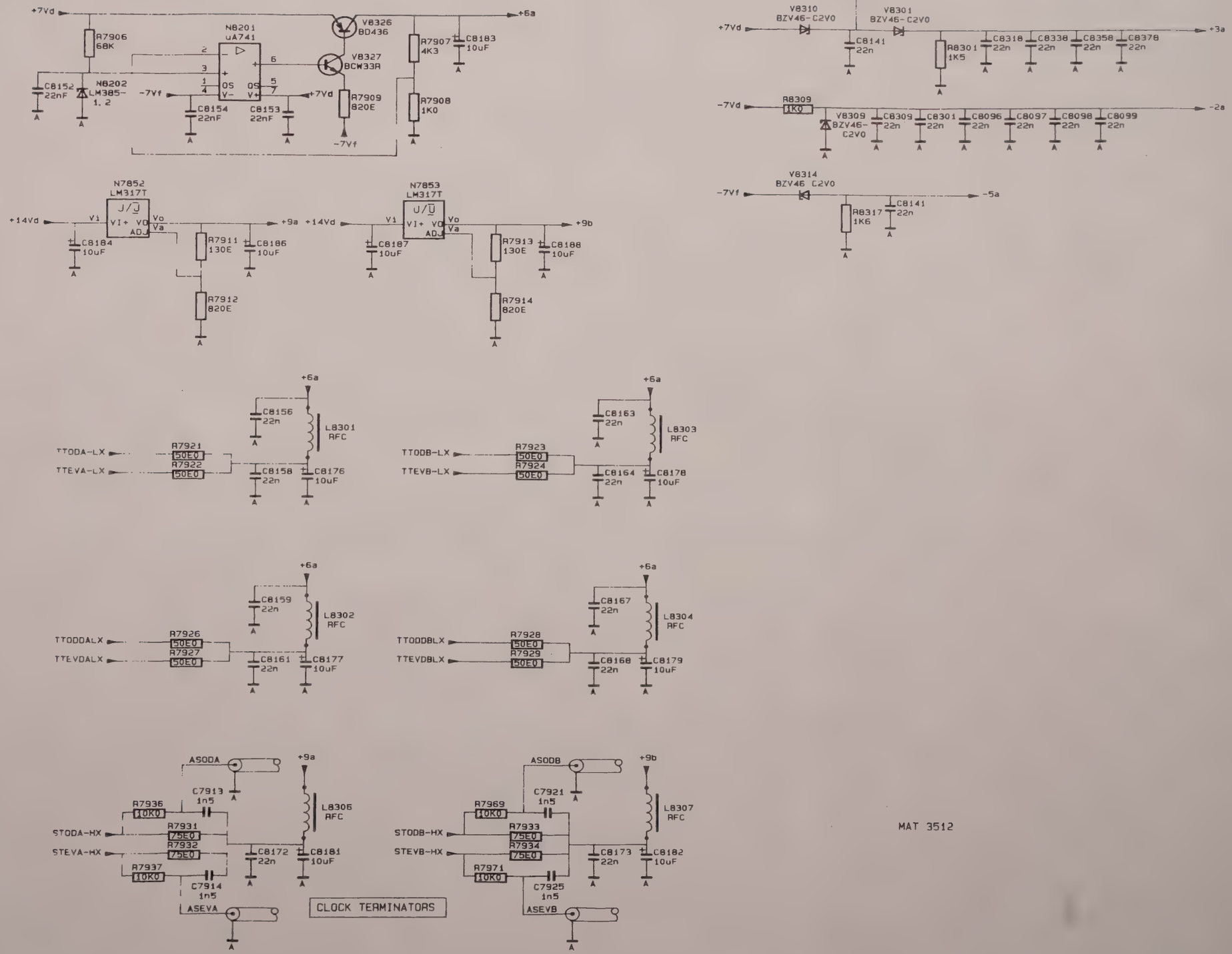
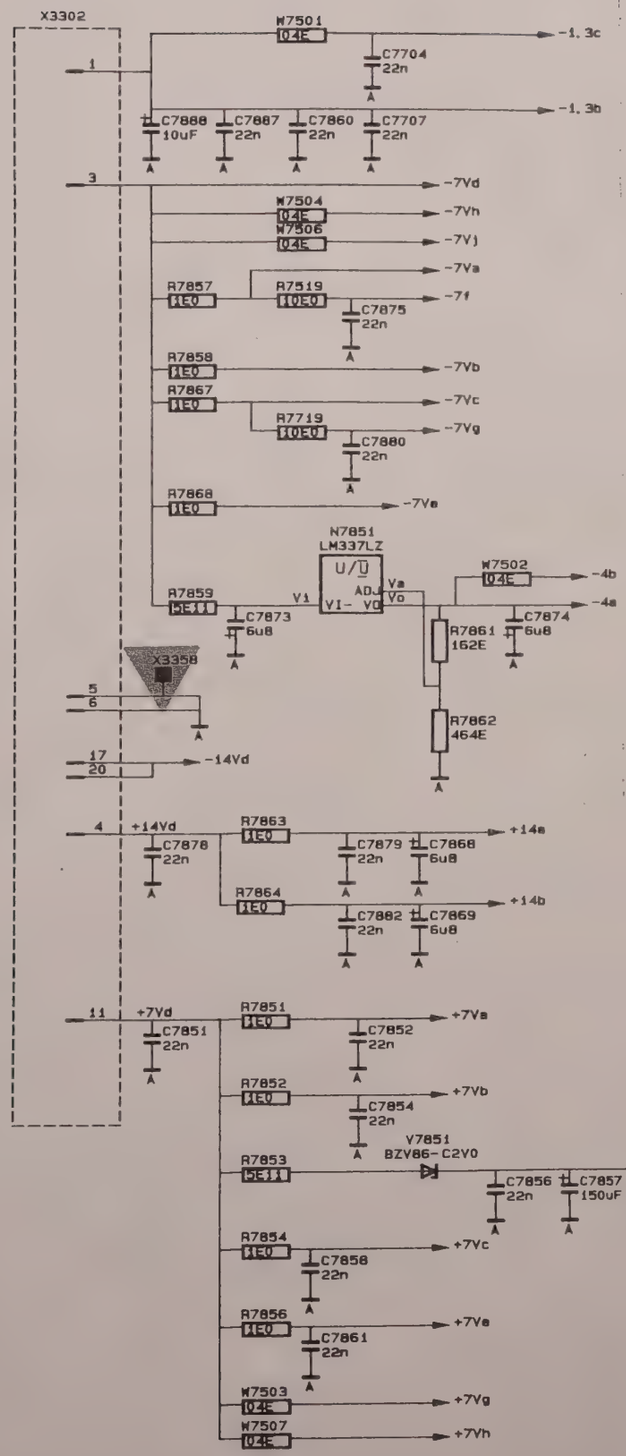
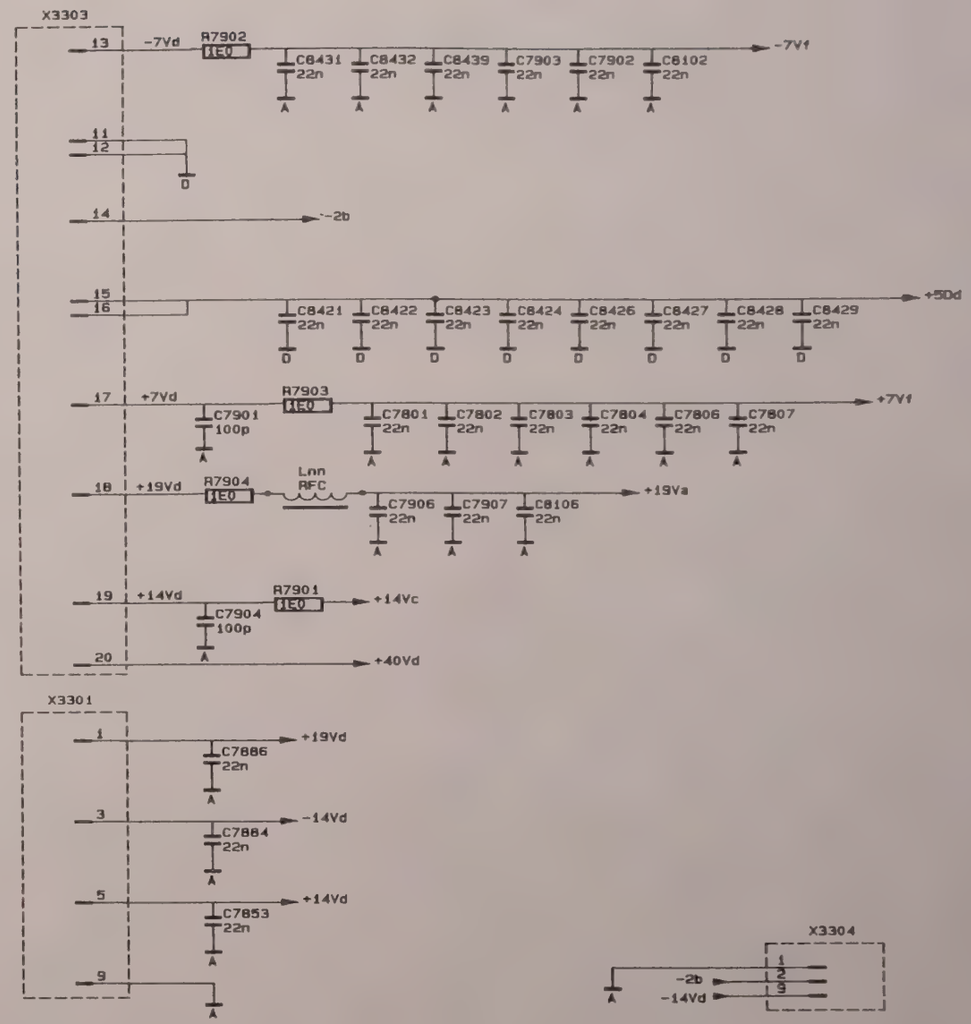


Figure 8.33.28 Unit A33 - P^2CCD - circuit diagram.

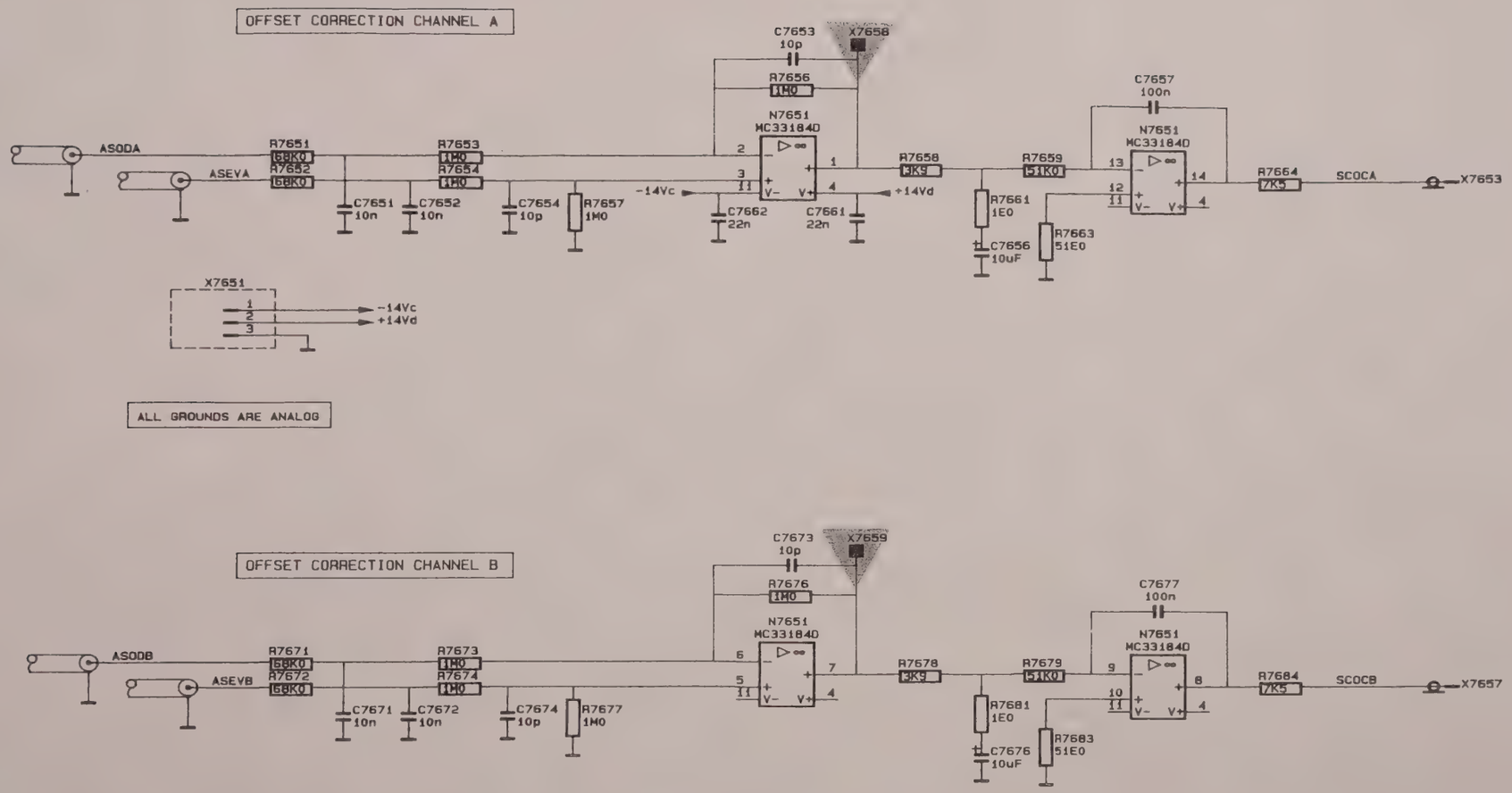
MAT 3512





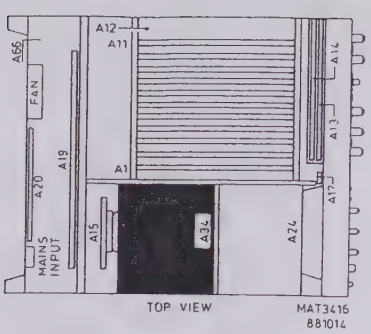
MAT 3513

Figure 8.33.29 Unit A33 - P^2CCD - circuit diagram.



MAT 3677

Figure 8.33.30 Unit A33 - P^2CCD - circuit diagram.



CONTENTS

8.34.1 General information..... 8.34-1
8.34.2 The fast sample clock generator..... 8.34-1
8.34.3 The delta-t circuit..... 8.34-2
8.34.4 Signal name list..... 8.34-3

8.34.1 General information

This unit consists of two parts:

- a fast sample clock generator
- a delta-t circuit

The Mini Frequency Doubler unit A48 is also described in this section.

8

8.34.2 The fast sample clock generator

The fast sample clock generator consists of two crystal oscillators (100 MHz and 125 MHz), which can be enabled by the signals EN200MLT or EN250MLT respectively. Only one crystal oscillator operates at a time. The signal from the operating cristal oscillator (MACK) is led to the Mini Frequency Doubler unit A48. This unit doubles the frequency to 200 MHz resp. 250 MHz.

The frequency doubler operates as follows:

The input signal MACK is attenuated by the resistors R8701 and R8702. The signal amplitude is now just sufficient to make transistor V8701 conducting on the positive peaks.
The output signal of V8701 is applied to a filter, consisting of L8701, C8701 and C8702. The filter resonates at a frequency of 250 MHZ, a higher harmonic frequency of MACK.
If the 100 MHz oscillator is active, C8703 is switched parallel by transistor V8707, which brings the resonance frequency of the filter to 200 MHz.
Via a buffer stage, consisting of the circuit around FET V8702 and transistor V8703, the output signal FSCK is generated.
An amplitude detector (V8708, V8709, C8706 and R8711) detects the amplitude of the signal. The output signal of the amplitude detector is fed back to the base of transistor V8701 via opamp N8701, to stabilise the signal amplitude.
If the signal amplitude increases, the voltage on the base of V8701 will decrease. This brings V8701 less in conduction, which results in a decreasing signal amplitude.
The output signal FSCK is fed to the CCD LOGIC + FAST TIME BASE DIVIDER on the CCD LOGIC unit A26.

In the two fastest P^2CCD mode time base settings (100 and 200 ns/div) the 125 MHz crystal oscillator is enabled, which results in an FSCK of 250 MHz.
In the other P^2CCD mode time base settings (500 ns/div ... 200 us/div) and in the RANDOM SAMPLING mode time base settings (5 ns/div ... 50 ns/div), the 100 MHz crystal oscillator is enabled, which results in an FSCK of 200 MHz.
The CCD LOGIC + FAST TIME BASE DIVIDER divides this frequency down to the desired sample and transport clocks for the P^2CCDs in the various time base settings.
In all other time base settings, no crystal oscillator is enabled.

8.34.3 The delta-t circuit

The function of the delta-t circuit is to measure the time between a trigger signal and the sample clock pulse. The times that are to be measured vary from 100 ps in the Random Sampling mode to 10 us in the P^2CCD mode with Max-Resolution on. The used principle is current integration.
DAC N8511 is a serial DAC which gets its data from the microprocessor via the management unit. The data (DB15-1) are clocked in by a clock signal (CKSEDA). As soon as all bits are clocked in a latch enable clock (LDDTCK) is given, after which the data are converted.
The DAC gives an output current (Iout, pin 22), which is converted to a voltage by opamp N8512.
The output voltage (pin 6) can be adjusted by potentiometer R8602 (GAIN).
This voltage is converted to a current (DTIGCU) by opamp N8513 and associated components.
This current is led to a symmetrical circuit, which discharges (integrate) or charges (reset) capacitor C8501. In the hold phase capacitor C8501 is neither charged nor decharged.
The discharge current is determined by DTIGCU. The circuit is controlled by two signals, coming from the mini CCD logic (unit A49) on unit A26:

- a start signal (STDTSWHE and STDTSWLE)
- a stop signal (SPDTSWHE and SPDTSWLE)

The truth table is:

Phase	STDTSWHE (start)	SPDTSWHE (stop)
Reset	0	0
Integrate	1	0
Hold	1	1

x = don´t care

The voltage capacitor C8501 is buffered by FET V8506 and is led via Opamp N8502 to the input of ADC N8503.
The going low of SPDTSWLE (start of hold phase) generates a pulse via N8501 at pin 18 of the ADC. The conversion is started.
The data from the ADC (DTADDA) are clocked by a clock signal(DTADCK) into a serial parallel converter on the management unit A25.
When all data are send to the management unit, a strobe signal is

The reset level of capacitor C8501, which is a reference level, is determined by the reference output voltage of the ADC (pin 24) via opamp N8506 and the circuit around transistors D8501 and V8518.

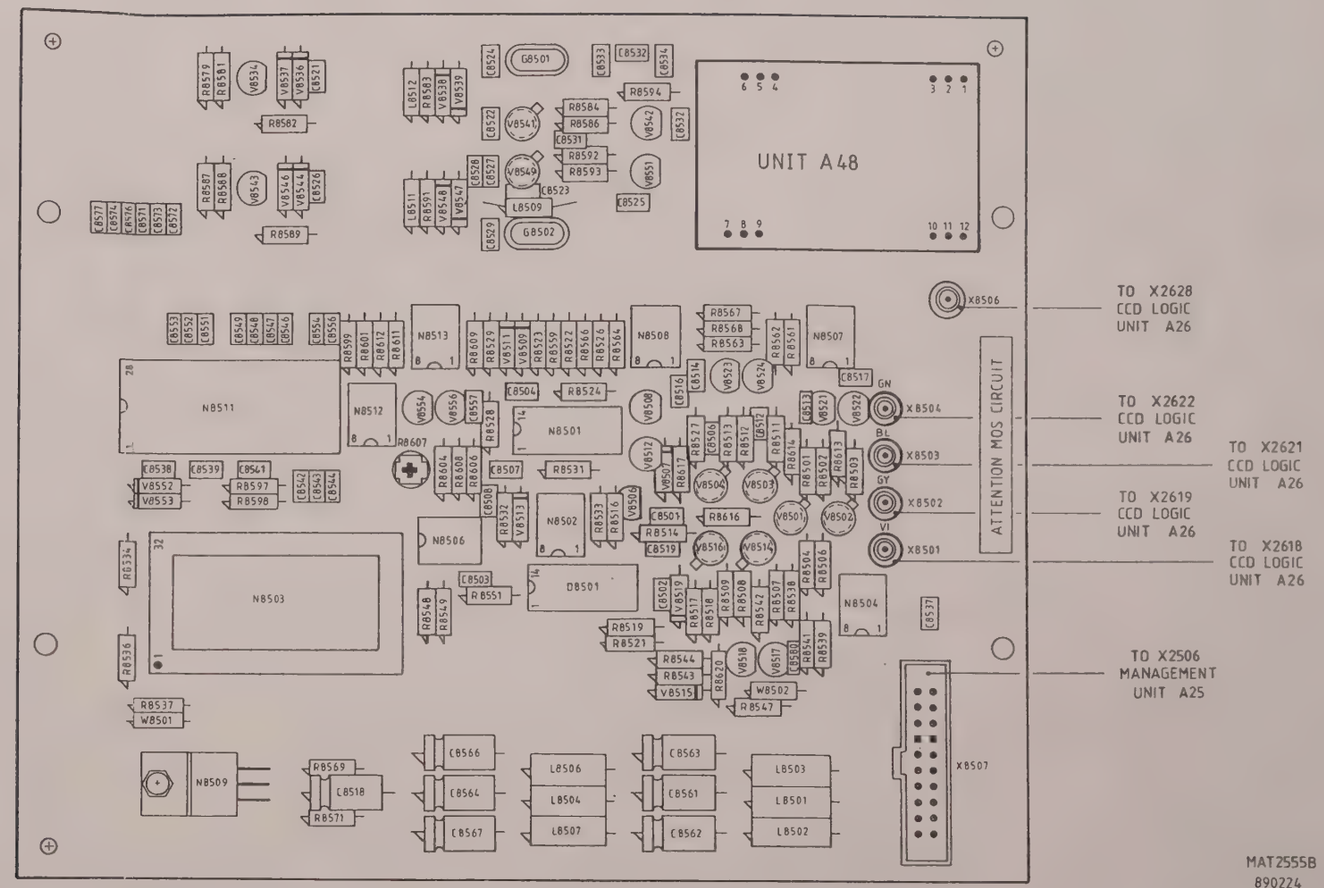
RESUMED: The delta-t circuit is of a time measuring circuit based on integration of a current. The time range that can be measured, is determined by the amplitude of this current. The amplitude of this current is determined by the microprocessor via DAC 8511.
The measured time is calculated by the microprocessor by using the integration voltage via ADC N8503.

NOTE: If the GAIN adjustment (R8602) is not set correctly in the Random Sampling mode (5 ns...50 ns/div), then a signal on the screen shows discontinuities. These discontinuities appear every 20 ns, independent of the time base setting.
The discontinuities may be a gap (gain too low) are a vertical step (gain too high).

8.34.4 Signal name list

UNIT A34 (including MINI UNIT A48)

Signal name	Description	Signal source	Signal destination(s)
CKSEDA	Clock serial data	A25	-
DB15-1	Data bus 15-1	A25	-
DTADCK	Delta-t ADC clock	A34	A25
DTADDA	Delta-t ADC data	A34	A25
DTADST	Delta-t ADC status	A34	A25
DTIGCU	Delta-t integration current	A34	A34
EN2ØØMLT	Enable 2ØØ MHz	A25	-
EN25ØMLT	Enable 25Ø MHz	A25	-
FSCK	Fast sample clock	A34	A26
IGOT	Integrator output	A34	A34
LADTCK	Latch delta-t clock	A25	-
MACK	Master Clock	A34	A49
RVIG	Reference voltage Integrator	A34	A34
SPDTSWHE	Stop delta-t sweep	A49	-
SPDTSWLE	Stop delta-t sweep	A49	-
STDTSWHE	Start delta-t sweep	A49	-
STDTSWLE	Start delta-t sweep	A49	-



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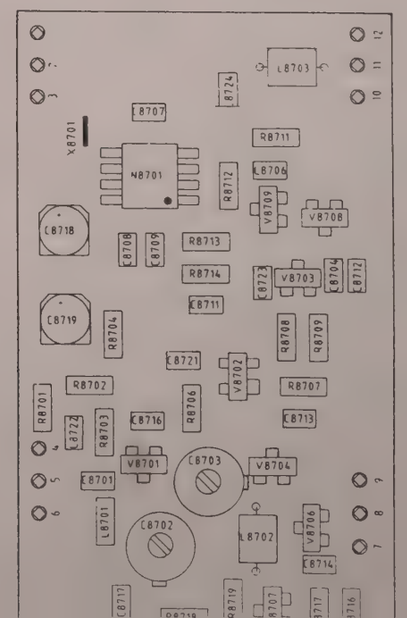


TYPE	MARKING CODE
BAV70	A4
BAW56	A1
BCW30	C2
BCW30R	C5
BCW33	D3
BCW33R	D6
BFS12	S8
BFQ19	FF
BFR92	P1
BFR92R	P4
BFT92R	W4

Figure 8.31.2 Unit A31 - EXT TRIG INPUT - circuit diagram.

X4703
12 → TREV/5
7 → TREV/50
2 → TREVLV

EVENTS / EXT.CLK. X4 EVENTG C4806 4p7

TREV/5 R4839 10K
TREV/50 R4847 10K
TREVLV

L4801 4p7 R4801 120E
R4802 22E
V4807 BAS45 -14Vc
R4803 100K
C4802 15p

+5Vd R4804 100E
V4801 BF512
C4804 22n
V4803 BFR92R
R4707 100K
R4806 150E
-14Vc

+14Vc R4834 2K7
V4819 BCW33
R4836 388E
R4837 1K2
C4816 22n
+14Vc V4821 BFR92R
R4841 47E
+14Vd V4822 BFR92R
R4838 180E
R4850 560E
R4851 100E
R4852 560E
I.F. RESPONSE
R4855 56E

CAPACITIVE ATT.

R4862 10K
R4866 82K
R4864 27K
C4803 22n
V4820 BCW30R
R4863 27K
-14Vc

+14Vc R4842 2K7
V4826 BCW33R
R4843 180E
R4844 1K2
C4817 22n
V4824 BFR92
R4848 47E
+14Vd V4823 BFR92R
R4853 100E
NOT USED
R4860 56E
C4865 1n
R4846 180E

R4871 10K
R4868 82K
R4867 27K
C4812 22n
V4831 BCW30
R4869 27K
-14Vc
R4813 100K
C4811 15p
R4812 72E
+5Dc R4814 100K
C4813 22n
C4807 2p7
R4808 180E
R4811 15E
C4809 4p7
V4806 BF512
R4816 150E
V4807 BFR92
R4809 72E
C4808 22p
R4817 100K
-14Vc

V4827 BAV70
V4804 BAV70
R4829 33E
-14Vc
R4810 47E
V4809 BFR92
V4808 BAW56
R4819 39E
R4821 39E
C4810 5p6
C4814 1p
SUMMATION AMPLIFIER

+5Dc R4856 72E
R4857 56E
V4810 BFQ19R
C4823 22n
C4824 22n
V4817 BFT92
-7Vb
+5Dc R4858 33E
R4859 39E
-7Vb
X4801 EVSGBM TO X7013 UNIT A3Z
R4861 39E

R4822 100E
V4812 BAW56
R4824 220E
V4811 BFT92
R4826 1K
-14Vc
R4823 72E
C4820 22n
C4821 22n
V4813 BFR92
R4827 39E
R4828 1K2
C4822 1n

COMPARATOR
N4801 UA714
+5Vd -14Vd
C4848 22p
C4849 220p
R4883 196K
R4884 23K7
R4885 26K
V4838 BSV88
V4837 BSV88
R4886 10K
C4847 10n
V4846 BAW62

X4802
R4877 1M
V4832 BAW62
V4833 BAW62
R4897 1M
R4898 1M
C4846 10n

N4702 UA324
VREF
TREV/50
+5Vd
-14Vd
R4888 10K
V4842 BC558B
V4841 BSV80
R4887 10K
C4851 10n
-14Vd

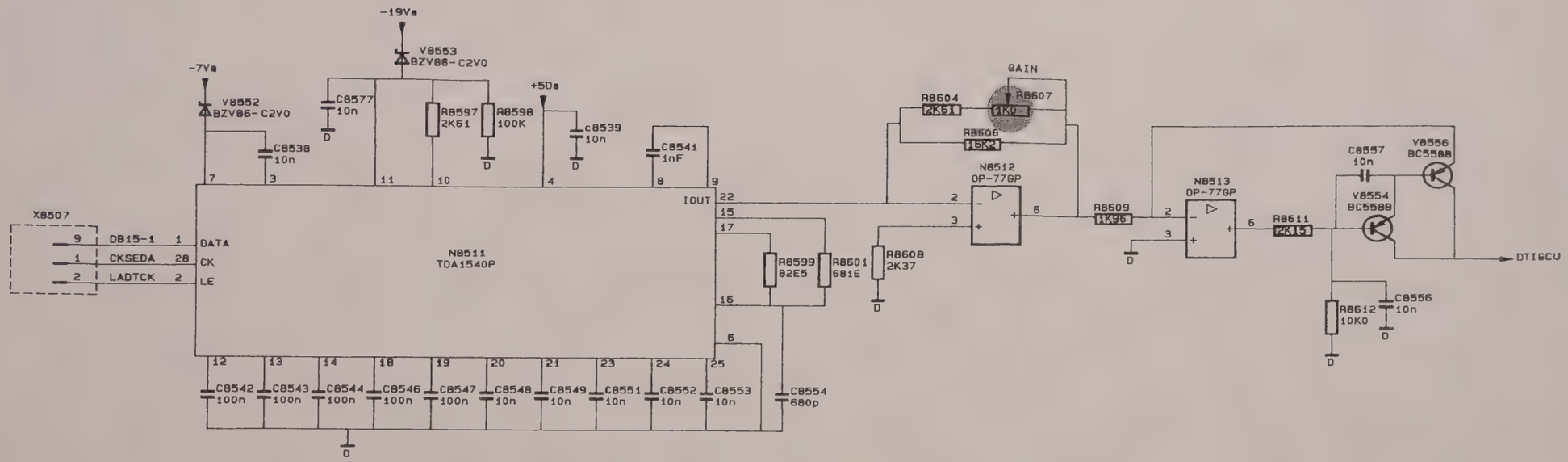
+14V R4872 100E C4837 68U C4733 22n C4834 22n +14Vc
+14V R4849 270E C4831 +14Vd
-14V R4896 10E C4858 68U C4754 10n -14Vc
-14V R4876 100E C4841 68U C4826 22n C4827 22n C4836 22n C4861 22n -14Vd
-7V R4874 10E C4839 68U C4828 22n C4832 22n -7Vb
+5D R4873 10E C4838 68U C4829 22n +5Dc
+5D R4894 10E C4857 68U C4754 10n +5Dd

SURFACE MOUNTED SEMICONDUCTORS

TYPE	MARKING CODE
BAV70	A4
BAW56	A1
BCW30	C2
BCW30R	C5
BCW33R	D6
BF512	S8
BFQ19R	BFQ19R
BFR92	P3
BFR92R	P4
BFT92	W1

CODE
BFQ19R

MAT 2613



REF.NR	TYPE	SUPPLY AND GROUND PIN CONECTIONS					
		-19Va	+14Va	-14Va	-7Va	+5Da	DIGITAL GND
N8511	TDA1540P	M			M	M	M
N8512	OP-77GP		7	4			
N8513	OP-77GP		7	4			

MAT 35 17

Figure 8.34.4 Unit A34 - CLOCK - circuit diagram.

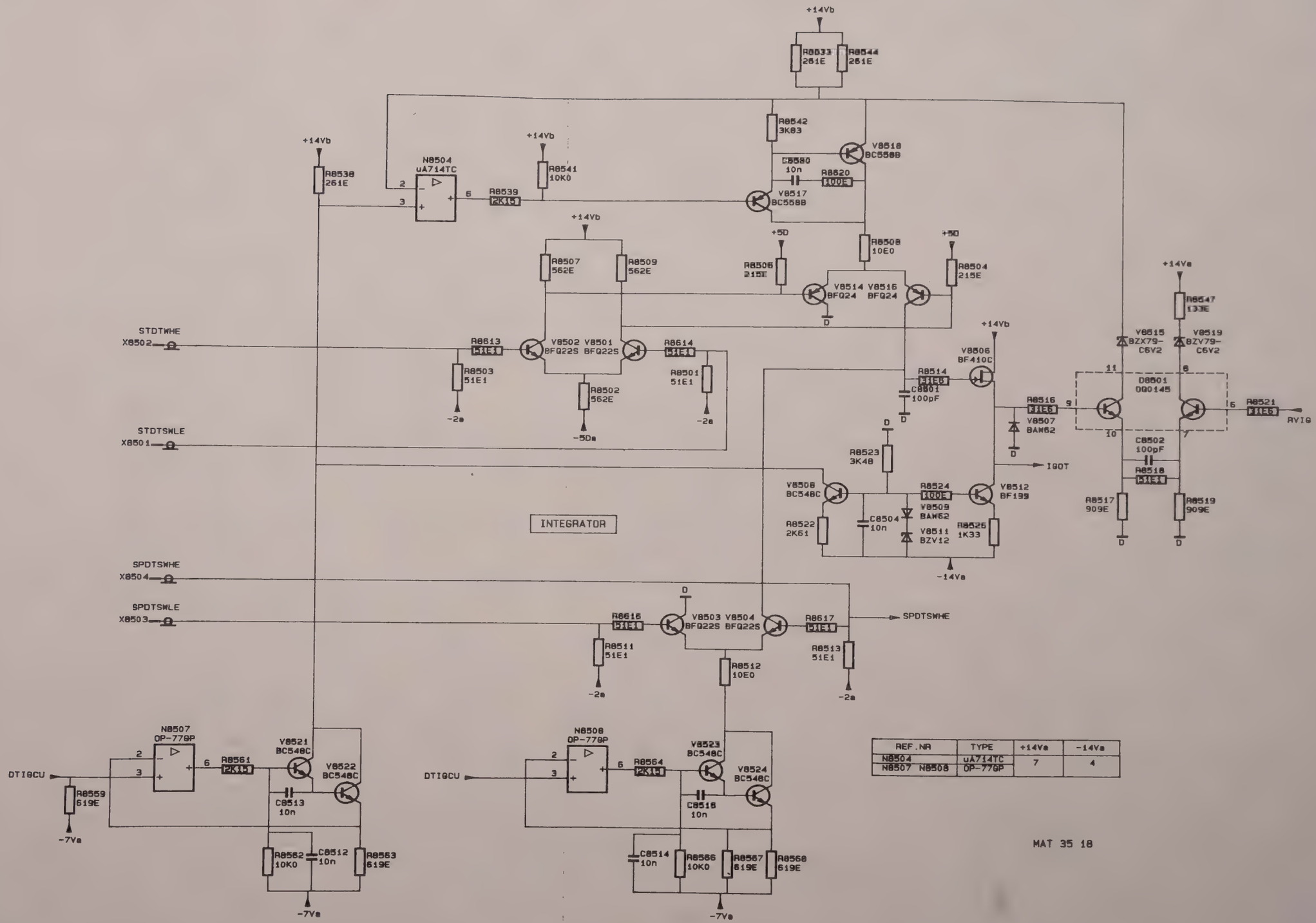
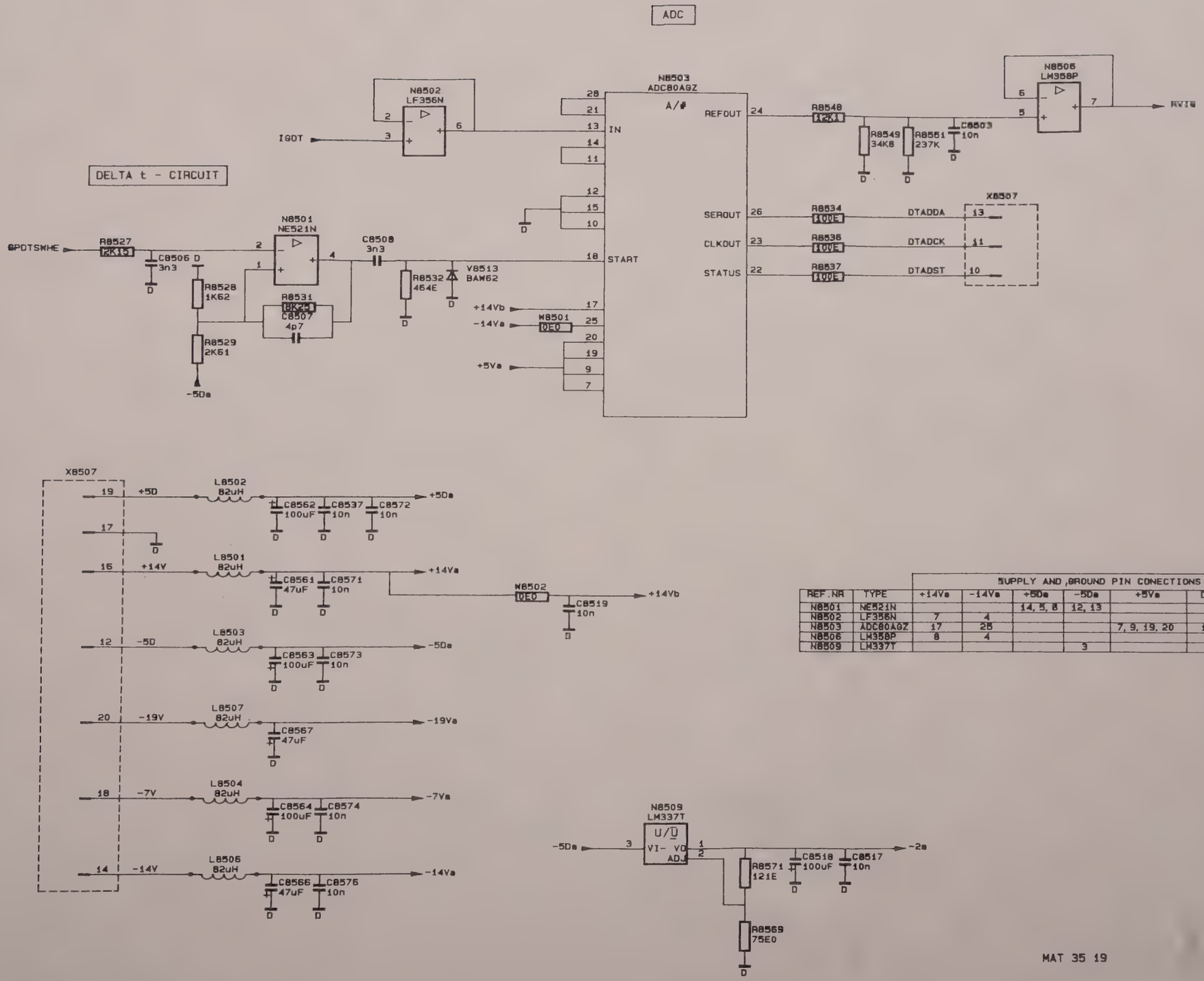


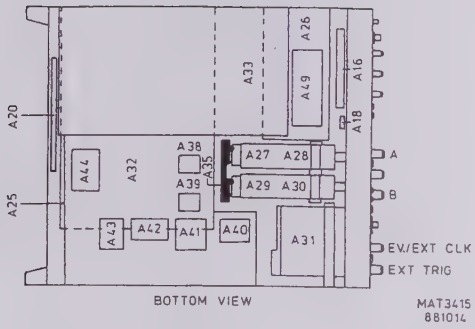
Figure 8.34.5 Unit A34 - CLOCK - circuit diagram.



		SUPPLY AND ,GROUND PIN CONECTIONS					
REF.NR	TYPE	+14Va	-14Va	+5Da	-5Da	+5Va	DIGITAL GND
N8501	NE521N			14, 5, 8	12, 13		7, 8, 11
N8502	LF356N	7	4				
N8503	ADC80A8Z	17	25			7, 9, 19, 20	12, 15, 10,
N8506	LM358P	8	4				
N8509	LM337T				3		"

Figure 8.34.6 Unit A34 - CLOCK - circuit diagram.

UNIT A35 - ATTENUATOR ADAPTION



CONTENTS

8.35.1 Description of the adaption unit A35..... 8.35-1
8.35.2 Signal name list..... 8.35-1

8.35.1 The adaption unit is an interconnection unit between the channel A and B attenuators (units A27...A30), the offset adaptation unit A50 and the management unit A25.
Two potentiometers R7451(A) and R7454(B) are also present to adjust the DC offset of both LF attenuators.
Also four capacitors are present to reduce interference on the probe information lines and on the 50-Ohm protection lines.

8.35.2 Signal name list

UNIT A35

Signal name	Description	Signal source	Signal destination(s)
ACDCA	AC/DC A	A25	-
ACDCB	AC/DC B	A25	-
ATSWØA	Attenuator switch Ø A	A35	A27,A28
ATSWØB	Attenuator switch Ø B	A35	A29.A30
ATSW1A	Attenuator switch 1 A	A35	-
ATSW1B	Attenuator switch 1 B	A35	-
AT1A	Attenuation x1 A	A25	-
AT1B	Attenuation x1 B	A25	-
AT1ØA	Attenuation x1Ø A	A25	-
AT1ØB	Attenuation x1Ø B	A25	-
AT1ØØA	Attenuation x1ØØ A	A25	-
AT1ØØB	Attenuation x1ØØ B	A25	-
HFXA	High frequency A	A27	-
HFXB	High frequency B	A29	-
LFXA	Low frequency A	A28	-
LFXB	Low frequency B	A30	-
OSA	Offset A	A25	A50
OSB	Offset B	A25	A50
OSBIAAXA	Offset bias analog A	A35	A28
OSBIABXA	Offset bias analog B	A35	A30

Signal name	Description	Signal source	Signal destination(s)
PRIFA-XA	Probe indication A analog	A27+A28	-
PRIFB-XB	Probe indication B analog	A29+A30	-
PT5ØA-LT	Protect 5Ø-Ohm A	A27	-
PT5ØB-LT	Protect 5Ø-Ohm B	A29	-
TM5ØA	Termination 5Ø-Ohm A	A25	-
TM5ØB	Termination 5Ø-Ohm B	A25	-
ZEA-HX	Zero A	A25	-
ZEB-HX	Zero B	A25	-
ZEA-LX	Zero A	A27	-
ZEB-LX	Zero B	A29	-

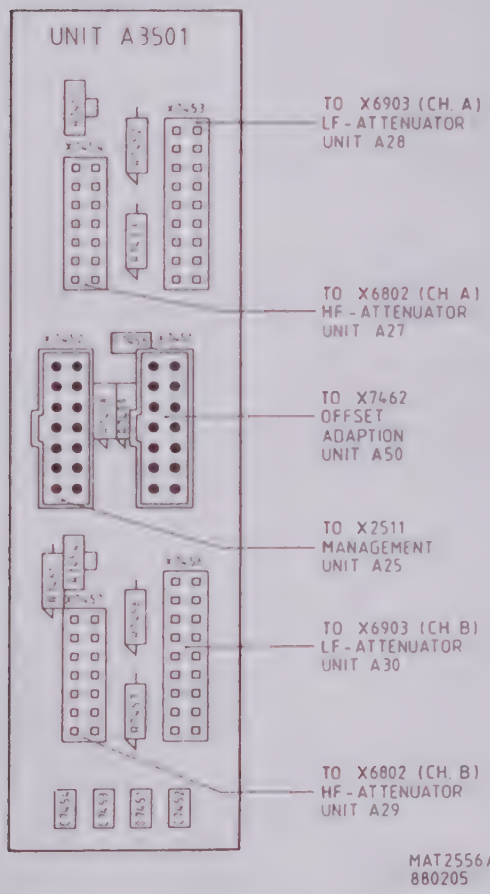


Figure 8.35.1 Unit A35 - ATTENUATOR ADAPTION - p.c.b. lay-out.

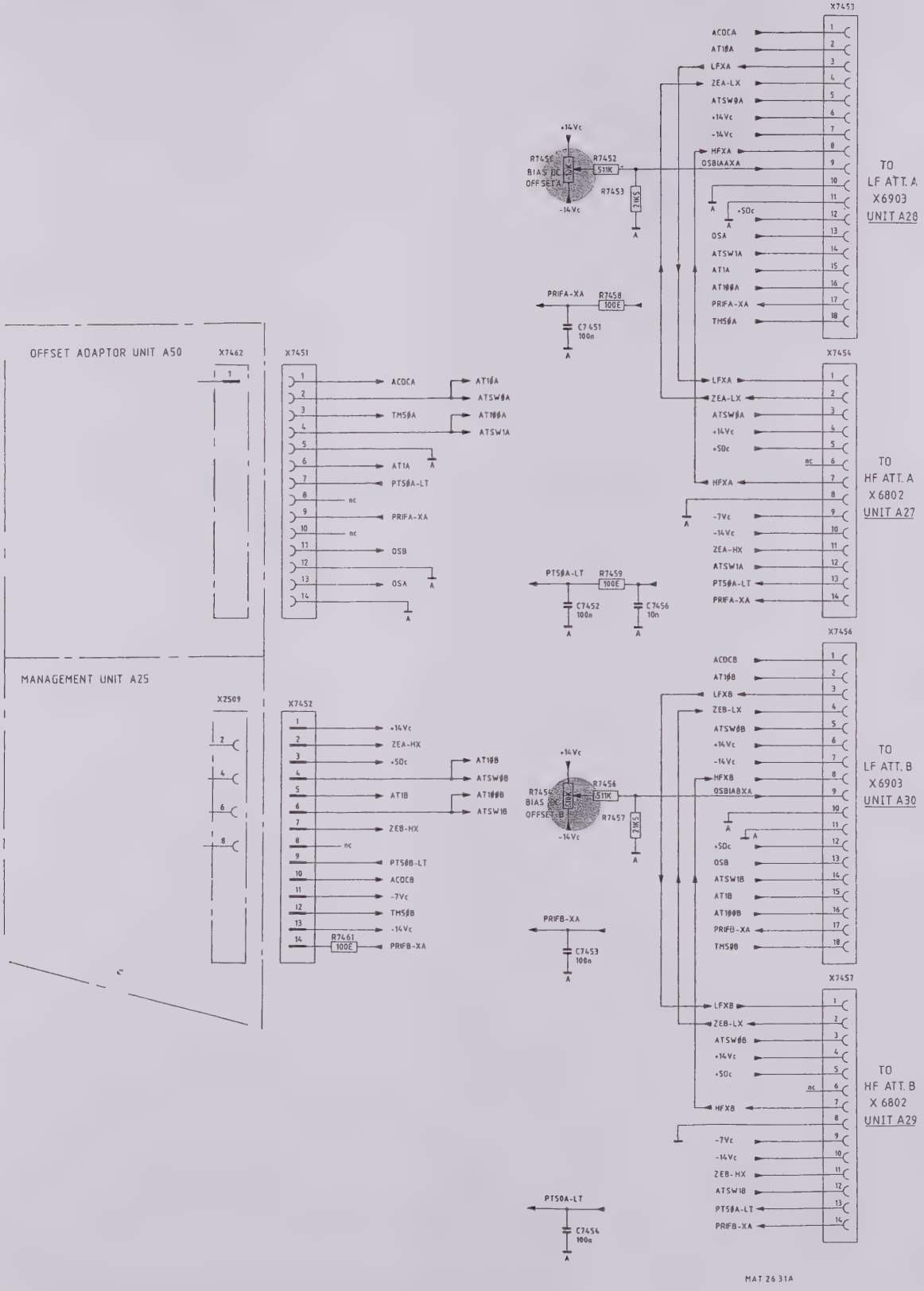
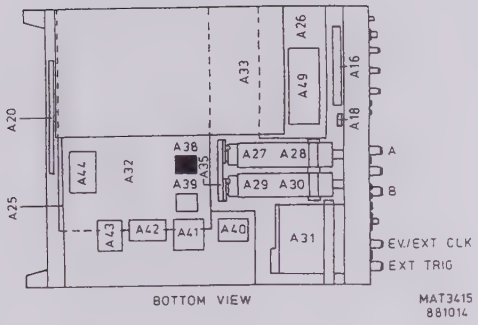


Figure 8.35.2 Unit A35 - ATTENUATOR ADAPTION - circuit diagram.

UNIT A38 - MINI TRIGGER SELECT A



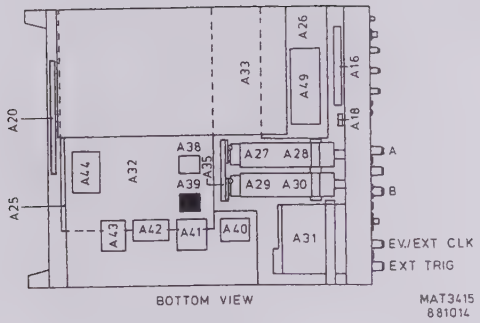
CONTENTS

8.38.1 General information..... 8.38-1

8.38.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.32.

UNIT A39 - MINI TRIGGER SELECT B



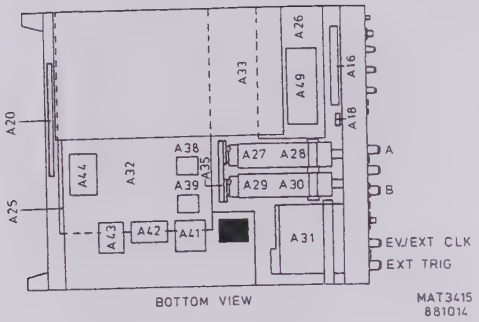
CONTENTS

8.39.1 General information..... 8.39-1

8.39.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.32.

UNIT A40 - MINI TRIGGER FILTER UNIT



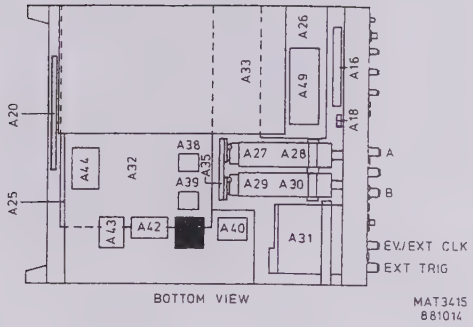
CONTENTS

8.40.1 General information..... 8.40-1

8.40.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.32.

UNIT A41 - MINI TRIGGER AMPLIFIER UNIT



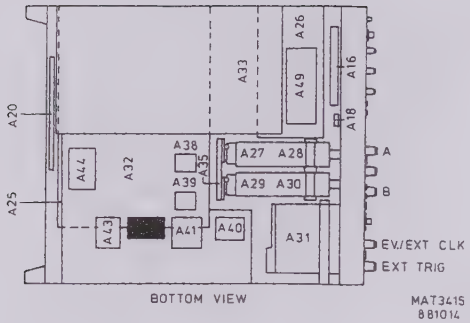
CONTENTS

8.41.1 General information..... 8.41-1

8.41.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.32.

UNIT A42 - MINI TRIGGER LOGIC



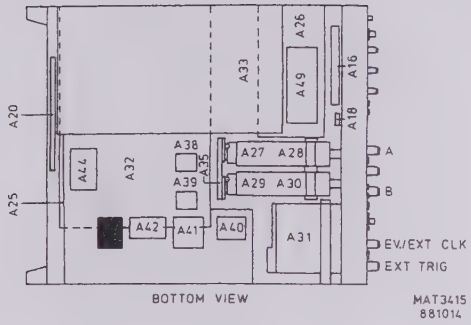
CONTENTS

8.42.1 General information..... 8.42-1

8.42.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.32.

UNIT A43 - MINI EVENTS AMPLIFIER UNIT



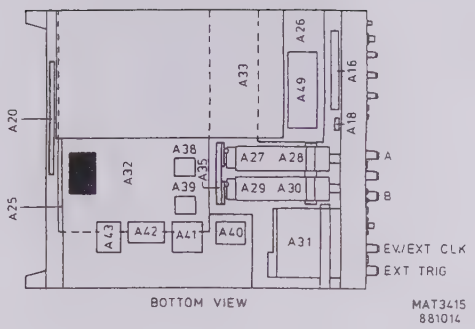
CONTENTS

8.43.1 General information..... 8.43-1

8.43.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.32.

UNIT A44 - MINI VERTICAL AMPL. PROC. UNIT



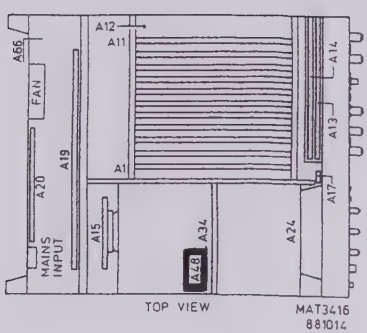
CONTENTS

8.44.1 General information..... 8.44-1

8.44.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.32.

UNIT A48 - MINI FREQUENCY DOUBLER



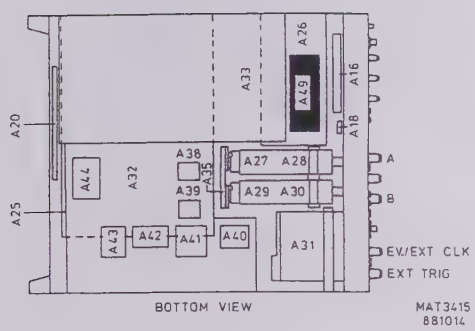
CONTENTS

8.48.1 General information..... 8.48-1

8.48.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.34.

UNIT A49 - MINI CCD LOGIC



CONTENTS

8.49.1 General information..... 8.49-1
8.49.2 Circuit description..... 8.49-1
8.49.3 Signal name list..... 8.49-3

8.49.1 General

The mini CCD logic is an SMD unit, which can be found on unit A26; the CCD logic.
It consists of:

- the peak detector reset logic
- a TTL/ECL converter
- the aliasing detection circuit
- the reset auto trigger logic
- the trigger sync logic

8.49.2 Circuit description

The PEAK DETECTOR RESET LOGIC generates 20 ns reset pulses for the peak detectors on unit A33.
A reset pulse for the MIN peak detector is generated on the negative slope of D6403 pin 1. The pulse length is determined by the delay line on unit A26. A reset pulse for the MAX peak detector is generated on the negative slope of D6403 pin 19.
The reset pulses are only generated when MIN / MAX is on. In the P^2CCD mode (200 ns/div...200 us/div) the reset pulses are generated by SCEV and SCOD.
In the other modes the reset pulses are generated by RSMN and RSMX.
The generation of the reset pulses is controlled by the MMSLØ1 and MMSLØ2 signals according to the following truth table:

Time base range	MMSLØØ	MMSLØ1	Reset pulse from:
5 us/div...200 us/div	1	0	SCEV + SCOD
500 us/div...360 s/div	0	1	RSMN + RSMX
5 ns/div...360 s/div	1	1	None, MIN / MAX OFF

Gate D6401 pins 20, 12 and 13 is a TTL-ECL level converter for the SYSWTB signal.

The RESET AUTO TRIGGER circuit consists of a flip flop which is clocked by the TRSG signal. It can be enabled by the ENAURSLT signal. The output signal RSAUFF resets the AUTO TRIGGER logic on unit A26.

The ALIASING DETECTION detects if the sample frequency is lower than twice the trigger signal frequency.
The FSTB--HE signal is divided by two divide-by-two stages (D6406). The first stage can be bridged by D6409 (pins 18 and 5) under control of the DR signal via transistors V4616 and V4617.
The frequency of the signal at pin 11 of D6406 is always the sample frequency divided by four. This signal is applied to a two stage clocked circuit with D-type flip flops (D6404).
The open D input of the first stage is "Ø" (pin 6). On the first clock pulse of TRSG, the D input of the second stage (pin 15) becomes "1". On the next TRSG pulse output pin 14 becomes "1", unless the first stage is set earlier by the signal from pin 11 of D6406 via D6403 pins 24 and 12. So if the frequency of TRSG is twice or more of the quarter frequency of the sample clock then pin 14 of D6404 goes high. Due to the feedback line to pin 16 it stays high.
Then the ALID signal goes high. This is read by the microprocessor and it lights the pilot lamp on the front panel. The microprocessor also generates the RSALIDLT signal, which resets the circuit.Transistors V6401 and V6402 convert from ECL to TTL level.

In the time base range (200 us/div...5 ns/div) the DR signal is low. This resets the first stage of the divider (pin 17 of D6406) and it is bridged by D6409.
FSTB--HE is divided by two; unless flip flop D6406 is set via a set signal at pin 23.
This set signal comes from flip flop D6406 pin 8.
This flip flop is set by STAL (pin 3) and clocked back to the reset state by DTUF-2 (pin 5).
When DR is low the aliasing detection operates only between the STAL and the DTUF-2 signal, so only before the read out stroke of the P^2CCD mode.

In the time base range (360 s/div...500 us/div) the DR signal is high. Now both divider stages operate.
Because transistor V6418 conducts pin 3 of D6406 is high. The signals STAL and TDUF-2 have no influence. The FSTB--HE signal is divided by four. The aliasing detection operates continuously in the direct modes.

The TRIGGER SYNC LOGIC generates the start and stop signals for the delta-t circuit, a trigger signal for the auto trigger logic and an enable signal for the events counter and the trigger delay counter on unit A26.
When HDOF is low, a trigger signal (TRSG) sets the output of flip flop D6408 pin 14.
If it takes more than 10 usec before a trigger occurs, the flip flop is set by D6409 pin 14, due to the pulse circuit R6506...R6509 and C6417 and D6409.
The second trigger sets the flip flop in D6408 with output pins 7 and 8. Via transistors V6406...V6409, which convert from ECL to TTL level, the TRSGØ1 signals for the auto trigger logic on unit A26 are set.
When events is not selected via the ENEV--LT signal, the flip flop in D6408 with output pins 11 and 12 is also set by the second trigger. This sets the STDTSWHE and STDTSWLE signals via D6409 which start the delta-t circuit.

When events are selected, V6403 conducts. Now the STDTSW signals are not set by the second trigger, due to the high level at pin 1 of D6408. The base of V6409 is set at the ECL threshold level. Therefore the level of ENEVCNLT is determined by the level of D6408 pin 8 via V6408.
After the second triggerpulse this level goes low and ENEVCNLT goes low, which enables the events counter on unit A26 to count events.
When the events counter on unit A26 has counted down, the EVUF signal goes high. This sets STDTSWHE and STDTSWLE via D6401 and D6409.
The SPDTSWHE and SPDTSWLE signals, which stop the delta-t circuit on unit A34, are set via a two stage flip flop circuit consisting of D6407 and D6409.
In the time base range 100 us...360 s/div the DTPUSL signal is low. The stop signals are set by the first sample pulse of FSTB--HE at pin 20 of D6407. In the other time base ranges DTPUSL is high. Now the stop signals are set at the second pulse of FSTB--HE.

After the stop signals are set, the next pulse of FSTB--HE sets the outputs of flip flop D6407 pins 7 and 8. The trigger delay counter on unit A26 is enabled via ENTDCNLE.
This counter can also be enabled by the STTDCNLE signal, which is done during the zero correction stroke in the P^2CCD and the random sampling mode.

8.49.3 Signal name list

UNIT A49

Signal name	Description	Signal source	Signal destination(s)
ALID	Aliasing indication	A49	A26-A25
DR	Direct/Roll mode	A26	-
DTPUSL	Delta-t pulse select	A26	-
ENAURSLT	Enable Auto Reset	A26	-
ENEV--LT	Enable events	A26	-
ENEVCNLT	Enable events counter	A49	A26
ENTDCNLE	Enable trigger delay counter	A49	A26
EVUF	Events underflow	A26	-
FSTB--HE	Fast time base	A26	-
HDOF	Hold off	A5	-
MMSLØØ	Min/max select ØØ	A26	-
MMSLØ1	Min/max select Ø1	A26	-
MNDLIN	Min delay in	A26	-
MNDLOT	Min delay out	A49	A26
MXDLIN	Max delay in	A26	-
MXDLOT	Max delay out	A49	A26
RSALIDLT	Reset aliasing indication	A26	-
RSAUFF	Reset auto flip flop	A49	A26
RSMN	Reset min	A5	-
RSMNPD	Reset min peak detector	A49	A26-A33
RSMX	Reset max	A5	-
RSMXPD	Reset max peak detector	A49	A26-A33
SCEV	Sample clock even	A26	-
SCOD	Sample clock odd	A26	-
STAL	Start aliasing detection	A26	-

Signal name	Description	Signal source	Signal destination(s)
SPDTSWHE	Stop delta-t sweep	A49	A26-A34
SPDTSWLE	Stop delta-t sweep	A49	A26-A34
STDTSWHE	Start delta-t sweep	A49	A26-A34
STDTSWLE	Start delta-t sweep	A49	A26-A34
STTDCNLE	Start trigger delay counter	A26	-
SYSWTB	Synchronised slow time base	A5	-
SYSWTBHE	Synchronised slow time base	A49	A26
TDUF-2	Trigger delay underflow 2	A26	-
TRSG	Trigger signal	A32	-
TRSGØ1HT	Trigger signal Ø1	A49	Not used
TRSGØ1LT	Trigger signal Ø1	A49	A26

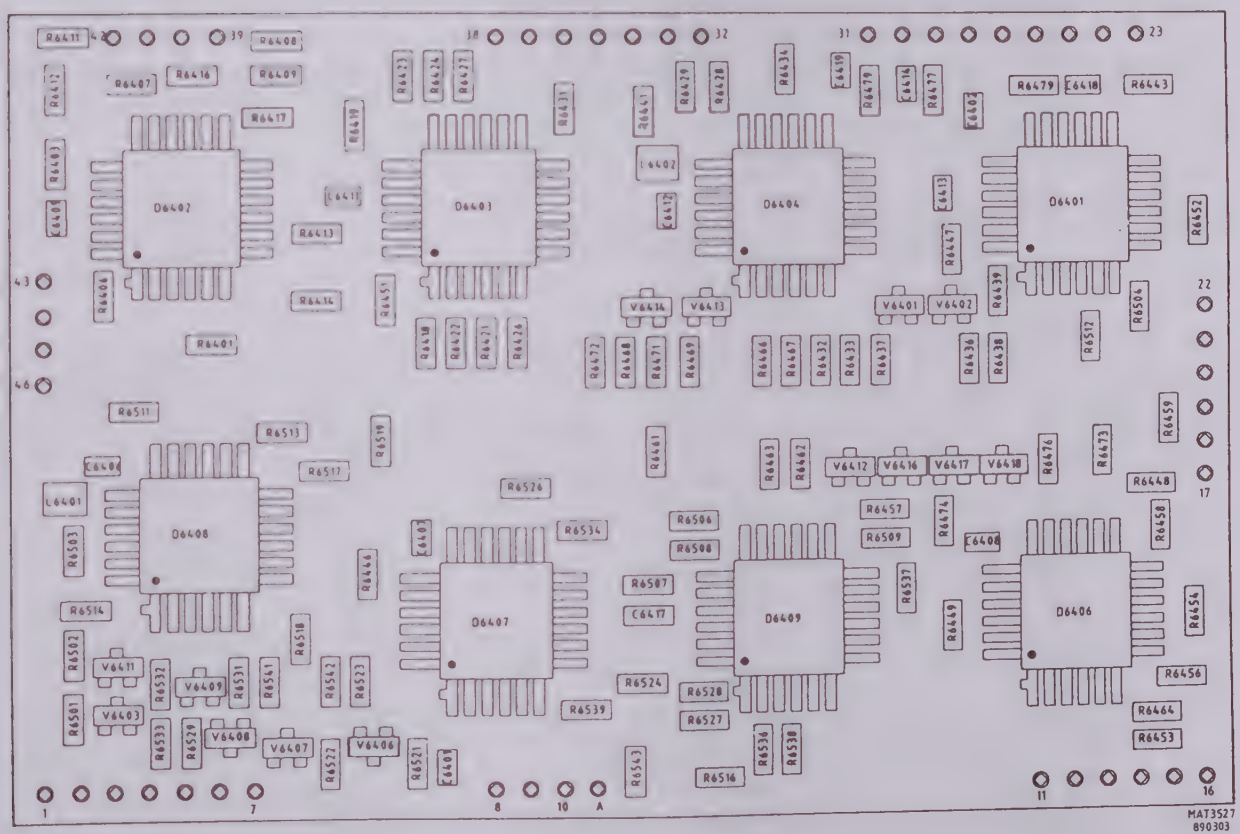
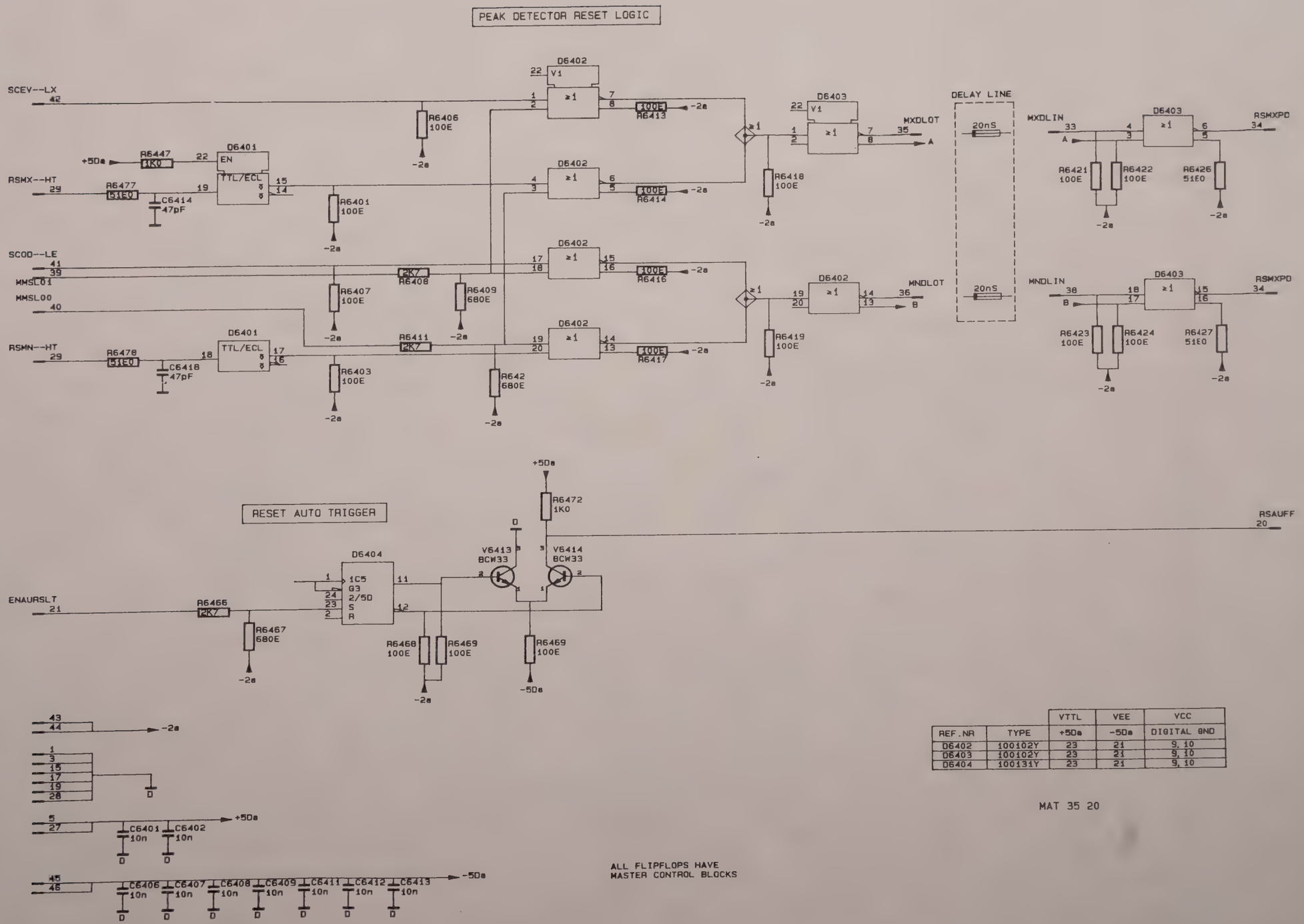


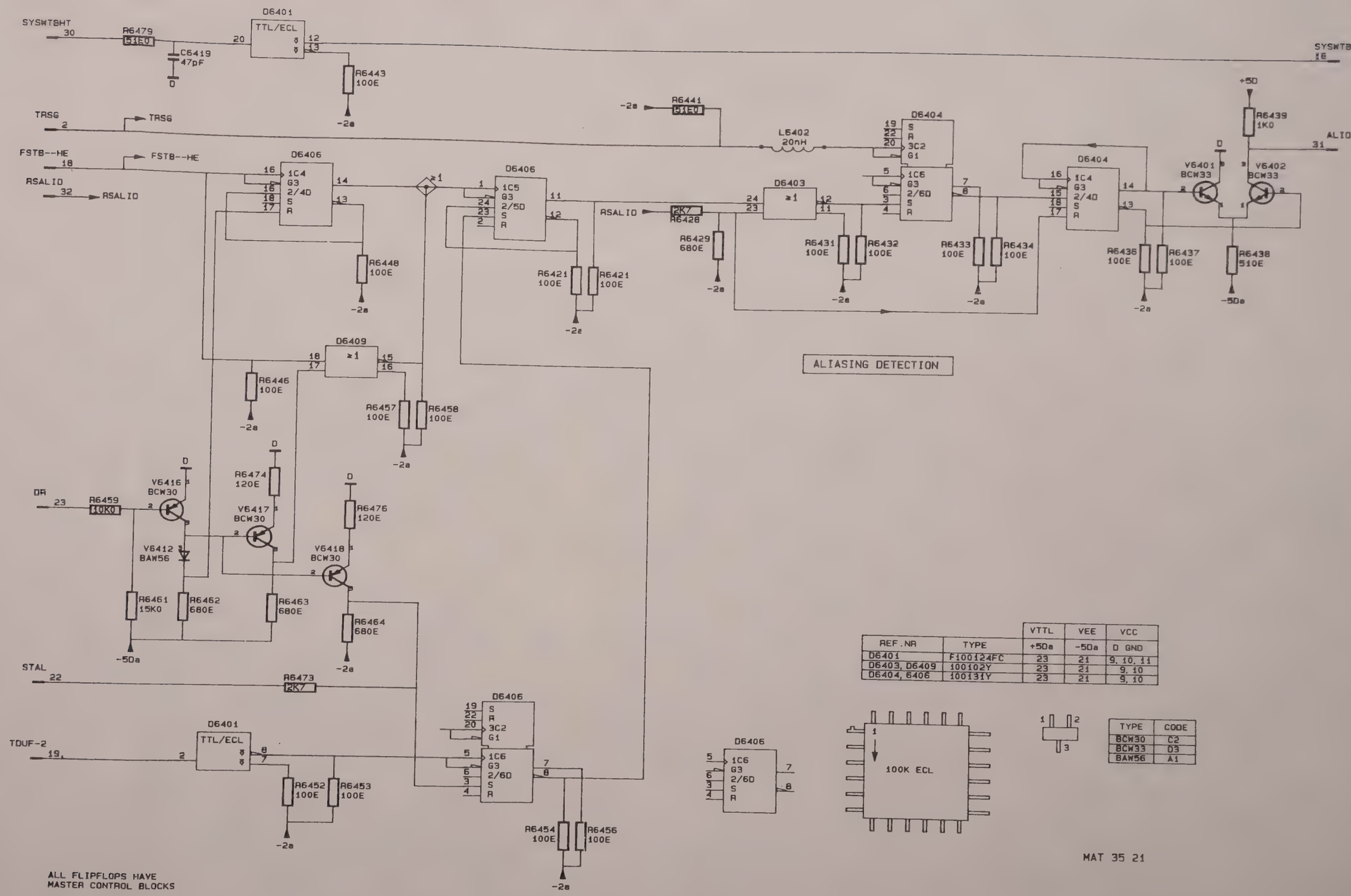
Figure 8.49.1 Unit A49 - MINI CCD LOGIC - p.c.b. lay-out. MAT 3527



REF.NR	TYPE	VTTL +5Da	VEE -5Da	VCC DIGITAL GND
D6402	100102Y	23	21	9, 10
D6403	100102Y	23	21	9, 10
D6404	100131Y	23	21	9, 10

MAT 35 20

Figure 8.49.2 Unit A49 - MINI CCD LOGIC - circuit diagram.

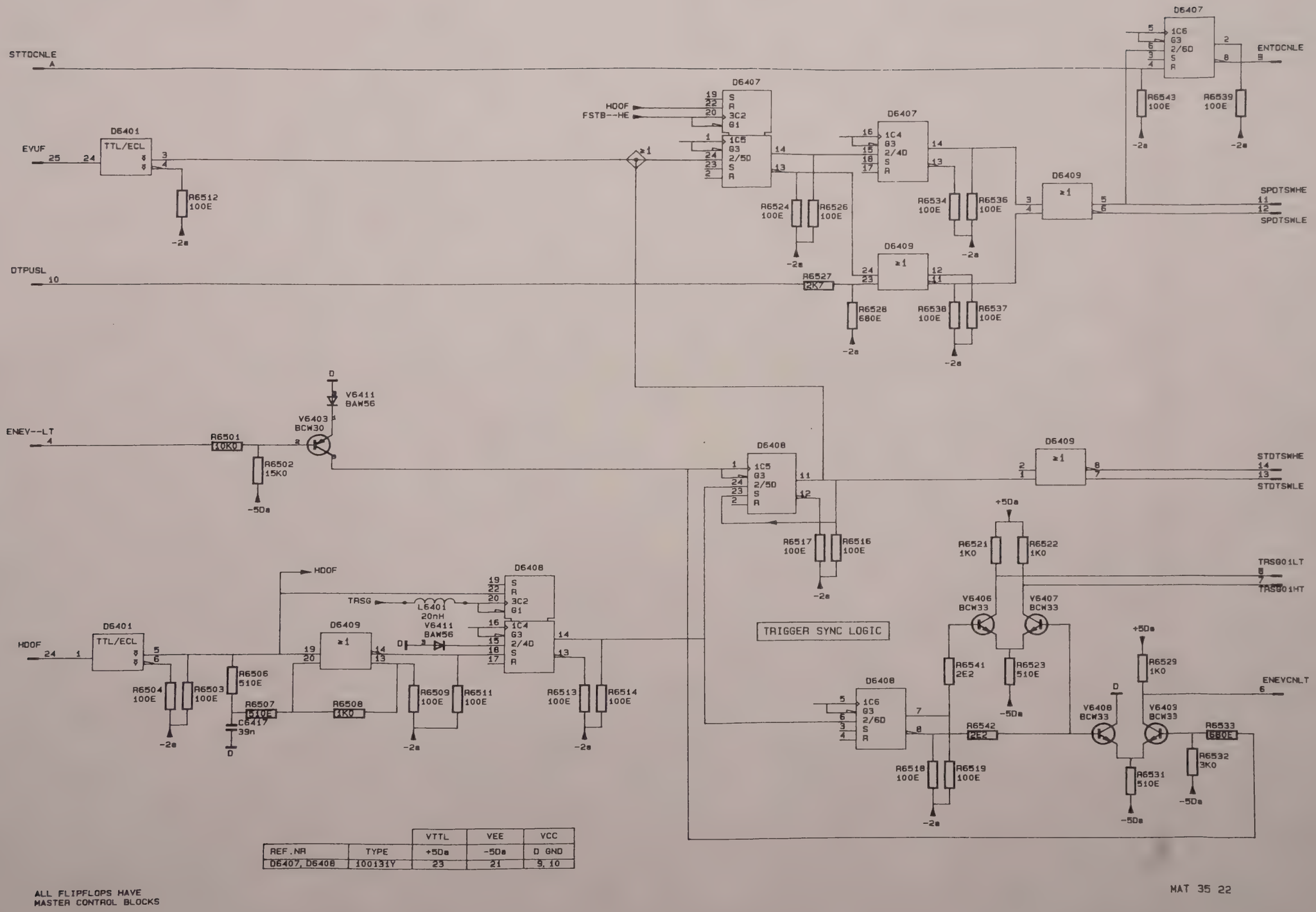


REF.NR	TYPE	VTTL +5Da	VEE -5Da	VCC D GND
D6401	F100124FC	23	21	9, 10, 11
D6403, D6409	100102Y	23	21	9, 10
D6404, 6406	100131Y	23	21	9, 10

TYPE	CODE
BCW30	C2
BCW33	D3
BAW56	A1

MAT 35 21

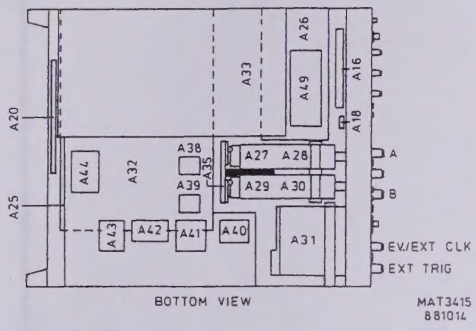
Figure 8.49.3 Unit A49 - MINI CCD LOGIC - circuit diagram.



REF.NR	TYPE	VTTL	VEE	VCC
		+5Da	-5Da	D GND
D6407, D6408	100131Y	23	21	9, 10

Figure 8.49.4 Unit A49 - MINI CCD LOGIC - circuit diagram.

UNIT A50 - OFFSET ADAPTION UNIT



CONTENTS

8.50.1 Circuit description..... 8.50-1
8.50.2 Signal name list..... 8.50-1

8.50.1 Circuit description

The offset adaption unit, which is located between the vertical attenuators, consist of two common mode suppression circuits for the offset signals for both channels and a number of interconnections, for the control signals for the channel A attenuator.
Each suppression circuit (N7462 for channel A and N7461 for channel B) consists of an opamp circuit, which suppresses common mode interference signals on the AOSA and SOSA inputs (AOSB and SOSB for channel B). The differential signal between both inputs, which is the offset signal, is amplified one time. The output signals (OSA and OSB) are applied to the LF vertical attenuator units A28 (channel A) and A30 (channel B), via the attenuator adaption unit A35.

8.50.2 Signal name list

UNIT A50

Signal name	Description	Signal source	Signal destination(s)
ACDCA	AC-DC input coupling A	A25	-
AOSA	Analog offset A	A25	-
AOSB	Analog offset B	A25	-
AT1A	Attenuator x1 A	A25	-
AT1ØA	Attenuator x1ØA	A25	-
AT1ØØA	Attenuator x1ØØA	A25	-
OSA	Offset A	A50	A35-A28
OSB	Offset B	A50	A35-A30
PRIFA-XA	Probe information A	A27+A28	-
PT5ØA-LT	50 ohm protection A	A27	-
SOSA	Shield offset A	A25	-
SOSB	Shield offset B	A25	-
TM5ØA	Termination 50 ohm A	A25	-
ØA	Analog ground	A25	-

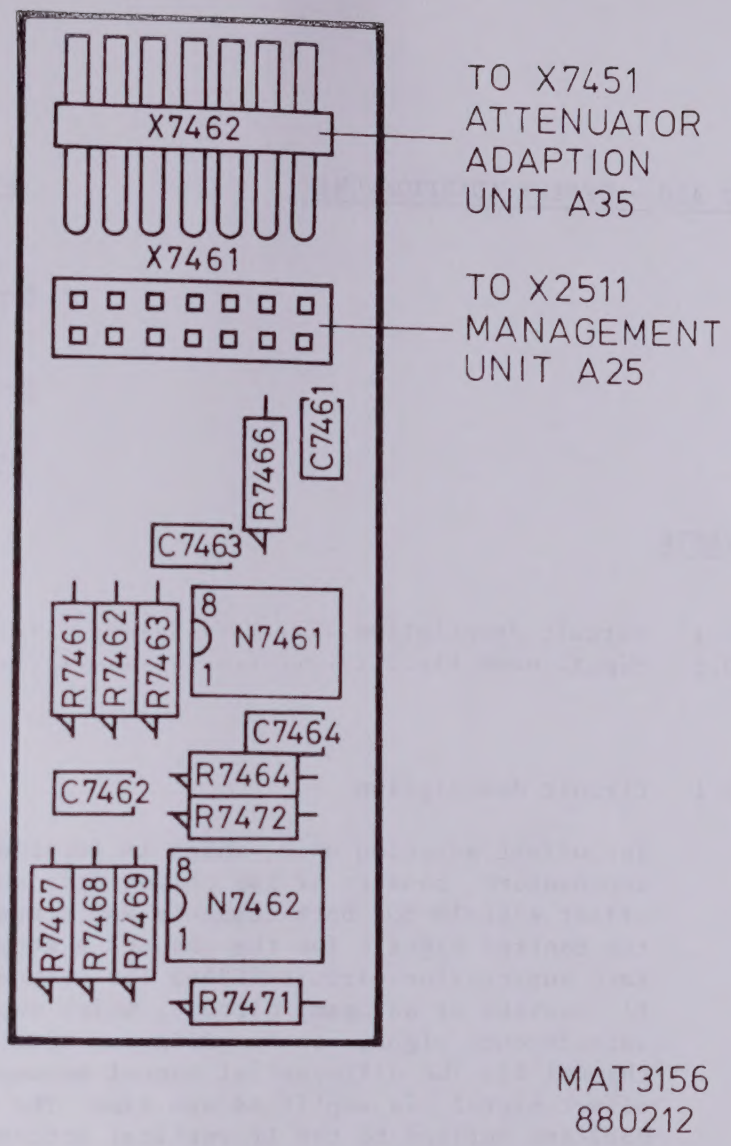


Figure 8.50.1 Unit A50 - OFFSET ADAPTION UNIT - p.c.b. lay-out.

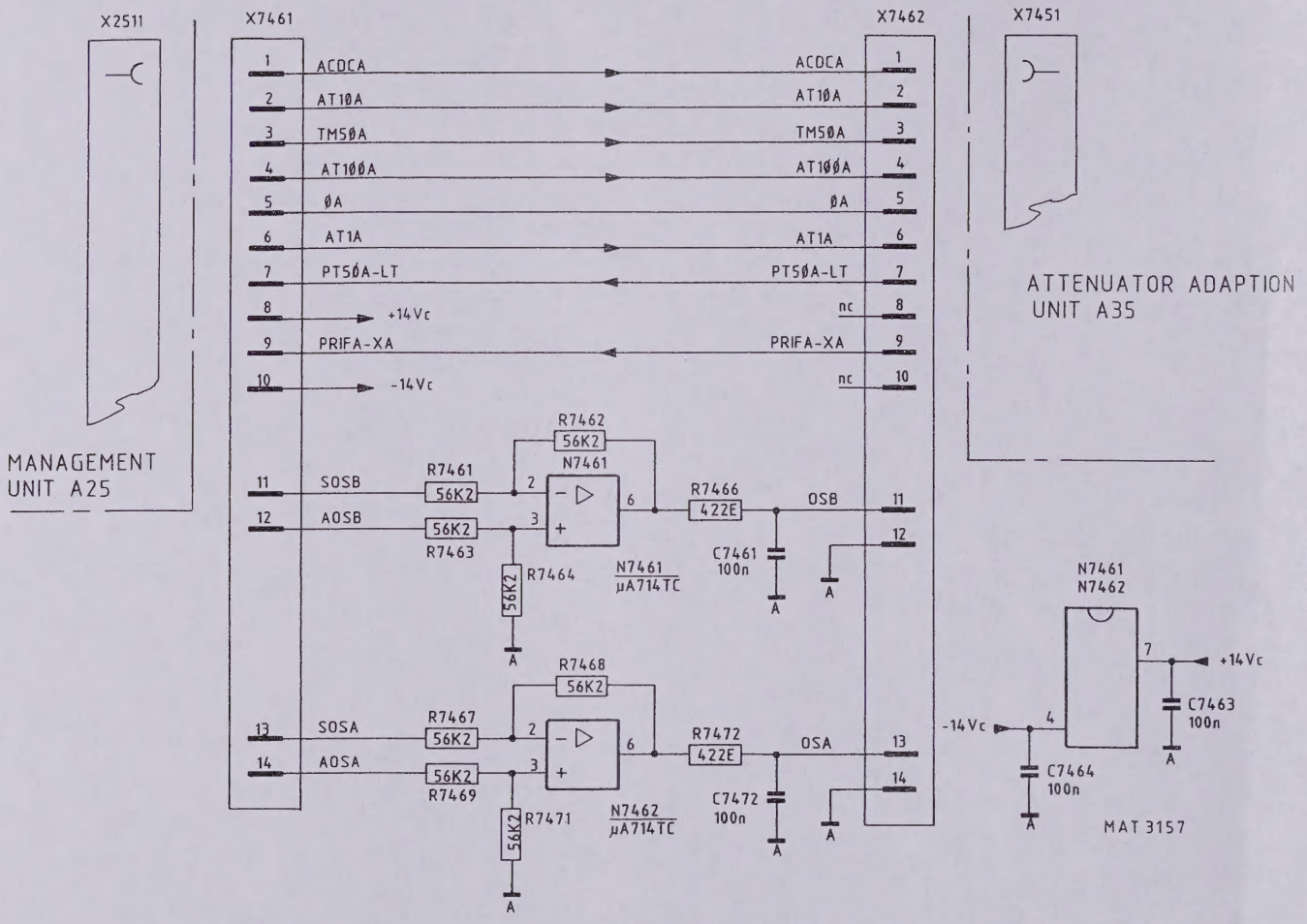


Figure 8.50.2 Unit A50 - OFFSET ADAPTION UNIT - circuit diagram.